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# K/Ka-Band Eight-Way Power-Combined Power Amplifier in 180 nm E-Mode GaAs


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***Abstract*—In this work, the design of a broadband K/Ka-band Power Amplifier (PA) Monolithic Microwave Integrated Circuit (MMIC) in 180 nm E-mode GaAs pHEMT technology is discussed. In small-signal the design has a flat frequency response from 23.8 GHz - 28.7 GHz covering a fractional bandwidth of 19.2%, with a maximum gain of 34.9 dB at 25.5 GHz. On top of that, the PA has a maximum output power of 28.5 dBm and a maximum Power-Added Efficiency (PAE) of 20.6%.**



***Index Terms*—Broadband Amplifiers, Power Amplifiers, Gallium Arsenide, K-Band, MMICs**


## I. Introduction

With the ever-increasing demands from the automotive and satellite communications sector in the K- and Ka-bands, it is important to advance in the constant development of broadband data transmission and accurate ranging [1]. The main benchmarks for a communication system are the efficiency, number of simultaneous users, distortion performance, and self-heating [2].

In the transmitter design, the PA is the main limiting component due to a trade-off between available linear output power, efficiency, and power consumption. Moreover, it is tricky to design a broadband low-loss power-combining matching network. A higher bandwidth is desired to enhance transmission data rates with modulated signaling.

In this paper, a four-stage K/Ka-band eight-way power-combined PA is presented. The circuit is fabricated on 150 mm GaAs wafers using the WIN Semiconductors PQH1-0P 180 nm E-mode pHEMT technology. The 90 GHz $f_t$, E-mode transistor operates at 4 V, provides 30 GHz minimum noise figure, $F_{min}$, of 1 dB, and 0.5 W/mm saturated output power, $P_{sat}$, at 29 GHz, enabling single supply Low-Noise Amplifier (LNA) and PA designs at millimeter-wave. The main focus is lying on the phase coherence of the combined transistors, diving into component placement and their influences. Additionally, the first driver stage has an option to be driven in a non-linear fashion to potentially linearize the PA [3].

## II. Design Methodology

Fig. 1 presents the layout of the four-stage power-combined PA. In total, the dimensions of the MMIC are 5.1 × 4.5 mm. The choice of the transistor sizing per stage and the design of the matching networks will be discussed in more detail now.

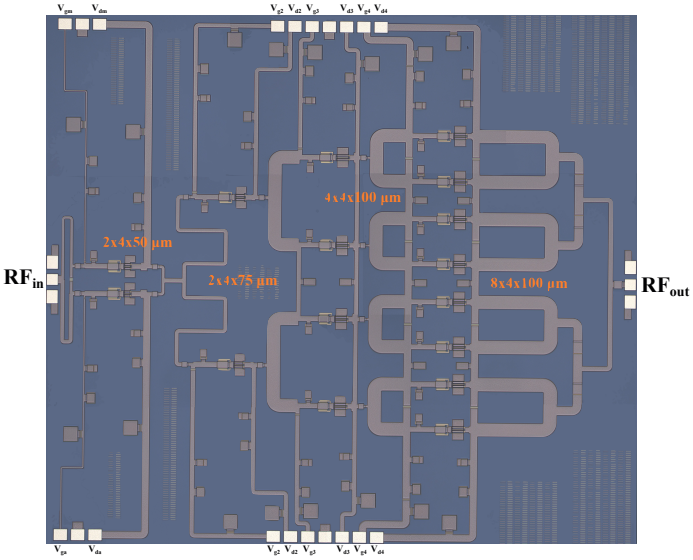


Fig. 1. Layout of the power-combined PA.

### A. Output Matching Network Design

In the design phase of the output stage, a trade-off was made between the available output power, loss of the matching network, and the number of devices that are combined. An output power of more than 30 dBm can easily be achieved by combining four 8 × 100 $\mu$m devices, but the loadpull impedance per device would be close to the edge of the Smith chart at $7.6 + j \cdot 2.1\ \Omega$, increasing the matching losses to our desired 50 Ω termination. Therefore, the choice was made to combine eight 4 × 100 $\mu$m devices, which increases the complexity of the power combining network, but yields a better loadpull impedance of $17.5 + j \cdot 2.9\ \Omega$.

To ensure a broadband output match, the optimum loadpull impedance, $Z_{opt}$, has been investigated for multiple frequency points, namely 23 GHz, 25 GHz, and 27 GHz. Afterwards, the found impedances have been modeled as a frequency-dependent RC-network per device. Fig. 2 depicts two testbenches that have been designed to find the overall matching network loss and to evaluate the phase coherence per branch. This design combines eight devices at the output, so for the overall matching network losses a two-port testbench is created

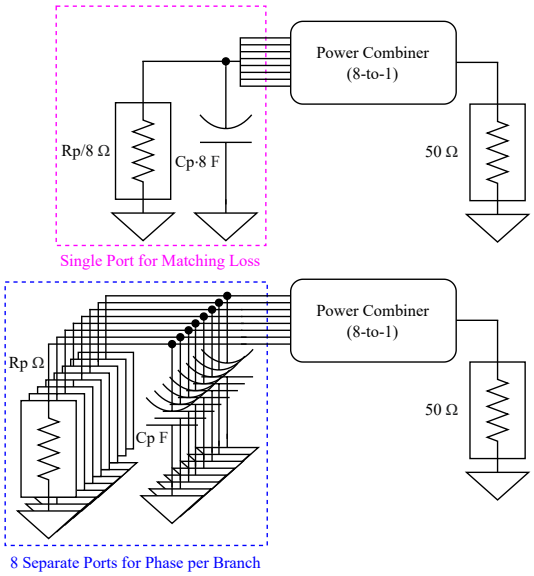


Fig. 2. Power-combining testbenches for matching loss and phase coherence.

by multiplying the capacitance, $C_p$, by eight and dividing the resistance, $R_p$, by eight. For the phase coherence, a nine-port testbench is created, where each combining branch represents a single device with capacitance $C_p$ and resistance $R_p$ [4].

For the output matching network presented in Fig. 1 there are four odd-mode stability resistors between each pair of two $4 \times 100$ $\mu$m devices. Next to that, there are dc decoupling capacitors closely next to the devices, with the vias facing to the transistor drain side to ensure that the phase of neighbouring combining branches are not influenced by additional coupling. Lastly, the top and bottom branch have less coupling (only a single parallel branch), so the output network has been designed asymmetric to ensure phase coherence.

### B. Interstage Matching Network Design

This PA has three distinct interstage matching networks with a different number of combined transistors. The first interstage matching network combines the eight gates of the output stage (eight $4 \times 100$ $\mu$m devices) to the four drains of the third driver stage (four $4 \times 100$ $\mu$m devices). To enhance the gain of the PA, a conjugate match is performed, again making use of a frequency-dependent RC-model for the gate and drain impedances. Similar to what is shown in Fig. 2, a two-port testbench can be made by manipulating the drain impedances by a factor of four and the gate impedances by a factor of eight, taking into account the number of devices used.

The second interstage matching network combines the four gates of the third driver stage (four $4 \times 100$ $\mu$m devices) to the two drains of the second driver stage (two $4 \times 75$ $\mu$m devices). Hence, more aggressive stage tapering is performed at the input, since there is plenty of drive margin available while bringing the dc power consumption down.

Finally, the third interstage matching network combines the two gates of the second driver stage (two $4 \times 75$ $\mu$m devices) to the single (combined) drain of the first driver stage (two $4 \times 50$ $\mu$m devices. The first driver stage employs two devices that can be driven in different operating regions independently to potentially linearize the PA. Moreover, to improve stability, RC-networks have been added to the gates of the transistors, as well as having a small resistor in the gate bias lines. Since the gate has a reactive impedance, small shunt capacitors have been added to ease the matching network design.

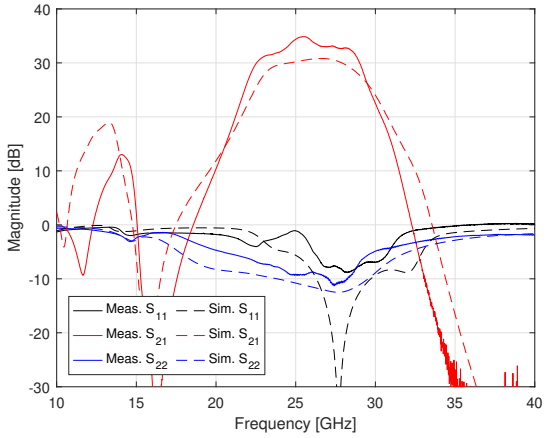


Fig. 3. Measured and simulated S-parameters.

### C. Input Matching Network Design

The input matching network is a conjugate match between the gate impedances of the two $4 \times 50$ $\mu$m devices and the 50 Ω input impedance. To be able to drive both devices differently, e.g. one in class A and one in class C, an unequal isolated Wilkinson power splitter is used, where the impedance in both branches is different with a power splitting ratio of 3.4 dB and 3.9 dB respectively.

## III. Measurement Results

For the measurements, the PA was mounted on an FR-4 carrier PCB, where only the bias lines on a single side of the MMIC were wire-bonded and the RF was still probed. All measurements use the same high-transconductance bias point with current densities $J_{gm} = 244.5$ mA/mm, $J_{ga} = 230.0$ mA/mm, $J_{g2} = 220.2$ mA/mm, $J_{g3} = 250.8$ mA/mm, $J_{g4} = 258.9$ mA/mm, and drain voltage $V_d = 4$ V

### A. Small-Signal Measurements

Initially, the S-parameters of the PA have been measured, where the results are presented in Fig. 3. The maximum small-signal gain is 34.9 dB at 25.5 GHz, and the half-power (3-dB) bandwidth spans from 23.8 GHz - 28.7 GHz, covering a total of 4.9 GHz with a fractional bandwidth of 19.2%. The low-frequency gain response has some deviations due to the lack of PCB parasitics in the simulations.

### B. Large-Signal Measurements

Large-signal measurements have been performed to investigate the PAE and output power of the PA. Fig. 4 depicts the measured large-signal gain compression and PAE for different frequency points versus output power. It can immediately be

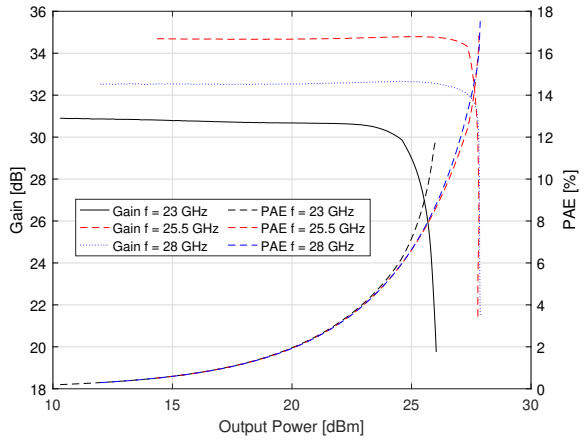


Fig. 4. Measured large-signal gain compression and PAE for different frequencies.

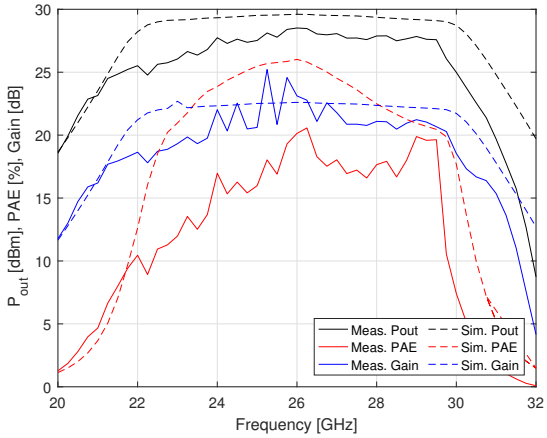


Fig. 5. Measured and simulated large-signal output power, PAE, and gain compression at maximum PAE point per frequency.

seen that the maximum attainable output power is 28.5 dBm, where the PA is fully in compression. Since the PA is biased at the transconductance peak in deep class A, the PAE curves in the back-off region show very low efficiency.

Fig. 5 shows the measured and simulated large-signal output power, PAE, and gain compression at the maximum PAE point per frequency. Comparing measurements and simulations mainly shows a decrease in output power, and thus efficiency due to the poor heat dissipation in the FR-4 carrier PCB. The frequency range and trend of the curves are similar to the simulations. The maximum PAE is 20.6% at 26.3 GHz, rolling off to around 15% at 24 GHz and 29.5 GHz.

## IV. Discussion

In Table 1 the designed PA is compared to the current State-of-the-Art (SotA). It can be seen that this work is competitive to the SotA in terms of available output power and the frequency range. This work has much higher gain than its competitors as it is a four-stage design, where each stage can ideally deliver around 10 dB of small-signal gain. Moreover,

TABLE I
Comparison table of previously-designed K/Ka-band PAs.

| | [2] | [5] | [6] | [7] | [8] | TW[1] |
|---|---|---|---|---|---|---|
| **Tech [-]** | 150 nm GaAs | 150 nm GaAs | 150 nm GaAs | 150 nm GaAs | 100 nm GaAs | 180 nm GaAs |
| **Freq [GHz]** | 20-23 | 16-28 | 24-28 | 21-25 | 18-26[2] | 23.8-28.7 |
| **Gain [dB]** | 9.5 | 12 | 21.3 | 10 | 16-18.5 | 34.9 |
| **Pout [dBm]** | 31.8 | 27[3] | 31 | 29.5-30.2 | 20-24 | 28.5 |
| **PAE [%]** | 24 | 41 | 27.3 | 30-37 | 23-31 | 20.6 |
| **Area [mm$^2$]** | - | 9 | 4.5 | 3.79 | 5 | 23.24 |

[1]This Work [2]Visually estimated [3]Compression point at 1-dB

the PAE is slightly lacking due to the power-hungry output stage and its many drivers.

## V. Conclusion

A K/Ka-band eight-way power-combined PA has been designed in the WIN Semiconductors PQH1-0P 180 nm E-mode GaAs pHEMT technology. In the power combining it is of utmost importance to have phase coherence between all combined branches, which often leads to an asymmetric design. This PA has a maximum small-signal gain of 34.9 dB at 25.5 GHz, together with a bandwidth of 4.9 GHz. In terms of large-signal, the PA has a maximum PAE of 20.6% at 26.3 GHz, as well as a maximum output power of 28.5 dBm.

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## References

[1] T. Sim, S. Lee, D. Lee, W. Choe, M. Kim, S. Kim, Y. Lee, K. Na, and J. Kim, "A ku-band high gain 40 w gan hpa mmic for satellite systems in a 0.25- $\mu$m gan technology," in *2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*. Institute of Electrical and Electronics Engineers Inc., 2024, pp. 31–34.

[2] T. Fersch, R. Quaglia, M. Pirola, V. Camarchia, C. Ramella, A. J. Khoshkholgh, G. Ghione, and R. Weigel, "Stacked gaas phemts: design of a k-band power amplifier and experimental characterization of mismatch effects," in *2015 IEEE MTT-S International Microwave Symposium*. Institute of Electrical and Electronics Engineers Inc., 2015, pp. 1–4.

[3] G. Reza Nikandish, R. B. Staszewski, and A. Zhu, "Broadband fully integrated gan power amplifier with minimum-inductance bpf matching and two-transistor am-pm compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4211–4223, 12 2020.

[4] C. Campbell, *Microwave monolithic power amplifier design*. John Wiley & Sons, Inc, 2013.

[5] N. Mullins, Y. Vega, T. Sonnenberg, and Z. Popovic, "A ku/k/ka-band gaas mmic load-modulated amplifier with a negative group delay output network," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*. Institute of Electrical and Electronics Engineers Inc., 2022, pp. 845–848.

[6] K. Wang, Y. Yan, and X. Liang, "A k-band power amplifier in a 0.15-um gaas phemt process," in *2018 IEEE MTT-S International Wireless Symposium (IWS)*. Institute of Electrical and Electronics Engineers Inc., 6 2018, pp. 1–3.

[7] C. Ramella, V. Camarchia, A. Piacibello, M. Pirola, and R. Quaglia, "Watt-level 21-25-ghz integrated doherty power amplifier in gaas technology," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 5, pp. 505–508, 2021.

[8] D. N. Martin, P. Enrico De Falco, M. Roberg, G. Lasser, and T. W. Barton, "An 18-38-ghz k-/ka-band reconfigurable chireix outphasing gaas mmic power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 3028–3038, 2020.