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AI-Assisted Deep-Learning-Based Design of High-Efficiency Class F Power Amplifiers

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***Abstract*—This article presents a deep-learning-based approach for designing Class F power amplifiers (PAs). We use convolutional neural networks (CNNs) to predict the scattering parameters of pixelated electromagnetic (EM) layouts. Using a CNN-based surrogate model and an evolutionary algorithm, we synthesize complex Class F output networks. As a proof of concept, we implement a gallium nitride (GaN) HEMT Class F PA, achieving a measured output power of 41.6 dBm and a drain efficiency of 74% at 2.9 GHz. The prototype also linearly reproduces a 20-MHz modulated signal with an 8.5-dB peak-to-average power ratio (PAPR), achieving an adjacent channel leakage ratio (ACLR) of −50.7 dBc with digital predistortion (DPD). To the best of our knowledge, this is the first deep-learning-based Class F PA design using pixelated layout structures.**

***Index Terms*—Artificial intelligence (AI), Class F, deep learning, energy efficiency, gallium nitride (GaN), harmonic tuning, machine learning, power amplifier (PA), waveform engineering.**

I. Introduction

THE increasing demand for higher data rates in wireless communication systems has posed significant challenges, particularly in energy efficiency. Among various components, the power amplifier (PA) is the most power-intensive element in base stations. Consequently, the development of highly efficient, waveform-engineered PAs has been a key research focus for decades [1].

The output network of a waveform-engineered PA typically consists of a matching network, a harmonic-tuning network, and a bias network. Traditional designs rely on predefined electromagnetic (EM) topologies based on prior physical insights, using lumped or distributed elements. However, these fixed topologies inherently constrain the design space, limiting the potential for globally optimal performance. Inspired by advances in integrated photonics [2], [3] and metalens antennas [4], a recent trend in microwave circuit design involves pixelating layout geometries into binary matrices [5], [6]. While previous works have explored this approach using traditional optimization and machine learning techniques, they often require manual feature engineering, restricting their adaptability and scalability.

Deep learning has recently emerged as a powerful framework for solving complex EM and circuit design problems, with applications spanning photonics [2], transistor modeling [7], scattering theory [8], and antenna design [9]. Unlike conventional machine learning methods, deep learning can automatically learn hierarchical representations directly from raw data, eliminating the need for manual feature extraction. In PA design, deep-learning-based surrogate models with pixelated layouts have been proposed for design of a wideband class B PA [10]. However, their application to the synthesis of output networks for highly efficient waveform-engineered PAs, such as Class F PAs, remains unexplored.

This letter presents a deep-learning-based approach using convolutional neural networks (CNNs) with pixelated layouts for synthesizing the output network of a Class F PA. The fabricated prototype circuit demonstrates a drain efficiency of 74% and an output power of 41.6 dBm at 2.9 GHz, validating the effectiveness of the proposed methodology.

II. Theory

Harmonic-tuned PAs maximize efficiency and output power by minimizing the overlap between drain current and voltage waveforms through precise harmonic impedance control. Among these, the Class F PA offers excellent performance with a relatively straightforward implementation. Its optimal loading conditions at the fundamental, second, and third harmonics are as follows: $Z_{f_0} = R_{\text{opt}}$, $Z_{2f_0} = 0$, and $Z_{3f_0} = \infty$.

The proposed deep learning approach discretizes a planar circuit layout into a binary grid, where "1" represents metal and "0" represents nonmetal. A deep CNN model, trained on a large dataset of pixelated circuit structures and their scattering parameters (*S*-parameters), serves as a surrogate for time-consuming EM simulations. The trained model efficiently evaluates candidate solutions with an evolutionary algorithm, specifically a genetic algorithm (GA), generating pixelated circuit layouts to achieve the target *S*-parameters [10].

A. Dataset Generation and Augmentation

Our dataset comprises 957728 two-port circuits with the *S*-parameters simulated at 21 discrete frequencies: seven evenly spaced points within 2.4–3 GHz, 4.8–6 GHz, and 7.2–9 GHz. To accelerate training, we generate eight two-port structures from a single four-port EM simulation. Using

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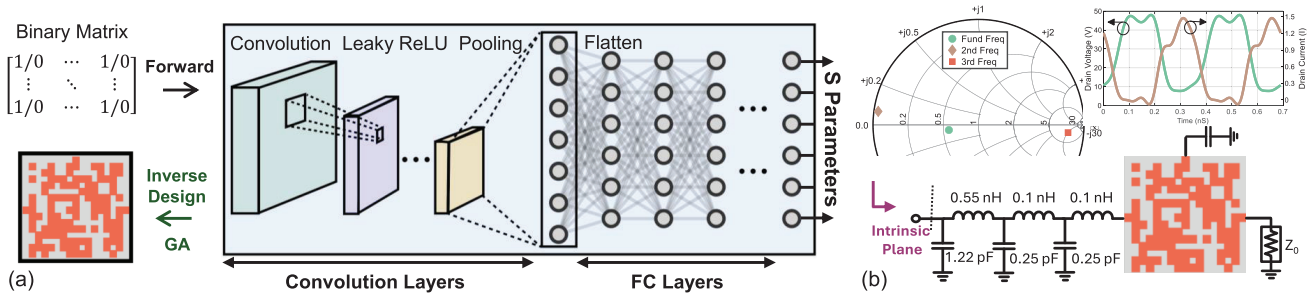

Fig. 1. (a) Trained deep CNN architecture takes a binary matrix input representing the pixelated EM layout and outputs *S*-parameters across the designed frequencies. Once trained, the CNN-based surrogate model accurately predicts the *S*-parameters for any given pixelated EM structure. The forward emulator, derived from the deep CNN architecture, facilitates the inverse synthesis of arbitrary EM structures with desired *S*-parameters. (b) Equivalent output parasitic and package model of the CG2H40010F transistor used in the GA and the simulated results at the transistor's intrinsic plane.

ADS Momentum and Python automation, we simulate around 119716 pixelated four-port layouts, with ports centrally placed on each side of a 15×15 grid. The circuit density follows a normal distribution with a mean of 50% and a standard deviation of 15%. Postprocessing in Python expands each four-port structure into eight two-port circuits by first converting one port into an open circuit, yielding four three-port variations, and then shorting the opposite port to represent the bias network. Finally, mirroring generates four additional circuits per configuration. To ensure reliable direct connections between pixels, we enforce a 10% overlap on each side of the metal pixels. In addition, during data generation, we ensure that 80% of the circuits include a direct connection between ports. This condition is verified using a depth-first search (DFS) algorithm implemented in Python.

B. Deep CNN Model

As shown in Fig. 1(a), the input of the deep CNN architecture is a 15×15 binary matrix and the output is the predicted *S*-parameters. Since we evaluate *S*-parameters at 21 discrete frequencies, each frequency point includes the real and imaginary components of S_{11}, S_{21}, and S_{22}, resulting in a total of 126 values that fully characterize the *S*-parameters.

The deep CNN architecture comprises 14 convolutional layers and five fully connected (FC) layers. To address the vanishing gradient problem and enhance the model's stability and convergence speed, we incorporate a residual network structure [11]. Each convolutional layer uses 32 filters, with specific filter sizes and the corresponding residual connections detailed in Table I. The feature maps generated by the convolutional layers are formatted into a 1-D vector using a flattening layer, enabling the FC layers to process the extracted information. Each of the five FC layers contains 2048 neurons and use the leaky rectified linear unit (ReLU) activation function to introduce nonlinearity [12]. To prevent overfitting, we apply a 30% dropout rate and *L*2 regularization, followed by batch normalization [13].

We trained the deep CNN using Python's TensorFlow library on an Nvidia RTX 3090 GPU for eight hours. The final trained model is 375 MB. Once trained, the CNN-based surrogate model rapidly predicts various pixelated circuit topologies, significantly accelerating the design process.

TABLE I
DETAILS OF THE DEEP CNN ARCHITECTURE

Conv. Layer	Filter Size	Filter Number	Layer Input
L_1	12×12	32	$\text{Matrix}_{\text{in}}$
L_2	12×12	32	L_1
L_3	10×10	32	L_2 + $\text{Matrix}_{\text{in}}$
L_4	10×10	32	L_3
L_5	8×8	32	L_4 + L_2
L_6	8×8	32	L_5
L_7	6×6	32	L_6 + L_4
L_8	6×6	32	L_7
L_9	5×5	32	L_8 + L_6
L_{10}	5×5	32	L_9
L_{11}	4×4	32	L_{10} + L_8
L_{12}	4×4	32	L_{11}
L_{13}	3×3	32	L_{12} + L_{10}
L_{14}	3×3	32	L_{13}

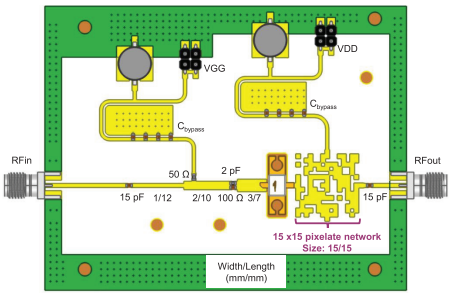

Fig. 2. Circuit schematic of the proposed deep-learning-aided class F PA.

C. Class F PA Output Network Synthesis

After training, the deep CNN-based surrogate model is integrated with a population-based GA [14], using the Python library pyGAD. To maintain population diversity, we use tournament selection and an injection-based mutation mechanism, introducing entirely new matrices to enhance variation. As shown in Fig. 1(b), the equivalent output parasitic and package model of the used CG2H40010F transistor is cascaded with the pixelated layout structure to form a new two-port network [15]. The optimization goal is to achieve Class F loading conditions at fundamental and harmonic frequencies at the transistor's intrinsic plane.

III. PROTOTYPE DESIGN

The complete schematic of the proposed deep-learning-aided Class F PA prototype circuit is shown in Fig. 2. The circuit is implemented on a 20-mil Rogers 4350B substrate,

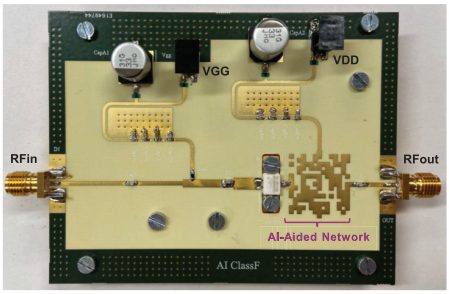

Fig. 3. Photograph of the fabricated deep-learning-aided Class F PA prototype.

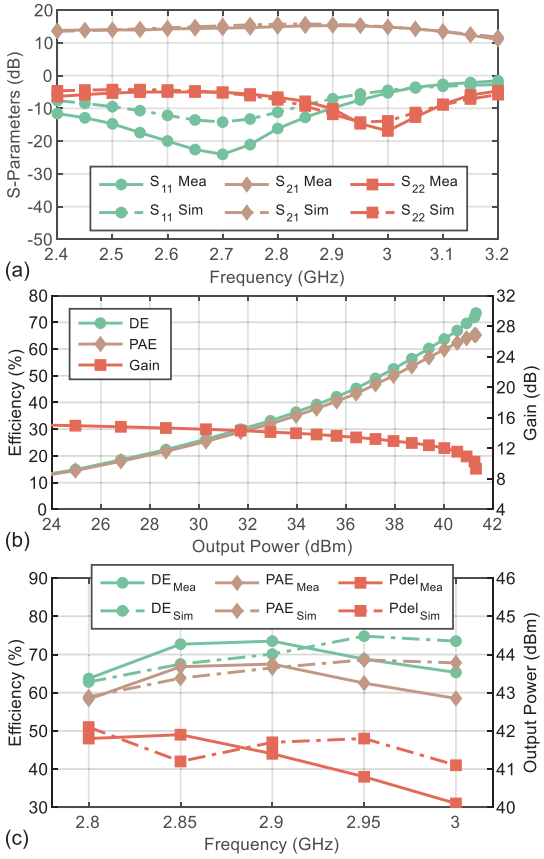

Fig. 4. (a) Measured and simulated small-signal performance, (b) measured large-signal performance at 2.9 GHz, and (c) measured and simulated large-signal performance across frequencies for the fabricated Class F PA prototype.

using a 10-W packaged gallium nitride (GaN) HEMT transistor from Macom as the active device. The output network, designed with the proposed method, features a compact 15×15 pixelated structure, with each pixel having dimensions of 1.2×1.2 mm to balance pixel coupling considerations and training resource constraints. Integrated with the transistor's parasitic and package network, this layout provides the necessary fundamental and higher order harmonic impedances for Class F operation. At the saturated power level, the prototype demonstrates a distinct Class F PA waveform at the intrinsic plane, as illustrated in Fig. 1(b).

IV. Measurement Results

Fig. 3 presents a photograph of the fabricated Class F PA. During the measurements, the drain bias voltage of the PA is set to V_{DD} = 28 V, and the gate bias voltage is fixed at V_{GG} = −2.85 V. Fig. 4 illustrates the simulated and measured small-signal and large-signal performance of the fabricated prototype circuit. The results show excellent agreement between the measured and simulated data across the design frequencies. At 2.9 GHz, the prototype achieves a measured drain efficiency of 74% and an output power of 41.6 dBm. The performance of the prototype is also assessed using a 20-MHz orthogonal frequency division multiplexing (OFDM) signal, with an 8.5-dB peak-to-average power ratio (PAPR). As shown in Fig. 5, the adjacent channel leakage ratio (ACLR) of the prototype improves from −32.6 to −50.7 dBc after applying digital predistortion (DPD) [22]. The performance of the prototype PA is benchmarked against state-of-the-art high-efficiency PAs in Table II, which exhibits its excellent efficiency compared with previously published designs.

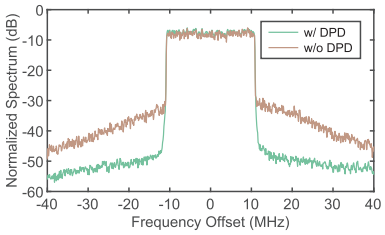

Fig. 5. Normalized spectrum of the prototype circuit with a 20-MHz, 8.5-dB PAPR OFDM signal at 2.9 GHz before and after applying DPD.

TABLE II
Summary of State-of-the-Art High-Efficiency PAs

Ref.	Arch.	f_0 (GHz)	η_{SAT} (%)	P_{SAT} (dBm)	Gain (dB)	ACLR (dBc)
[16] 2022	class E	2.5	70	40.8	15.1	N.A.
[17] 2022	class F	1.7	72*	41.7	9.2	−49.0
[18] 2023	class F^{-1}	3.0	65*	38.4	10.3	N.A.
[19] 2023	class F^{-1}	2.3	77	40.8	12.3	−56.1
[20] 2024	class F^{-1}	3.7	71	40.3	10.6	−46.4
[21] 2024	class J^{HI}	1.7	82	40.5	14.3	N.A.
This Work	**class F**	**2.9**	**74**	**41.6**	**11.2**	**−50.7**

a ^{HI} stands for harmonic injection, b * PAE is reported

V. Conclusion

In this article, we present a deep-learning-based approach for designing high-efficiency Class F PAs. The design process combines a deep CNN architecture as a forward model to predict the behavior of pixelated EM structures with an evolutionary algorithm for inverse design. As a proof of concept, we design and fabricate a GaN HEMT Class F PA prototype using the proposed approach. When used in combination with a standard DPD, the prototype achieves excellent efficiency and linearity, satisfying the stringent requirements of modern wireless communication standards.

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