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Novel D-Band Up-Conversion Mixer Designs in 130-nm SiGe BiCMOS technology

Marzieh Mollaalipouramiri

CHALMERS

Microwave Electronics Laboratory,
Department of Microtechnology and Nanoscience (MC2)
CHALMERS UNIVERSITY OF TECHNOLOGY
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Marzieh Mollaalipouramiri

Chalmers University of Technology
Microtechnology and Nanoscience - MC2
Microwave Electronics Laboratory
SE-412 96 Göteborg, Sweden
Phone: +46 (0) 31 772 1000

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Abstract

The rapid advancement of digital technologies and the increasing demand for ultra-fast, reliable, and low-latency communication systems have driven the exploration of higher-frequency bands, such as the D-band (110–170 GHz), for next-generation wireless networks. This thesis addresses the critical challenges in designing high-performance up-conversion mixers for D-band communication systems. The D-band, with its wide bandwidth and compact implementation potential, is particularly promising for high-capacity backhaul links, satellite communications, and advanced imaging systems. However, designing mixers for this frequency range presents significant challenges, including achieving high linearity, output power, wide bandwidth, local oscillator suppression, I-Q imbalance (for I-Q mixers), noise, energy efficiency, and circuit compactness while maintaining high isolation between ports.

To address these challenges, in this thesis, two novel mixer architectures are proposed: a cascode mixer and a Darlington mixer, both implemented using 130-nm SiGe BiCMOS technology. The cascode mixer employs a double-mixing technique within a balanced cascode topology, where the first stage (common-emitter transistors) performs initial signal conversion, and the second stage (common-base transistors) enhances the RF signal through double mixing. This design achieves high linearity, robust LO-RF isolation, and enhanced RF output power, making it suitable for high-performance D-band communication systems. On the other hand, the Darlington mixer leverages the Darlington configuration to improve current gain and bandwidth while maintaining low DC power consumption, offering a compelling balance between performance and energy efficiency, making it ideal for low-power and low-voltage applications. Both designs were fabricated and tested, demonstrating competitive figures of merit (FOM) in terms of linearity, isolation, and power efficiency.

Keywords: D-band, up-conversion mixer, SiGe BiCMOS, cascode mixer, Darlington mixer, high-frequency communication, 5G, 6G, linearity, DC power efficiency, wireless networks, double mixing, microwave monolithic integrated circuit (MMIC).

List of publications

Appended Publications

The research presented in this thesis is derived from the work documented in the following papers:

[A] M Mollaalipour, M. Bao, Y. Yan and H. Zirath, "D-Band Cascode Up-Conversion Mixer Utilizing Double Mixing Technique for Enhanced Linearity and Output Power in 130-nm SiGe Process," *IEEE Trans. Microw. Theory Tech.* DOI: 10.1109/TMTT.2025.3560920.

[B] M Mollaalipour, M. Bao, Y. Yan and H. Zirath, "An Efficient and Compact D-Band Darlington Up-Conversion Mixer," to be submitted to *IEEE Microw. Wireless Compon. Lett.*

Other Publications

The content of the following publication is out of the scope of this thesis.

[a] M. Mollaalipouramir, K. Buisman, C. Fager and H. Zirath, "Low Power and High Linear, Low Noise Amplifier Designed in 22nm FDSOI Technology for 5G Wireless Systems," *IEEE APMC 2023. Taipei, Taiwan*, Dec. 2012, pp. 778–780.

Notations and Abbreviations

Notations

P_{sat}	Saturation power
f_T	Transition frequency
f_{max}	Maximum oscillation frequency
P_{1dB}	1 dB compression point
g_m	Transconductance
g_0	Average transconductance
g_n	nth Harmonic of Transconductance
V_b	Base Bias Voltage
BV_{CEO}	Collector-emitter breakdown voltage
α	Duty cycle of a waveform
ω	Angular frequency ($\omega = 2\pi f$)
C_π	Base-emitter capacitance of a transistor
V_t	Threshold voltage

Abbreviations

BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
ADAS	Advanced Driver Assistance Systems
BJT	Bipolar Junction Transistor
HBT	Heterojunction Bipolar Transistor
HPC	High-Performance Computing
HFC	High-Frequency Capability
IC	Integrated Circuit

IoT	Internet of Things
LO	Local Oscillator
MIM	Metal-Insulator-Metal
mmWave	Millimeter-Wave
MRI	Magnetic Resonance Imaging
NPN	Negative-Positive-Negative (transistor type)
PDK	Process Design Kit
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SOI	Silicon-On-Insulator
SoC	System-on-Chip
FOM	Figure of Merit
RF	Radio Frequency
IF	Intermediate Frequency
AMC	Active Multiplier Chain
THz	Terahertz
PNA-X	Keysight's Performance Network Analyzer
WR6.5	Waveguide band covering 110–170 GHz
GSG	Ground-Signal-Ground
CG	Conversion Gain
VR	Virtual Reality
AR	Augmented Reality
D-band	Frequency range of 110–170 GHz
IM3	Third-order intermodulation distortion
IM2	Second-order intermodulation distortion
BW	Bandwidth
FOM	Figure of Merit
5G	Fifth-generation wireless technology
6G	Sixth-generation wireless technology
TL	Transmission Line
Class-B	A type of amplifier
LO-to-RF	Local Oscillator to Radio Frequency isolation
IF-to-RF	Intermediate Frequency to Radio Frequency isolation
SiGe HBT	Silicon Germanium Heterojunction Bipolar Transistor

B11HFC	A specific 130-nm SiGe BiCMOS process by Infineon Technologies
AMC	Active Multiplier Chain
GaN	Gallium Nitride
InP	Indium Phosphide
VDI	Virginia Diodes Inc. (Equipment provider)

Contents

Chapter 1

Introduction

1.1 Motivation and Opportunities

Digital technologies are advancing at an unprecedented rate, driving a transformative era of connectivity and innovation that is reshaping industries, economies, and societies worldwide. Central to this transformation is the global push for digitalization, which is placing extraordinary demands on communication networks. The transition toward smart cities, autonomous systems, immersive virtual environments, and real-time healthcare solutions has heightened the need for ultra-fast, reliable, and low-latency communication. This demand is driving researchers and industry leaders to explore advanced wireless technologies, particularly in higher-frequency communication bands.

Emerging technologies such as autonomous vehicles, virtual reality (VR), augmented reality (AR), the Internet of Things (IoT), and next-generation healthcare systems are no longer futuristic concepts but tangible realities that require robust communication infrastructures. These applications rely on the seamless transmission of vast amounts of data with minimal delay, pushing the boundaries of existing wireless technologies. To address these challenges, the focus has shifted toward higher-frequency bands, such as millimeter-wave (mmWave) and sub-terahertz (sub-THz) ranges, which offer the bandwidth necessary for high-speed communication systems. These bands are critical for the development of advanced wireless networks, including 5G and the emerging 6G [1]-[3].

Among these higher-frequency bands, the D-band (110–170 GHz) stands out as a particularly promising frontier. Its wide bandwidth, compact implementation potential, and versatility make it well-suited for various advanced applications. In 5G and future networks, the D-band plays a vital role in high-capacity backhaul links, efficiently connecting base stations to core networks to accommodate the exponential growth in data traffic. Additionally, its high-frequency characteristics make it an ideal candidate for satellite communications, enabling high-throughput links for seamless global connectivity [4]-[9].

Beyond telecommunications, the D-band holds immense potential in consumer electronics, such as wireless high-definition video streaming, where minimal latency and

robust signal quality are critical. It is also revolutionizing advanced imaging systems in fields like security, automotive radar, and medical diagnostics, where its ability to deliver high-resolution, precise outputs is transformative.

As the demand for faster, more reliable, and versatile communication solutions grows, the D-band emerges as a cornerstone of next-generation technologies. Its unique properties and wide-ranging applications underscore its potential to drive innovation across industries.

1.2 Challenges in D-Band Mixer Design

Despite its advantages, designing communication systems for the D-band poses significant challenges. In the transmitter, the up-conversion mixer plays a pivotal role in converting intermediate frequency (IF) signals to the desired radio frequency (RF) band using a local oscillator (LO) signal. Its performance directly impacts on the overall efficiency, reliability, and scalability of the communication system. Achieving optimal performance in D-band mixers requires addressing several key challenges [10]:

1. High Linearity: Maintaining linearity is critical for supporting complex modulation schemes, which are essential for achieving high data rates and signal integrity over long distances.
2. High Output Power: Mixers must deliver sufficient output power to meet the demands of high-performance communication systems, especially for long-range or high-data-rate applications.
3. Wide Bandwidth: The large spectral resources in the D-band necessitate mixers that can efficiently handle wide bandwidths to maximize data throughput.
4. Energy Efficiency: With the growing emphasis on sustainable and cost-effective solutions, minimizing power consumption is required in mixer design.
5. Compactness: The demand for miniaturized electronic components requires mixer designs that can fit within limited spaces while maintaining high performance and reducing the cost.
6. High Isolation: Ensuring proper LO-RF isolation is crucial to minimize interference, prevent saturation of the subsequent power amplifier (PA), and preserve signal quality, especially in systems with tightly integrated components.

Conventional mixer designs face notable challenges in meeting the demands of D-band communication systems. The double-balanced Gilbert mixer, a commonly used topology, offers high conversion gain and effective LO-RF isolation. However, its large chip size, high DC power consumption, and low output power make it less suitable for energy-efficient and compact designs [11], [12]. Resistive mixers, while offering more linearity and power efficiency, may exhibit conversion losses that can impact overall signal quality, although these losses can be mitigated with subsequent amplification.

While a passive architecture offers advantages such as lower power consumption and improved noise performance, its relatively low conversion gain often necessitates additional amplification stages, making it less suitable for applications that demand inherently high output power [13].

These limitations underscore the need for innovative active mixer designs that can address these challenges while maintaining high performance and efficiency.

1.3 Novel Approaches in D-Band Mixer Design

To address the challenges of D-band operation, this thesis introduces two innovative up-conversion mixer architectures based on transconductance mixers. Transconductance mixers offer a balanced trade-off between linearity, power efficiency, and conversion gain [14]. The proposed designs build upon this foundation, integrating advanced techniques to enhance performance at D-band frequencies (110–170 GHz).

One of the proposed architectures is the cascode up-conversion mixer, which employs a novel double-mixing technique within a cascode topology. In this design, the LO and IF signals are applied to a common-emitter (CE) transistor, with a cascoded common-base (CB) transistor remixing these signals at the CE transistor's collector. This configuration enhances linearity, improves saturated output power, and ensures robust LO-RF isolation due to its balanced design. Its balanced architecture minimizes spurious signal generation, making it well-suited for high-order modulation schemes and extended communication ranges. While the mixer operates effectively within a targeted frequency range, its compact layout is ideal for space-constrained systems.

The second proposed architecture is the Darlington-pair based up-conversion mixer leverages the high input impedance and gain of the Darlington configuration to achieve efficient operation with minimal power consumption, delivering significantly higher gain and output power than a single-transistor stage.

Both designs represent significant advancements in D-band circuit design, effectively addressing common limitations such as low output power, linearity, and high energy consumption. By overcoming these challenges, this thesis introduces innovative solutions that push the boundaries of high-frequency circuit performance.

These contributions advance the state-of-the-art in D-band wireless systems, enabling ultra-high-speed and energy-efficient communication networks. Beyond enhancing connectivity, the proposed designs open new possibilities for applications in imaging, radar, and other cutting-edge technologies, shaping the future of wireless innovation and fostering breakthroughs in next-generation systems.

The outline of the thesis is as follows: Chapter 2 examines SiGe BiCMOS technology and transconductance mixers, focusing on SiGe's role in high-frequency applications and transconductance mixer design principles. Chapter3 introduces cascode and Darlington pair mixer architectures for D-band communication, detailing their design and performance. Chapter 4 presents measurement results, evaluating key performance metrics and benchmarking against state-of-the-art designs. Chapter 5 concludes with key contributions, implications for future wireless systems, and directions for future work.

Chapter 2

SiGe BiCMOS Technology and Transconductance Mixer Fundamentals

The rapid evolution of semiconductor technology has been a cornerstone of modern electronics, driving advancements in communication, computing, and sensing systems. Among the myriads of semiconductor materials, Silicon Germanium (SiGe) has emerged as a transformative material, offering a unique combination of high electron mobility, thermal stability, and compatibility with existing silicon-based fabrication processes. These properties make SiGe particularly well-suited for high-frequency and high-precision applications, such as radio frequency (RF) circuits, millimeter-wave (mmWave) communication, and next-generation wireless technologies like 5G and beyond. This chapter delves into the fundamental aspects of SiGe BiCMOS technology and its pivotal role in enabling high-performance integrated circuits (ICs) for a wide range of applications.

In addition to exploring the material properties and technological advancements of SiGe, we discuss transconductance mixers, a critical component in RF and microwave systems.

The chapter begins with an overview of semiconductor materials, highlighting the evolution from traditional silicon to advanced materials like SiGe, Silicon Carbide (SiC), and Silicon-on-Insulator (SOI). It then focuses on the unique advantages of SiGe, particularly its integration with BiCMOS technology. This combination has enabled the development of cost-effective, high-performance system-on-chip (SoC) solutions, exemplified by the 130 nm SiGe BiCMOS process from Infineon Technologies.

Following the discussion on SiGe BiCMOS technology, the chapter transitions to the fundamentals of transconductance mixers, detailing their operational principles, circuit configurations, and design trade-offs. By examining the small-signal equivalent circuits and the role of harmonic mixing, this section provides valuable insights into optimizing mixer performance for various applications.

2.1 Semiconductor Materials and SiGe BiCMOS Technology

2.1.1 Introduction to Semiconductor Materials

Over the past fifty years, the semiconductor industry has witnessed remarkable advancements, fueled by extensive research and development into various materials [15]. Semiconductor materials are the foundation of modern electronics, enabling the development of devices that power everything from smartphones to satellite communication systems. Each material offers unique properties that cater to specific applications, shaping the landscape of electronic innovation.

Among these materials, silicon (Si) has emerged as the most widely utilized due to its advantageous properties. Silicon's low raw material cost, high availability, and excellent manufacturing yield make it a cost-effective choice for large-scale production [15].

Additionally, its relatively high thermal conductivity enhances its performance under operational conditions, further cementing its position as a cornerstone of semiconductor technology.

The Evolution of Silicon Technology

The versatility of silicon has been instrumental in the development of increasingly compact and powerful integrated circuits (ICs). By combining silicon with other elements, researchers have created new materials with enhanced properties. Notable examples include:

- Silicon Germanium (SiGe): Offers higher electron mobility compared to pure silicon, making it an excellent choice for high-frequency and high-speed applications, such as RF and millimeter-wave circuits [16].
- Silicon Carbide (SiC): Known for its outstanding thermal stability, Silicon Carbide (SiC) has become essential in power electronics, especially for high-temperature and high-power application [17], [18].
- Silicon-on-Insulator (SOI): Reduces parasitic capacitance by isolating the active silicon layer from the substrate, enabling faster signal processing and improved energy efficiency in high-speed and low-power applications [19].

These innovations have revolutionized industries such as telecommunications, healthcare, and automotive technology, driving the adoption of high-performance devices.

Compound Semiconductor Materials in Emerging Technologies

The integration of compound semiconductors in emerging technologies has unlocked new potential across various industries. For example:

- Aerospace and Defense: The high-speed capabilities of SiGe are indispensable in radar and satellite communication systems [16].
- Autonomous Vehicles: SiC's high thermal stability and efficiency make it crucial for electric vehicle powertrains [20], [21].
- Healthcare Devices: Advanced bio-sensors and implantable devices frequently utilize SOI technology's minimized parasitic capacitance to achieve precise signal processing [22].

By understanding the specific properties of these materials, engineers and researchers continue to push the boundaries of what is possible in semiconductor design.

2.1.2 Silicon Germanium: A Modern Semiconductor

Silicon Germanium (SiGe) marks a major breakthrough in semiconductor technology, offering enhanced performance and capabilities that surpass traditional materials. By alloying germanium with silicon, researchers have achieved a material that combines the best of both worlds: the established reliability of silicon and the superior electrical properties of germanium. SiGe's enhanced electron mobility and compatibility with silicon manufacturing processes have made it a go-to material for high-frequency and high-performance applications [23], [24].

Applications of SiGe

SiGe has become indispensable in fields that demand high-speed performance and efficient signal processing. Key applications include:

1. Automotive Radar Systems: SiGe is used in radar systems for ADAS (Advanced Driver Assistance Systems) and autonomous vehicles, enabling object detection and collision avoidance. Its high-frequency performance is critical for reliable operation in harsh environments [25].
2. Satellite Communication: It is ideal for satellite transceivers, supporting high-frequency operation and low noise for global communication networks, including GPS and satellite internet [24].
3. Medical Imaging and Healthcare Devices: It is used in MRI, ultrasound, and implantable medical devices due to its high-frequency signal processing and low power consumption [26].
4. Aerospace and Defense: It is employed in radar, electronic warfare, and communication systems, offering high reliability and performance in demanding environments [16].
5. Optical Communication: It enables high-speed transceivers for fiber-optic networks, supporting data centers and telecommunications with efficient signal conversion [27].

6. IoT Devices: It used in IoT applications like smart sensors and wireless modules, providing low power consumption and high performance for connected devices [16].
7. High-Performance Computing (HPC): It supports high-speed processors and memory interfaces in data centers and supercomputers, enabling faster data processing [28].
8. Energy Harvesting and Power Electronics: It is used in energy harvesting systems and power electronics, such as DC-DC converters, for renewable energy and electric vehicles [29].

Advantages of SiGe in Modern Electronics

SiGe's properties make it a standout choice for modern electronic applications [16]:

- High Electron Mobility: Enhances speed and reduces power loss.
- Thermal Stability: SiGe's robust thermal properties make it suitable for high-frequency and high-power applications.
- Process Compatibility: Integrates seamlessly with existing silicon fabrication technologies, keeping production costs low.
- Flexibility: Supports a wide range of applications from low-power devices to high-frequency systems.
- High-Speed Operation: SiGe HBTs exhibit superior cutoff frequencies (f_T) and maximum oscillation frequencies (f_{max}), reaching up to 700 GHz for advanced processes.
- Cost-Effectiveness: The compatibility of SiGe with existing silicon fabrication processes ensures scalability and economic viability.

These attributes highlight SiGe as a versatile and efficient material that addresses the growing demands of advanced electronic systems.

SiGe in BiCMOS Technology

The integration of SiGe with BiCMOS technology has provided new possibilities in IC design. SiGe BiCMOS technology leverages the high-speed characteristics of SiGe heterojunction bipolar transistors (HBTs) alongside the low-power versatility of CMOS transistors. This combination enables the development of high-performance system-on-a-chip (SoC) solutions that are both cost-effective and scalable.

2.1.2 The 130 nm SiGe BiCMOS Process

This thesis explores the design and implementation of proposed circuits using the 130 nm SiGe BiCMOS technology developed by Infineon Technologies. By leveraging the

combined advantages of SiGe and CMOS, this advanced process provides a robust foundation for creating high-frequency, high-performance integrated circuits (ICs).

Key Features of the Process

The 130 nm SiGe BiCMOS process is a comprehensive technology that integrates the following key components [30]:

- NPN Transistors: Available in high-speed, medium-speed, and high-voltage variants.
- MOS Transistors: Complementary components for digital and analog applications.
- Passive Components: Includes metal film resistors, metal-insulator-metal (MIM) capacitors, junction capacitors, and PIN diodes.
- Interconnect System: A six-layer system (M_1-M_6) with copper metallization. The upper layers (M_5-M_6) are thicker, optimized for high-performance applications (Figure 2.1 (a)).

Figure 2.1 (b) illustrates the cross-section of an HBT. The active transistor region lies beneath the emitter contact, and the SiGe base is laterally connected using salicided polysilicon. [30].

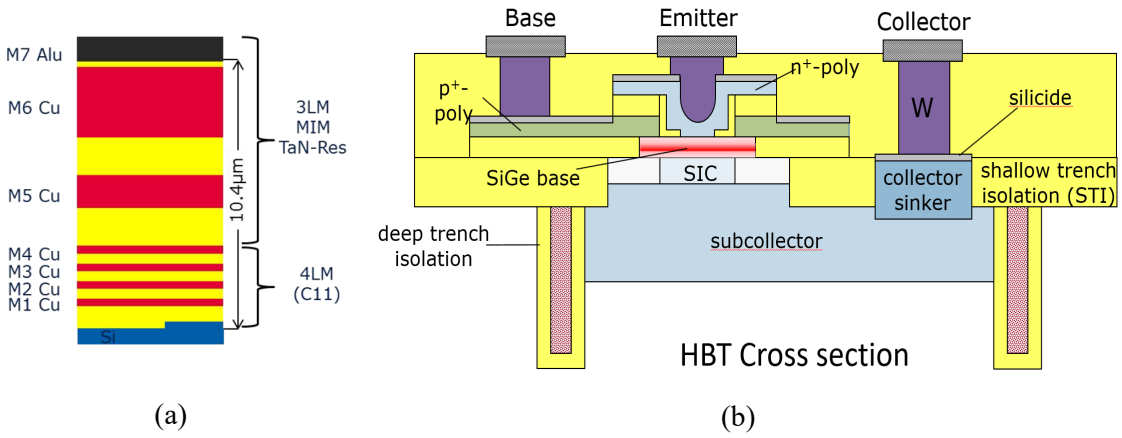


Figure 2.1: (a) 7-layer metallization (b) Cross section for an NPN transistor [30].

The process features advanced device structures designed to meet a wide range of application requirements. With an emitter mask size of 0.22 × 2.8 µm², these transistors achieve outstanding frequency performance.

- High-Speed NPN Transistors: Designed for ultra-fast operation with a cutoff frequency (f_T) of up to 250 GHz and a maximum oscillation frequency (f_{max}) of 370 GHz.

- Medium-Speed NPN Transistors: Offer a balanced performance with moderate frequency capabilities (f_T = 100 GHz) and higher breakdown voltages.
- High-Voltage NPN Transistors: Provide reliability in high-voltage environments with a breakdown voltage (BV_{CEO}) of up to 3.0 V.

2.2 Transconductance Mixer Fundamentals

2.2.1 Principle of Up-converted Transconductance Mixer

The transconductance mixer is a vital component in RF and microwave systems, primarily utilized for signal conversion in modern communication and sensing applications. This mixer operates on the principle of transconductance, where in an input intermediate frequency (IF) signal is converted into a radio frequency (RF) signal through the interaction with a local oscillator (LO). The fundamental theory behind the transconductance mixer has been thoroughly studied in earlier research [31], establishing it as a foundational technology.

In its most basic configuration, a fundamentally pumped transconductance mixer employs a transistor, typically biased to a voltage near its turn-on threshold (V_t). This precise biasing is critical to ensuring that the transistor generates an optimized transconductance waveform characterized by a 50% duty cycle. Such a duty cycle is significant because it enhances linearity and reduces distortion, ultimately influencing the mixer's conversion efficiency and dynamic range.

This section provides a detailed examination of the operational principles underpinning the transconductance mixer.

2.2.2 Circuit Description

The architecture of a single-ended transconductance mixer is illustrated in Figure 2.2. The circuit comprises a single bipolar junction transistor (BJT) functioning as the core mixing element. The RF and LO signals are combined via low-pass and high-pass filters respectively. The resulting RF signal is then extracted from the transistor's collector.

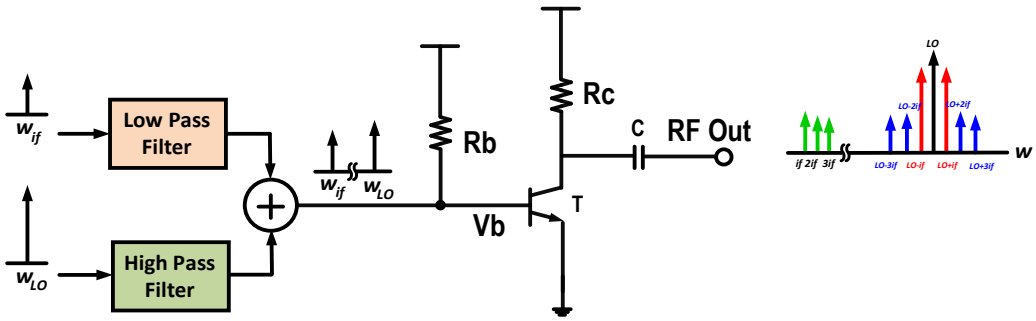


Figure 2.2: Circuit schematic of a single-ended transconductance mixer.

In this configuration, the transistor performs as a transconductance device. It converts the voltage signal applied at its base into a proportional current signal at the collector. The circuit's efficiency in achieving signal conversion depends heavily on selecting the right components and setting optimal biasing conditions.

2.2.3 Small-Signal Equivalent Circuit

The small-signal equivalent circuit of the transconductance mixer is depicted in Figure 2.3, offering a simplified representation of its behavior.

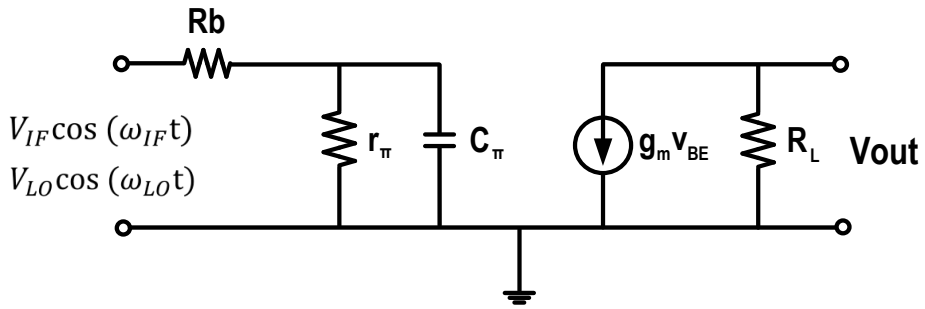


Figure 2.3: Simplified small-signal equivalent circuit of a bipolar transconductance mixer.

Consider an idealized transistor switching behavior, where its transconductance (g_m) operates as depicted in Figure 2.4 (a). When a large LO signal swing is applied, the transistor's transconductance transitions into a switched waveform, as illustrated in Figure 2.4 (b). This waveform exhibits a duty cycle of α, representing the fraction of time the transistor remains active within a given cycle. By expressing the g_m waveform in terms of its Fourier series expansion, it can be mathematically formulated as:

$$g_m = g_0 + \sum_{n=1}^{\infty} g_n \cos(n\omega_{LO}t) \tag{2.1}$$

Where:

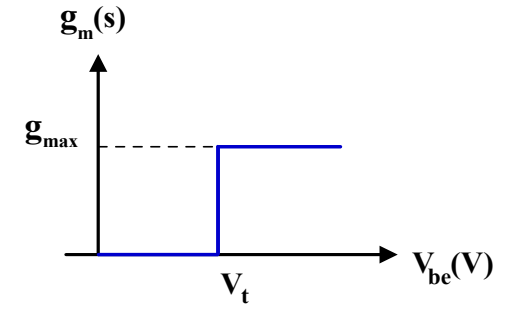
- g_0 represents the average transconductance over one period of the LO signal.
- g_n represents the nth harmonic of the transconductance waveform.

The Fourier coefficients are given by:

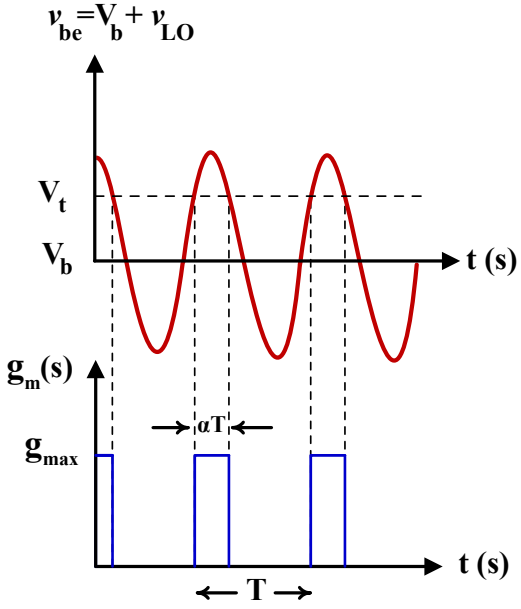
$$g_0 = g_{max} \cdot \alpha \tag{2.2}$$

$$g_n = \frac{2g_{max}}{n\pi} \cdot \sin(n\pi\alpha) \tag{2.3}$$

These coefficients indicate the contribution of each harmonic to the overall waveform.



(a)



(b)

Figure 2.4: (a) Transconductance of an ideal transistor. (b) Transconductance waveform [32].

The collector current (i_c) is determined by the product of the transconductance (g_m) and the IF voltage signal (v_{IF}):

$$i_c = g_m \times v_{IF}$$

$$= g_0 \cdot \frac{V_{IF}\cos(\omega_{IF}t)}{2\omega_{IF}C_\pi r_b} + \sum_{n=1}^{\infty} g_n \cos(n\omega_{LO}t)\frac{V_{IF}\cos(\omega_{IF}t)}{2\omega_{IF}C_\pi r_b}$$

$$= g_0 \cdot \frac{V_{IF}\cos(\omega_{IF}t)}{2\omega_{IF}C_\pi r_b}$$

$$+ \frac{V_{IF}}{4\omega_{IF}C_\pi r_b}\sum_{n=1}^{\infty} g_n \cos[(n\omega_{LO} - \omega_{IF})t]$$

$$+ \frac{V_{IF}}{4\omega_{IF}C_\pi r_b}\sum_{n=1}^{\infty} g_n \cos[(n\omega_{LO} + \omega_{IF})t] \quad (2.4)$$

Substituting the expressions for g_m and v_{IF}, i_c can be expanded into terms involving the RF signal and the harmonics of the LO signal. This expanded expression highlights the interaction between the LO and IF signals, leading to the generation of an RF signal at the output.

The presence of harmonics in g_m allows for mixing at multiple frequencies, enabling sub-harmonic mixing modes.

It is also important to note that the base-collector capacitance (C_π) is time-varying due to its voltage dependence; however, for the sake of analytical simplicity, this variation is neglected in the current analysis.

Key Insights and Design Implications

1. Optimal Biasing: The base bias voltage (V_b) plays a pivotal role in shaping the duty cycle (α) of the transconductance waveform. Adjusting V_b enables precise control over harmonic content, allowing designers to fine-tune the mixer's conversion gain and efficiency.
2. Harmonic Mixing: The Fourier coefficients (g_n) reveal the relative strength of various harmonic mixing modes. While the fundamental harmonic (g_0) is most significant, higher-order harmonics can be leveraged for specific requirements, such as sub-harmonic or non-fundamental frequency translation.
3. Trade-offs: Achieving a higher duty cycle (α) increases the average transconductance (g_0), enhancing conversion efficiency. However, it simultaneously reduces the impact of higher harmonics, necessitating a careful balance based on the application's performance criteria.

By understanding these principles, engineers can design transconductance mixers tailored to specific operational needs. Whether in wireless communication networks, high-frequency radar systems, or advanced sensing technologies, the transconductance mixer continues to be a good candidate for use in modern electronics.

2.3 Chapter Summary

This chapter explores the evolution of semiconductor materials, emphasizing the transformative role of Silicon Germanium (SiGe) in high-frequency and high-precision applications. It highlights SiGe's advantages, such as high electron mobility, thermal stability, and compatibility with existing silicon processes, which make it indispensable for RF circuits, mmWave communication, and 5G/6G technologies. The integration of SiGe with BiCMOS technology enables cost-effective, high-performance system-on-chip solutions, exemplified by the 130 nm SiGe BiCMOS process from Infineon, which supports diverse applications from high-speed communication to power management.

The chapter also delves into the fundamentals of transconductance mixers, key components in RF systems that leverage optimized transconductance waveforms for efficient frequency conversion. Design insights into biasing, harmonic mixing, and

performance trade-offs provide a foundation for tailored applications in wireless communication, radar, and sensing systems.

Chapter 3

Innovative Mixer Architectures for D-Band Communication: Cascode and Darlington Pair Configurations

As the demand for higher data rates and bandwidth continues to grow, the development of efficient, high-performance mixers becomes critical for enabling next-generation communication technologies. This chapter explores two innovative mixer architectures cascode and Darlington pair configuration designed to address the challenges of high-frequency operation, including linearity, power, isolation, and power efficiency.

The cascode mixer employs a double-mixing technique within a balanced topology, providing notable improvements in output power and linearity, while also offering simpler architecture and reduced power consumption compared to the conventional Gilbert mixer.By incorporating transmission line networks to mitigate parasitic capacitances, this design ensures stable operation at high frequencies while maintaining a compact chip footprint. The Darlington pair based up-conversion mixer introduces a modified topology that leverages the high input impedance and gain of the Darlington pair configuration, enhancing both current gain and frequency response. This architecture is particularly well-suited for low-power and low-voltage applications, as it achieves efficient operation with minimal power consumption.

This work offers a detailed evaluation of these two mixer architectures, highlighting their design principles, operational mechanisms, and simulated performance. By comparing their strengths and trade-offs, valuable insights are provided for advancing mm-Wave circuit design.

The chapter is structured as follows: First, the design and functionality of the cascode mixer are discussed, highlighting its double-mixing technique and phase-aligned signal design. Next, the Darlington mixer is introduced, with a focus on its transistor-level amplification and the role of transmission lines in mitigating parasitic effects. Simulation results are presented to validate the performance of both architectures, demonstrating their potential for high-frequency applications. Finally, the chapter concludes with a summary of the key findings and their implications for future mmWave circuit design.

3.1 D-Band Cascode Up-Conversion Mixer Utilizing Double Mixing Technique

The proposed mixer employs a balanced cascode topology, a widely recognized architecture designed to enhance linearity, improve isolation, and optimize power handling. This configuration is particularly well-suited for high-performance frequency conversion applications, as it effectively minimizes distortion while maintaining a compact chip footprint. The mixer leverages the principles of double mixing through a two-stage architecture. In the first stage, common-emitter transistors perform the initial signal mixing, ensuring efficient conversion of input signals. The second stage, consisting of common-base transistors, executes the double mixing process, thereby amplifying the output RF signal while enhancing both linearity and gain. This structured approach significantly improves the overall performance and efficiency of the frequency conversion process.

3.1.1 Design and Functionality of the Mixer

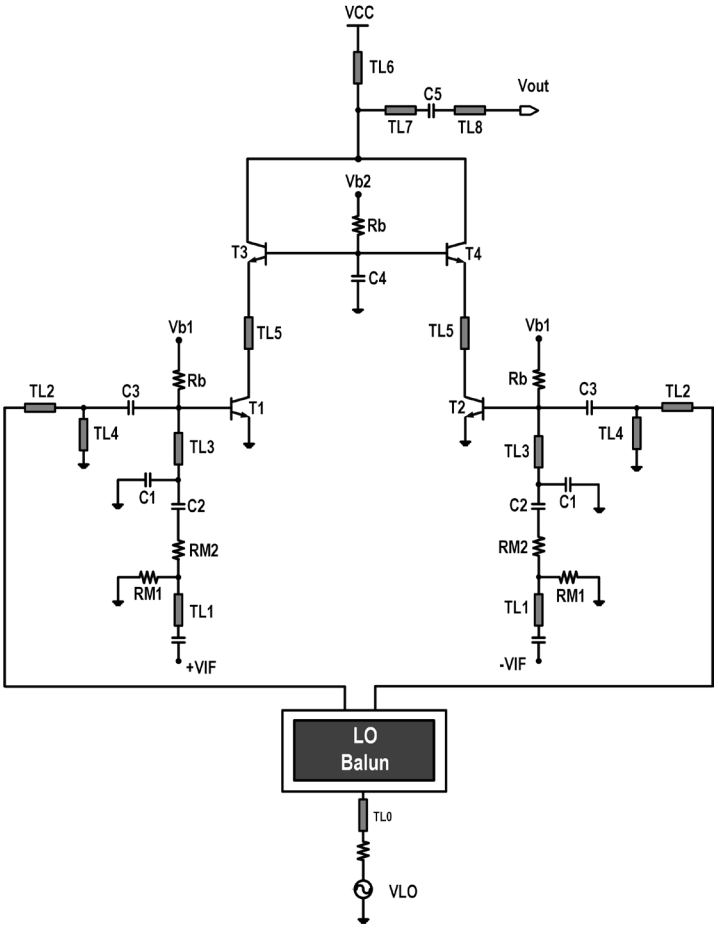
Figure 3.1(a) illustrates the schematic of the mixer, displaying the cascode structure formed by transistors T_1-T_4. Figure 3.1(b) provides a system-level view, emphasizing the flow of differential LO and IF signals through the mixer, and the isolation and impedance matching provided by carefully designed filters.

The operation of the mixer begins with the injection of the LO and IF signals into the bases of T_1 and T_2. These signals are routed through low-pass and high-pass filters, respectively. The low-pass filter isolates the LO signal, preventing high-frequency leakage to the IF port, while the high-pass filter ensures that only the desired IF signal reaches the transistors. This signal separation is critical for maintaining isolation between ports, reducing interference, and achieving efficient frequency conversion.

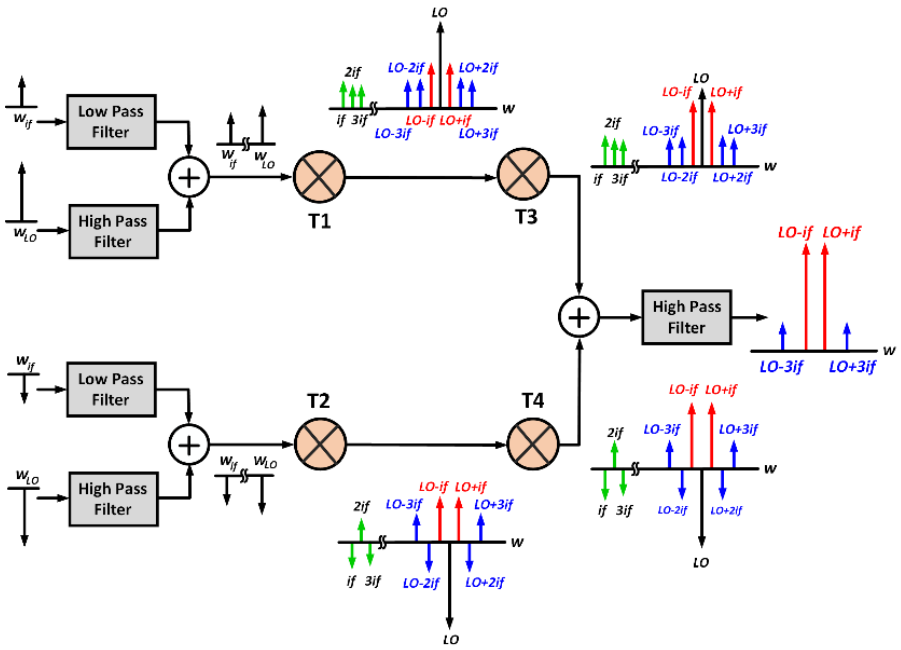
The input transistors, T_1 and T_2, are configured in a common-emitter topology. Here, the LO signal modulates the transconductance of the transistors, creating a spectrum of mixed signals at their collectors. This spectrum includes not only the desired RF signal but also harmonic and intermodulation components as shown in Figure 3.1(b).

The produced signals are fed into T_3 and T_4, where the double mixing technique further combines the LO and IF signals generated in T_1 (T_2) to produce fundamental RF signals. This enhances both linearity and output power. T_3 and T_4 not only amplify the RF signals at the output through mixing but also improve input-output isolation.

To ensure a low impedance for the IF signal at the emitter of T_3 (T_4), the bases of T_3 and T_4 are connected. Because the IF signals in T_3 and T_4 are in opposite phases, the base is virtually grounded. The RF signals at the emitter of T_3 (T_4) are in the same phase. Capacitor C_4 has been added to provide AC-grounding for the high-frequency RF common-mode signal. The design is biased for Class-B operation to achieve strong nonlinearity and low DC power consumption.



(a)



(b)

Figure 3.1: (a) Circuit diagram of the proposed cascode configuration up-converter (b) block diagram (system level) of the proposed technique.

To support the high data rates required in modern communication systems, the proposed mixer incorporates resistive matching networks (RM_1 and RM_2) at the IF ports. These networks ensure wideband impedance matching, enabling efficient signal transfer across a broad frequency range.

The proposed design carefully exploits phase relationships between the LO, IF, and RF signals to achieve high performance. At the input stage, the LO and IF signals are intentionally designed to be in opposite phases. In the output stage, the RF signals produced by T_3 and T_4 are added in phase, allowing their contributions to add constructively at the output. Conversely, unwanted signals such as the LO and IF components, as well as higher-order harmonics like $f_{LO}\pm2f_{IF}$ and $f_{LO}\pm4f_{IF}$, are suppressed due to their opposite phases. This phase-driven suppression mechanism eliminates the need for complex filtering at the output and simplifies the overall design as illustrated in Figure 3.1(b).

Parasitic capacitances pose a significant challenge in high-frequency circuit design, as they can degrade the performance of critical parameters such as gain, bandwidth, and stability. In the proposed mixer, these parasitics arise mainly from the inherent capacitances of the cascode transistors. To address this issue, the design incorporates a transmission line, TL_5, between T_1 and T_3 (and similarly between T_2 and T_4). This transmission line, in combination with the parasitic capacitances, forms a π-network for effectively mitigating parasitic capacitance effects and improving the mixer's stability.

3.1.1.1 The Role of Double Mixing in Performance Enhancement

The double mixing technique is a core innovation of the proposed design, enabling significant improvements in both output power and linearity. In conventional mixers, the RF signal is primarily generated at the first mixing stage, with limited opportunities for enhancement. However, the proposed mixer introduces a second mixing stage in T_3/T_4, where the LO and IF signals undergo additional interaction. This process amplifies the RF signal while maintaining its phase alignment, resulting in a doubling of the RF current at the output. This part focuses on evaluating the contribution of the cascode transistors T_3 (T_4) to the overall mixing process by systematically examining their performance under various conditions.

3.1.1.2 Mathematical Analysis of the cascode configuration employing a double mixing technique

In this section, a mathematical analysis of the cascode structure is presented when it is employed in a transconductance mixer utilizing a double mixing technique.

Figure 3.2 illustrates the small-signal equivalent circuit of the transconductance mixer with the cascode structure, providing a simplified representation of its behavior.

Consider an idealized transistor switching behavior, where its transconductance (g_m) operates as depicted in Figure 2.4 (a). When a large LO signal swing is applied, the

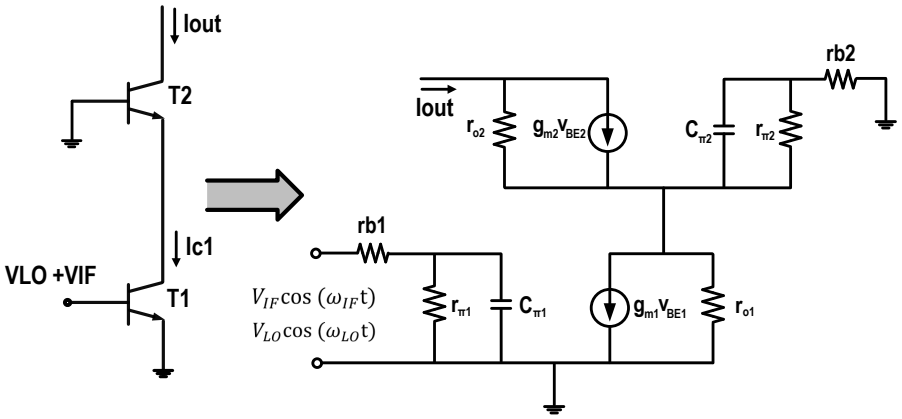


Figure 3.2: Simplified small-signal equivalent circuit of a bipolar transconductance mixer with the cascode structure.

transistor's transconductance transitions into a switched waveform, as illustrated in Figure 2.4 (b). This waveform exhibits a duty cycle of α, representing the fraction of time the transistor remains active within a given cycle. By expressing the g_m waveform in terms of its Fourier series expansion, it can be mathematically formulated as:

$$g_{mi} = g_{0i} + \sum_{n=1}^{\infty} g_{ni}\cos(n\omega_{LO}\mathrm{t}). \quad \mathrm{i} = 1{,}2 \tag{3.1}$$

Where *i* equal to 1 and 2 represent transistor T_1 and T_2, respectively.
g_0 denotes the average transconductance over one LO period, while g_n represents the nth harmonic of the transconductance waveform. The Fourier coefficients are given by:

$$g_0 = g_{max} \cdot \alpha \tag{3.2}$$

$$g_n = \frac{2g_{max}}{\mathrm{n}\pi} \cdot \sin(\mathrm{n}\pi\alpha). \tag{3.3}$$

These coefficients indicate the contribution of each harmonic to the overall waveform.

The collector current (i_{c1}) is determined by the product of the transconductance (g_m) and the IF voltage signal (V_{IF}). Substituting the expressions for g_m and v_{IF}, i_c can be expanded into terms involving the RF signal and the harmonics of the LO signal. This expanded expression highlights the interaction between the LO and IF signals, leading to the generation of an RF signal at the output.

$$\begin{aligned} i_{c1} &= g_{m1} \times v_{IF} \\ &= g_{01} \cdot \frac{V_{LO}\cos(\omega_{LO}\mathrm{t})}{2\omega_{LO}C_{\pi1}r_{b1}} + g_{01} \cdot \frac{V_{IF}\cos(\omega_{IF}\mathrm{t})}{2\omega_{IF}C_{\pi1}r_{b1}} \\ &+ \frac{g_{11} \cdot V_{IF}}{4\omega_{IF}C_{\pi1}r_{b1}}\cos(\omega_{LO} - \omega_{IF})t \\ &+ \frac{g_{11} \cdot V_{IF}}{4\omega_{IF}C_{\pi1}r_{b1}}\cos(\omega_{LO} + \omega_{IF})t \\ &+ \ldots \end{aligned} \tag{3.4}$$

By applying the same analytical process to the transconductance g_{m2} of transistor T_2, the output current expression can be derived.

The first term in (3.5) represents the RF current contribution from T_1, which is influenced by the product $(g_{02}g_{11})$. Since T_2 is configured in a common-base topology, its current gain remains close to unity. Consequently, the RF current generated by T_1 is efficiently transferred to T_2. This can also be verified mathematically, as the term $g_{02} \cdot r_{\pi 2}/(1 + j\omega_{IF}C_{\pi 2}r_{\pi 2})$ is approximately equal to one. The second term, (g_{12}), accounts for the contribution from T_2, highlighting its role in the overall mixing process.

$$i_{out} = \frac{(g_{02}g_{11} + g_{12}) \cdot V_{IF}r_{\pi 2}}{4\omega_{IF}C_{\pi 1}r_{b1}(1 + j\omega_{IF}C_{\pi 2}r_{\pi 2})}\cos(\omega_{LO} \pm \omega_{IF})t. \tag{3.5}$$

3.1.1.3 Simulation Configurations and Observations

To validate the contribution of T_3 and T_4 to the mixing process, harmonic balance simulations were performed under two scenarios: with and without the mixing function of T_3 and T_4 enabled. In the first scenario, an ideal band-pass filter was applied to isolate the low-frequency IF components from the output of T_1 and T_2. This isolation effectively disabled the mixing function of T_3 and T_4. The system-level and circuit diagrams are illustrated in Figure 3.3 (a) and Figure 3.3 (b). In the second scenario, the filter was removed, allowing T_3 and T_4 to participate fully in the mixing process.

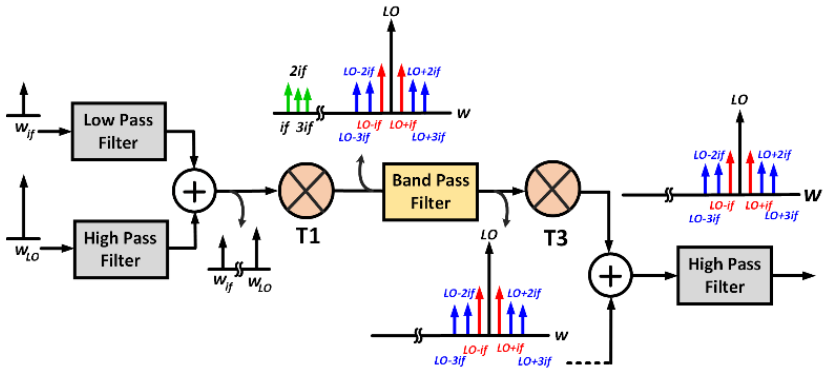
Case Study: With Filtering

An ideal band-pass filter is added at the output of T_1 (T_2) to remove only the low-frequency IF components. After filtering out the IF signal, T_3 and T_4 no longer perform their mixing functionality, and the fundamental RF signal is generated solely by T_1 and T_2. In this case, T_3 and T_4 function as amplifiers configured in a common-base arrangement.

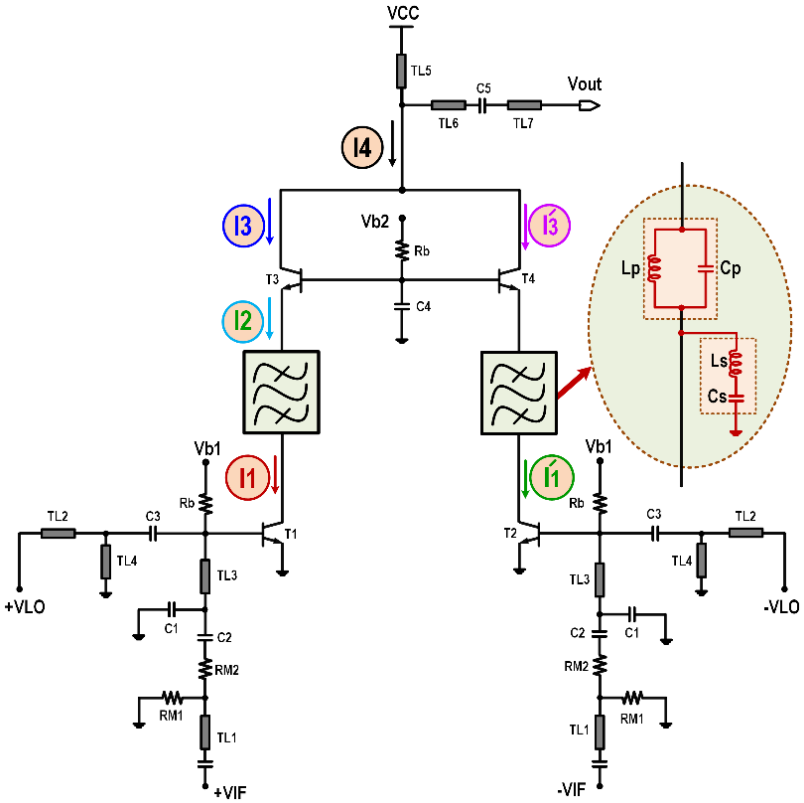
Figure 3.4 shows the harmonic balance simulation results for the mixer configurations with the filter. These simulations are based on an LO signal with a frequency of 140 GHz and a power of 0 dBm, and an IF signal with a frequency of 1 GHz and a power of –10 dBm.

The generated harmonics include f_{IF} (1 GHz), f_{LO} (140 GHz), $f_{LO} \pm f_{IF}$ (139 GHz/141 GHz), $2f_{IF}$ (2 GHz), $f_{LO} \pm 2f_{IF}$ (138 GHz/142 GHz), and $f_{LO} \pm 3f_{IF}$ (137 GHz/143 GHz). In the figures, red and blue colors represent the current spectrum at the outputs of T_1 (T_2) and T_3 (T_4), respectively.

As shown in Figure 3.4, incorporating the filter to eliminate low frequency IF components from the collector current of T_1, I_1, the mixing functionality of T_3 is disabled. However, the ideal band-pass filter does not disturb the LO and RF signals, as the magnitudes of the LO and RF inputs to T_3 (I_2) remain unchanged. The RF signal at the output of T_3 (I_3) closely matches that of T_1 (I_1) due to the near-unity current gain provided by the common-base configuration of T_3.



(a)



(b)

Figure 3.3: (a) Block diagram (system level) (b) circuit diagram of the cascode configuration up-converter with the deal band-pass filter.

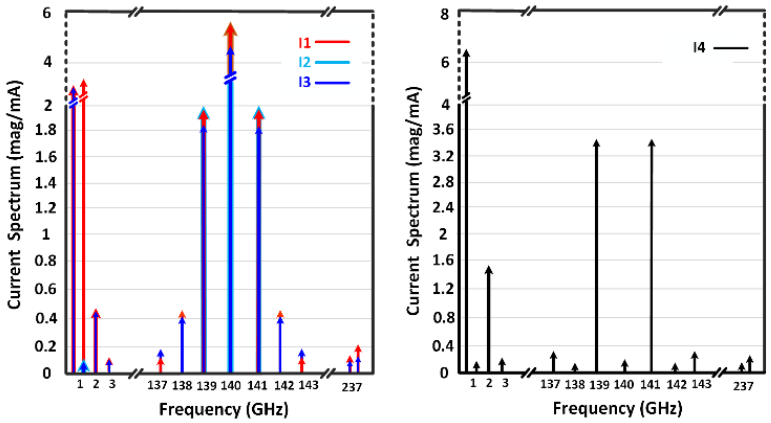
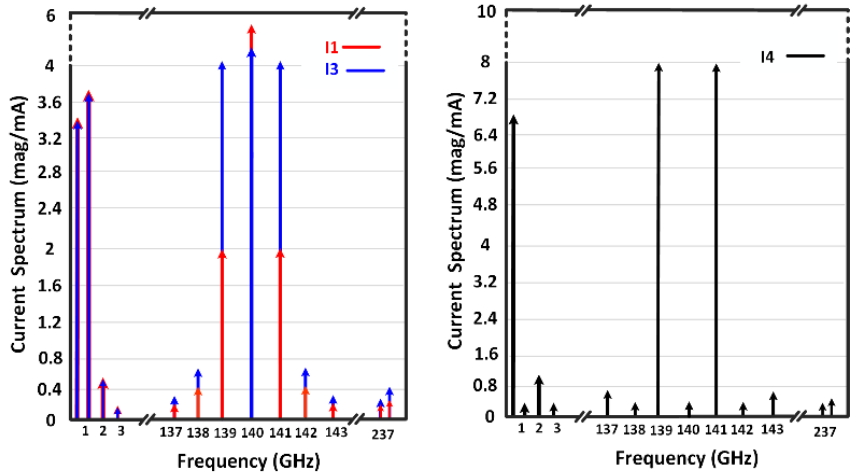


Figure 3.4: Simulated spectrum of the mixer currents magnitude with the ideal band-pass filter.

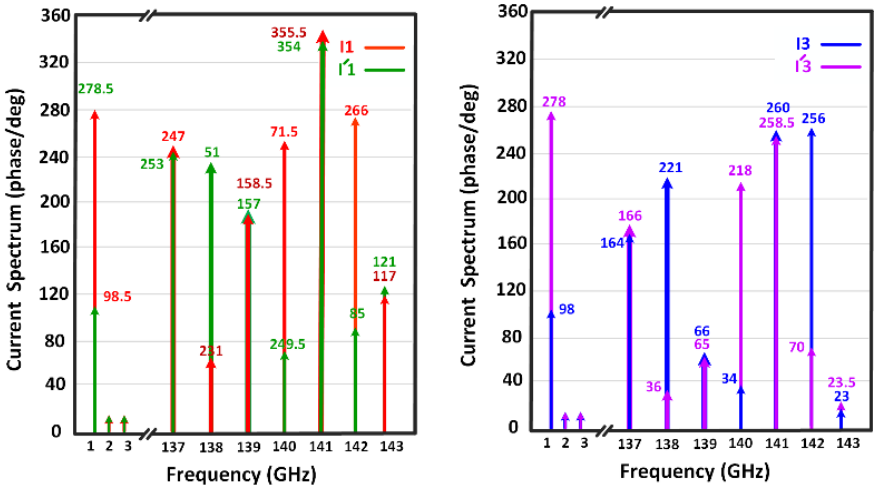
Case Study: Without Filtering

As shown in Figure 3.5 (a), removing the filter allows the IF signal at the output of T_1 to mix with the LO, generating an additional RF signal. The RF current at the output of T3 is approximately double that of T_1. This increase in RF current is a direct outcome of the double mixing technique, where T_3 and T_4 enhance the mixing process, leading to improved output power.

Figure 3.5(b) illustrates the current phases in T_1, T_2, and T_3, T_4. As previously noted, the LO (140 GHz) and IF (1 GHz) currents generated in T_1 and T_2 are in opposite phases, while the RF signals (139 GHz/141 GHz) are in the same phase. When these signals are applied to transistors T_3 and T_4, the additional RF signals produced by T_3 and T_4 also remain in phase since the LO and IF signals are in opposite phases. As the outputs of T_3 and $_{T4}$ are combined, the magnitude of the RF signal I_4 (139 GHz/141 GHz) and IM_3 (137 GHz/143 GHz) doubles due to their in-phase alignment. Conversely, the LO (140 GHz) and IM_2 (138 GHz/142 GHz) signals are canceled out as they are in opposite phases.



(a)



(b)

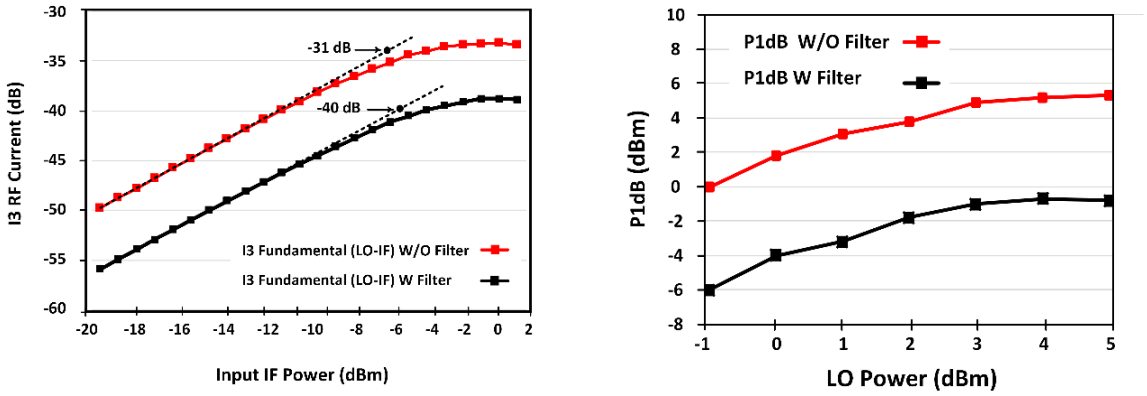
Figure 3.5: Simulated spectrum of the mixer current's (a) magnitude (b) phase without the ideal band-pass filter.

Gain and Linearity Characteristics

To assess the linearity of the proposed double mixing technique, Figure 3.6 (a) shows the fundamental output currents at transistors T_3 and T_4 (denoted as I_3/I_4) as functions of the input intermediate frequency (IF) power. Simulations are presented for both filtered and unfiltered IF currents, enabling a detailed comparison. The vertical axis is plotted on a logarithmic scale to highlight the 1dB compression point, a key indicator of linearity. The compression characteristics of the curves reveal that implementing the double mixing technique in the cascode circuit, without filtering the IF current, significantly boosts gain.

Notably, this gain enhancement does not introduce additional distortion, maintaining the mixer's high linearity. As a result, the double mixing technique not only increases the overall gain but also preserves excellent linearity, making it particularly effective for high-frequency linear applications.

Figure 3.6 (b) further illustrates the P_{1dB} as a function of LO power. Incorporating the low-pass filter leads to a reduction of approximately 6 dB in the output refereed P_{1dB}.



(a) (b)

Figure 3.6: (a) T_3 Fundamental RF currents (I_3) magnitude with and without filter versus input IF power. (b) Mixer's P_{1dB} with and without filter versus LO power.

3.2 Modified Darlington Mixer for High-Frequency Applications

The Darlington pair is composed of two bipolar junction transistors (BJTs) connected in series, where the signal, generated by the first transistor, is further amplified by the second transistor. This cascaded structure enhances the conversion gain compared to a single transistor, making it a preferred topology for applications requiring high amplification and improved signal integrity. Due to its ability to boost gain and optimize frequency response, the Darlington pair is widely employed in high-frequency circuits.

The proposed up-conversion mixer, illustrated in Figure 3.7, features a modified Darlington pair topology that incorporates a conventional Darlington pair along with a small series transmission line (TL_5) where RF signal generated by mixing LO and IF signals at the first transistor (T_1) is amplified further by the second transistor (T_2). The

transmission line plays a crucial role in mitigating parasitic capacitance at the base of T_2/T_4 and the emitter of T_1/T_3. By compensating for these parasitic effects, the mixer achieves an enhanced frequency response, making the Darlington pair more effective for broadband signal processing.

In the proposed design, the differential LO and IF signals are applied to the bases of transistors T_1 and T_2. To ensure proper impedance matching and signal isolation, the LO signal is routed through a low-pass filter, while the IF signal passes through a high-pass filter. These filtering networks function similarly to those used in the cascode up-conversion mixer, effectively minimizing signal interference and optimizing the impedance characteristics of the circuit. The transistors, T_1/T_2, operate in Class-B mode, which provides high nonlinearity while maintaining low DC power consumption.

Within the mixer, the LO signal modulates the transconductance of the transistors, generating an RF signal at the collector and emitter of T_1/T_2. This RF signal is then routed to the inputs of T_3/T_4, where it undergoes further amplification. The collector of T_1 is connected to the collector of T_3, allowing the RF signals from T_1 and T_3 to be combined and delivered to the output port.

Moreover, the design employs a balanced architecture to ensure superior port-to-port isolation. At the output nodes of T_1/T_3 and T_2/T_4, the RF signals remain in phase, whereas the LO and IF signals are 180° out of phase. This inherent phase cancellation effectively suppresses LO and IF leakage at the output, enhancing the overall signal purity of the mixer.

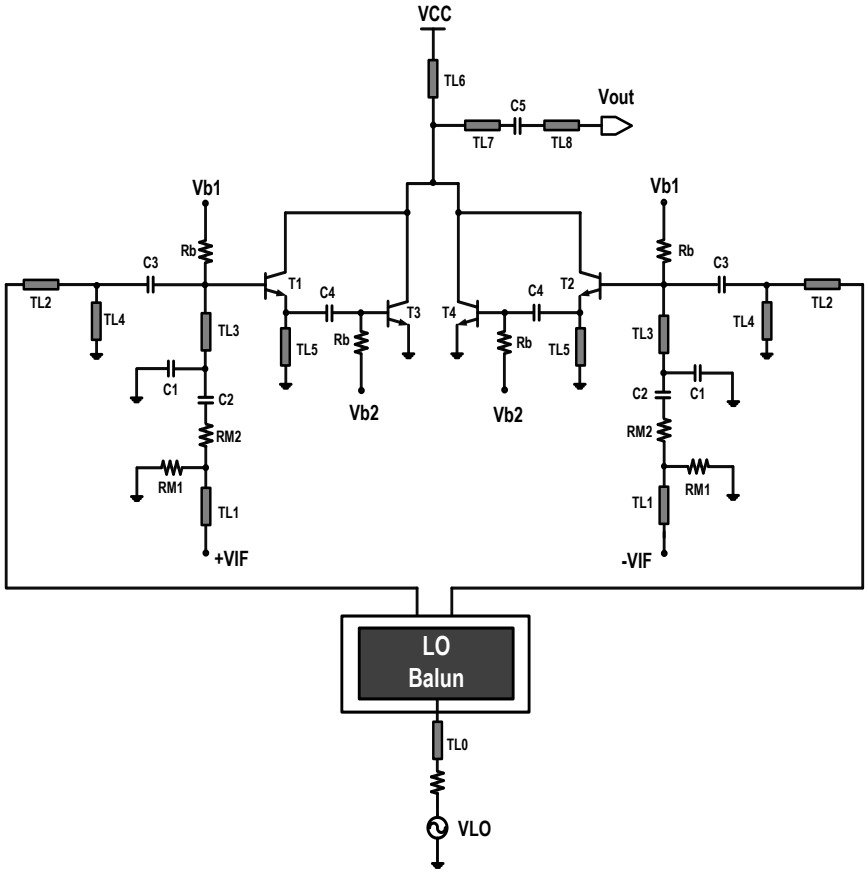


Figure 3.7: Circuit diagram of the proposed Darlington up-converter.

3.2.1 Effect of Transmission Line on Circuit Performance

To provide a comprehensive understanding of the transmission line's role (TL_5) in the circuit's overall performance, a series of simulations were conducted. The primary objective was to evaluate how the transmission line mitigates parasitic effects, particularly those caused by the Miller capacitance, which is known to degrade high-frequency response. The results from these simulations indicate that the transmission line serves as an effective mechanism to counteract the parasitic influences. This mitigation is critical for maintaining a stable and efficient high-frequency operation.

One key aspect of this analysis was the effect of varying the transmission line length. Figure 3.8 illustrates this dependency, showing that longer transmission lines tend to introduce additional inductive effects. These effects, while beneficial in some contexts, lead to a narrowed bandwidth, which may not be ideal for applications requiring wideband performance.

Conversely, shorter transmission lines may fail to adequately neutralize the parasitic capacitance, leading to reduced conversion gain. This trade-off between gain and bandwidth underscores the importance of precise length selection. An optimal transmission line length ensures the best balance between these parameters, enabling stable circuit operation with enhanced performance. The optimization process highlights that achieving this balance is critical for meeting both gain and bandwidth requirements.

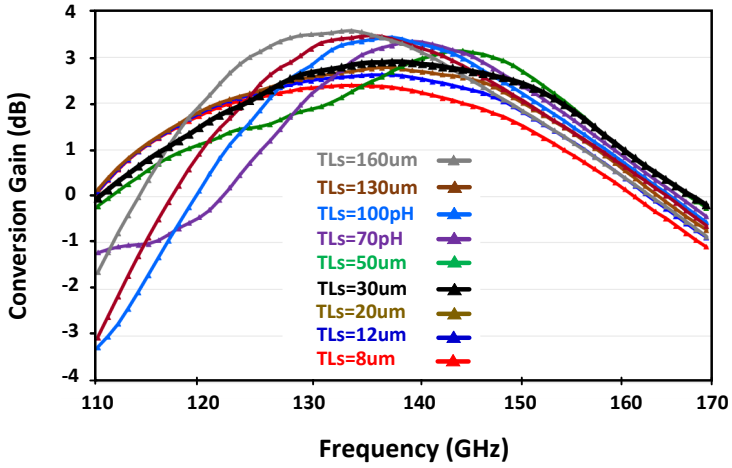


Figure 3.8: The conversion gain of the circuit versus LO frequency with different length of the transmission line (TL_5).

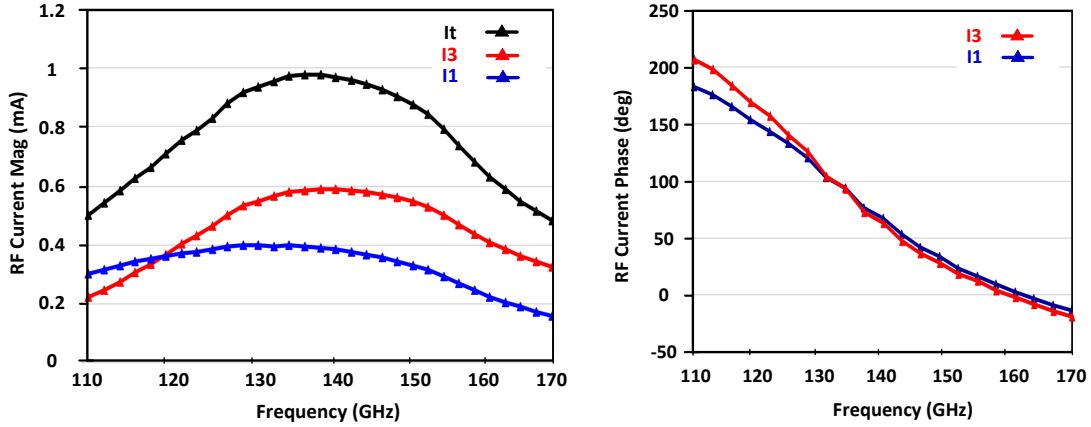
3.2.2 Role of Transistors in RF Current Generation

The contribution of transistors T_1 and T_2 to the generation of the output RF current was also analyzed in detail, with results presented in Figure 3.9 and Figure 3.10. These figures demonstrate the relationship between the LO frequency, input power, and the resulting RF current.

Transistor-Level Analysis

Transistor T_1 primarily generates the initial RF current, which is subsequently amplified by transistor T_3. This amplification process is highly dependent on the phase relationship

between the two transistors, as shown in Figure 3.9 (a) and Figure 3.9 (b). The phase alignment ensures that the currents produced by T_1 (I_1) and T_3 (I_3) combine constructively at the output node. This constructive addition significantly enhances the output current, denoted as I_t, ($I_t = (I_1 + I_3)$), which is the cumulative contribution of both transistors.
The efficient phase alignment and current addition are pivotal for achieving a strong RF output and bandwidth, as any misalignment could lead to destructive interference, reducing the overall circuit efficiency.



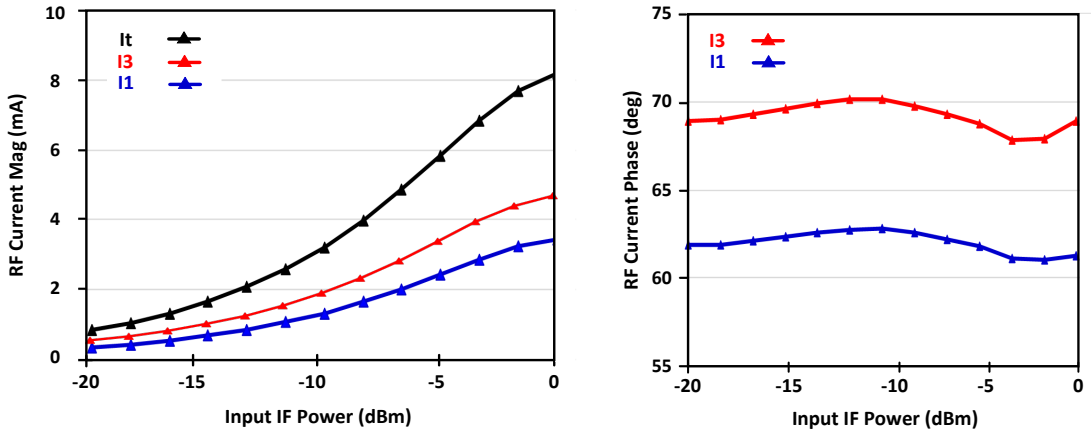
(a) (b)

Figure 3.9: Simulated RF currents I_1, I_3 and I_t versus f_{LO} (a) magnitude (b) phase at IF frequency 2 GHz, LO power 5 dBm.

Output RF Current as a Function of Input Power

Further analysis was conducted to examine the output RF current as a function of IF power. Figure 3.10 (a) and Figure 3.10 (b) present these results, confirming that the constructive current addition observed between T_1 and T_2 is consistent across varying levels of IF power when IF frequency is 2GHz and LO power is 5dBm.

This consistency in performance under different input conditions validates the robustness of the circuit design. The results highlight that the design not only achieves high output current levels but also maintains stability across a range of input power levels.



(a) (b)

Figure 3.10: Simulated RF currents I_1, I_3 and I_t versus P_{if}. (a) magnitude (b) phase at LO frequency 140 GHz, IF frequency 2 GHz, LO power 5 dBm.

3.3 Chapter Summary

This chapter presented two innovative mixer architectures, the cascode and Darlington pair configurations, designed for D-band (110–170 GHz) communication systems. These designs aim to address key challenges in high-frequency up-conversion, including linearity, power, isolation, power efficiency, and bandwidth.

The cascode mixer utilizes a balanced double-mixing topology, where the first stage (common-emitter transistors) performs initial signal conversion, while the second stage (common-base transistors) further enhances the RF signal by double mixing, improving both gain and linearity. The integration of transmission lines and parasitic capacitances to form low pass filters, ensuring better frequency response and stability. Additionally, the mixer's single-balanced design effectively cancels LO and IF leakage at the output, enhancing signal purity without requiring complex filtering. Harmonic balance simulations confirmed that the double mixing technique significantly boosts output power and compression characteristics (P_{1dB}).

The Darlington pair mixer, on the other hand, employs two- transistors, where the first transistor generates the RF signal, and the second transistor amplifies it. A short transmission line (TL_5) is introduced to counteract Miller capacitance effects, improving frequency response and bandwidth. This configuration is well-suited for low-power and low-voltage applications, as it achieves higher efficiency while maintaining competitive performance. Simulation results demonstrated that the transistor phase alignment plays a crucial role in constructive RF current addition, maximizing output power

Chapter 4

Measurement Results

The fabrication, measurement setup, and performance evaluation of the proposed cascode and Darlington up-conversion mixers are presented, focusing on addressing the challenges of high-frequency operation while ensuring low power consumption and a compact chip area. Using the 130-nm SiGe HBT B11HFC process technology, the mixers were designed and optimized for minimal parasitics and interconnect lengths, resulting in a remarkably compact core area. The measurement setup, carefully designed to evaluate key performance metrics such as conversion gain, output power, isolation, and DC power consumption, employed advanced calibration techniques to ensure accurate and reliable results.

The chapter is structured as follows: First, the fabrication process and chip layout are discussed, highlighting the compact design and key parameters of the mixers. Next, the measurement setup is described in detail, including the calibration procedures and equipment used. The subsequent sections present the measured performance results, including conversion gain, linearity, isolation, and power consumption, with comparisons to simulation data. Finally, the performance of the proposed mixers is benchmarked against state-of-the-art designs, demonstrating their competitive figures of merit and validating their potential for use in future D-band communication systems.

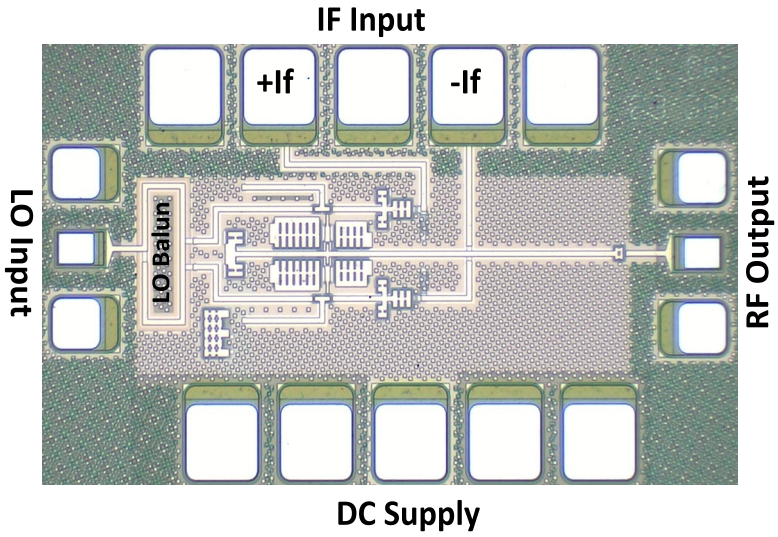
4.1 Fabrication and Chip Layout

The proposed up-conversion mixers were fabricated using the B11HFC 130-nm SiGe HBT process technology provided by Infineon Technologies AG. The chip micrograph of the cascode and Darlington up-conversion mixers are provided in Figure 4.1 (a) and Figure 4.1 (b), respectively. The total chip area, including the LO balun and all bonding pads, for cascode and Darlington up-conversion mixers measures 620 × 360 μm² and 600 × 430 μm², respectively. The core of the mixers, excluding pads, is remarkably compact, occupying just 410 × 180 μm² and 350 × 252 μm², respectively. This compact layout is achieved through careful optimization of the circuit and meticulous arrangement of components.

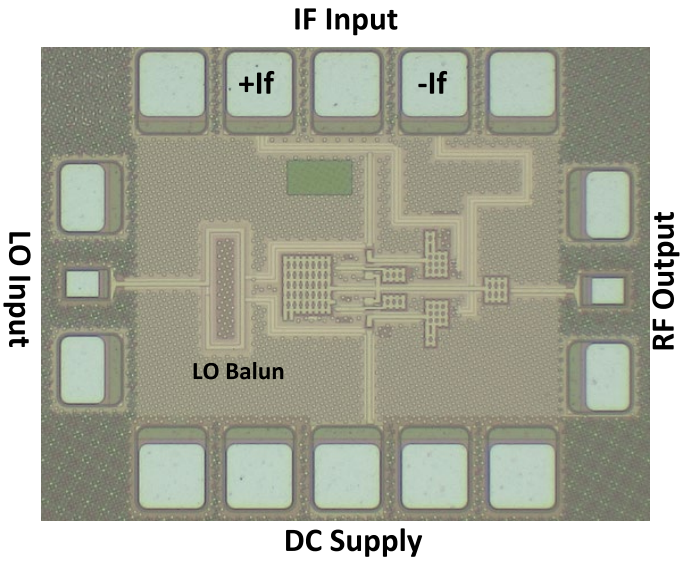
The layout of the mixer is designed to maintain symmetry in the differential structure, except for the IF transmission line parts. The lengths of the IF transmission lines are

identical to ensure balanced signal paths, and the perpendicular placement of the differential IF lines relative to the RF output trace was chosen to minimize coupling and interference between the IF and RF signals. Since the IF signal operates at a much lower frequency compared to the RF and LO signals, its perpendicular placement does not significantly affect the symmetry or performance of the differential structure. The low-frequency nature of the IF signal means that any minor asymmetry in the IF transmission lines has a negligible impact on the overall mixer performance. Additionally, the layout ensures that the critical high-frequency paths (LO and RF) remain symmetric and optimized for performance. The LO and RF traces are carefully routed to maintain equal lengths and minimize parasitic effects, which is crucial for maintaining the balance of the differential structure at high frequencies.

The key design parameters, including the dimensions of the transmission lines and capacitors, are summarized in Table I, highlighting the specific active and passive components used in both designs.



(a)



(b)

Figure 4.1: Chip micrograph (a) Cascode and (b) Darlington pair mixer.

TABLE I
ACTIVE AND PASSIVE COMPONENTS VALUES

	TL*	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8
Cascode	**Length (µm)**	206	152	47	98	14	80	290	38
Darlington	**Length (µm)**	206	150	60	100	30	69	110	73

*Width (µm): 4.9

	Cap	C1	C2	C3	C4	C5
Cascode	**Capacitance (fF)**	120	320	26	3000	70
Darlington	**Capacitance (fF)**	180	570	36	350	630

	Transistor	T1/T2	T3/T4
Cascode	**Emitter Length (µm)**	18*	15*
Darlington	**Emitter Length (µm)**	9**	10**

*Number of fingers:2 **Number of fingers:1

4.2 Measurement Setup

To validate the performance of the mixer, a measurement setup was established, as shown in Figure 4.2 The setup was designed to evaluate the mixer's conversion gain (*CG*), output power, isolation, and DC power consumption. The LO and RF signals were applied through dedicated extenders, while the IF signals and DC power supplies were delivered via separate probe pads. The LO signal, operating in the 110–170 GHz range, was generated using a VDI WR6.5 active multiplier chain (AMC), which multiplies a lower-frequency input signal to achieve the desired frequency. For higher LO power levels, a VDI WR6.5 SGX-M amplifier multiplier chain was employed, capable of delivering up to 10 dBm of output power.

The RF output signal was down-converted using an additional WR6.5 AMC to facilitate accurate power measurement. The IF signal calibration is performed using the Keysight U8488A Power Sensor (10 MHz–67 GHz) and the N4694A Electronic Calibration Module. An Erikson PM5 power meter is used to calibrate the power of the LO signals.

Losses due to cables, connectors, and probes were carefully measured and de-embedded from the final results to ensure the accuracy of the reported data. The on-wafer probing utilized three millimeter-wave probes. These probes were positioned at the top, left, and right of the chip to access the IF, LO, and RF ports, respectively. A ground-signal-ground (GSG) probe with a 75-µm pitch was employed for the RF and LO ports, while a GSGSG probe with a 100-µm pitch was utilized for the differential IF ports. This configuration ensured robust and reliable connections for all critical signals.

4.3 Conversion Gain and Linearity Performance

The conversion gain and output power characteristics of the mixer were measured under various operating conditions. Figure 4.3 illustrates the measured conversion gain and output power of both mixers as functions of the input IF signal power at an LO frequency

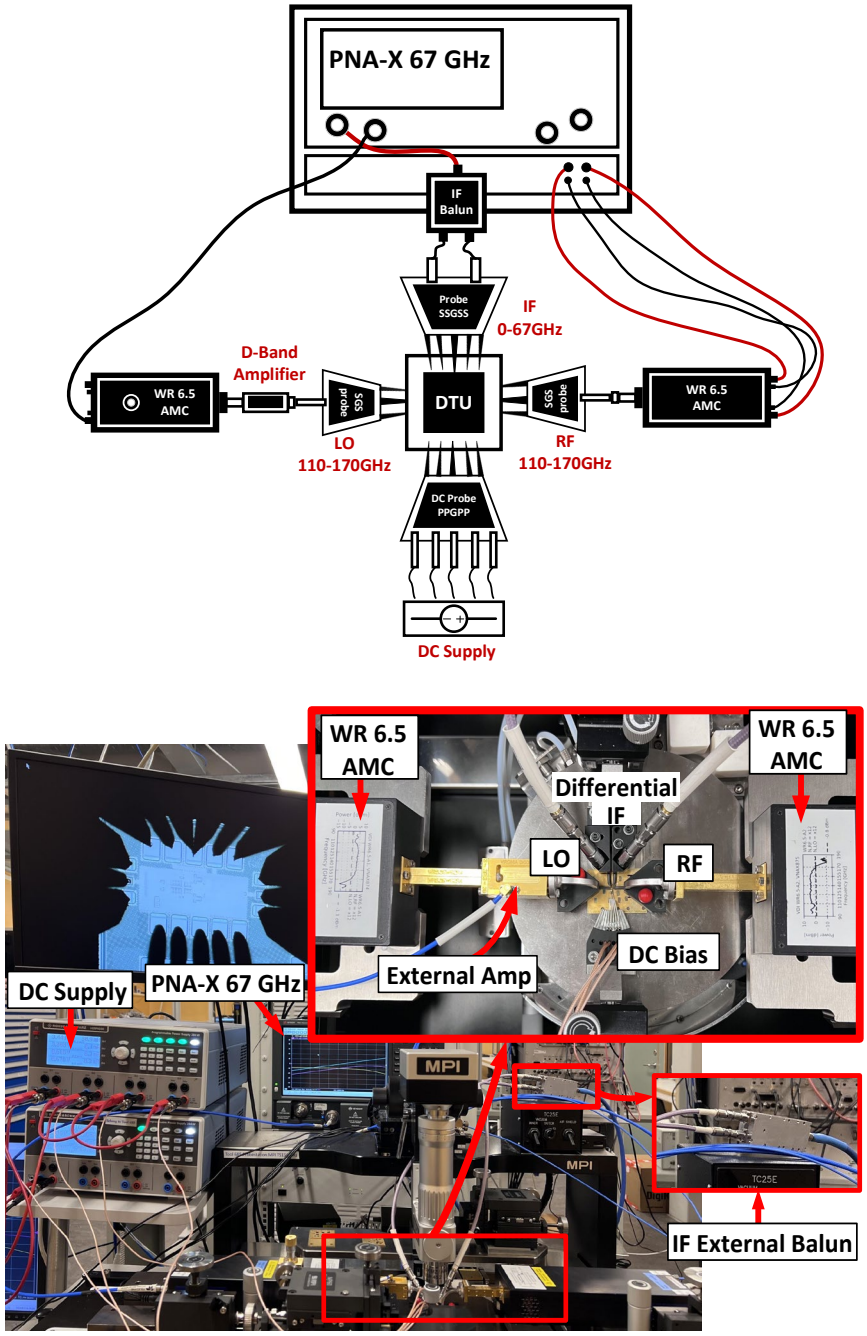


Figure 4.2: Measurement setup for CG and output power.

of 140 GHz and an IF frequency of 2 GHz. The cascode up-conversion mixer achieves a maximum conversion gain of 9.3 dB with a saturation output power (P_{sat}) of 5.4 dBm when driven with an LO power of 5 dBm. These results demonstrate the effectiveness of the mixer in maintaining high gain and output power across a range of input conditions. Simulation results included for comparison exhibit agreement with the measured data, validating the accuracy of the design and modeling process. Figure 4.3 (b) shows the result for the Darlington pair up-conversion mixer at an LO frequency of 138 GHz and an IF frequency of 2 GHz, with the LO power adjusted across different levels. The mixer

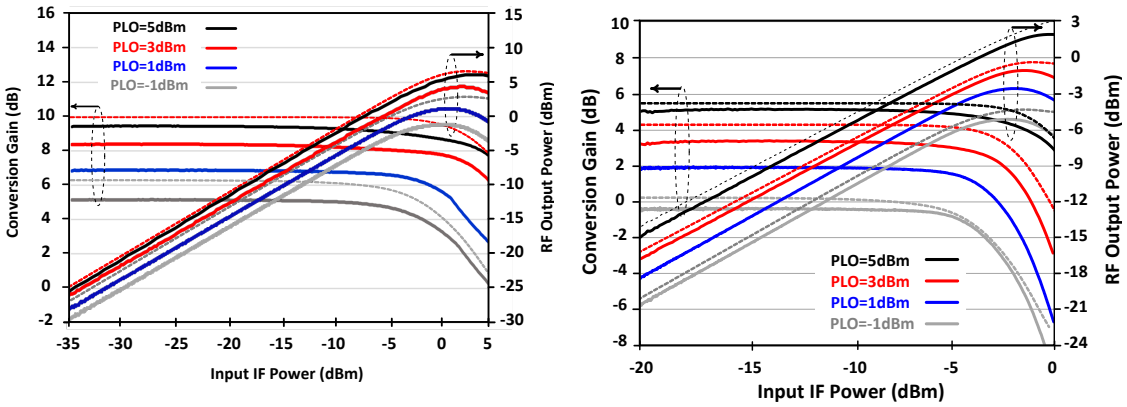


Figure 4.3: Measured conversion gain (*CG*) and output RF power versus input IF power with -1, 1, 3 and 5 dBm LO at 140 GHz. Simulated (dashed line) *CG* and output power are also included. (a) Cascode mixer - and (b) Darlington pair.

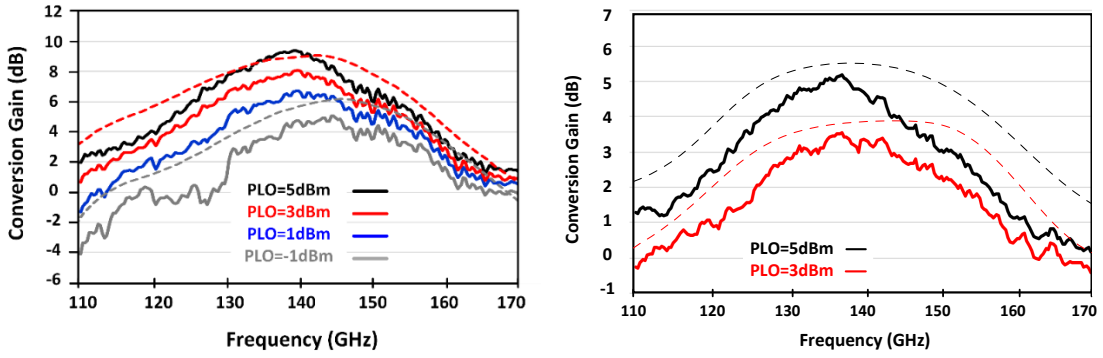


Figure 4.4: Measured *CG* versus LO frequency at an input IF frequency of 2 GHz and -20 dBm power. Simulated (dashed line) *CG* is also included. (a) Cascode mixer - and (b) Darlington pair.

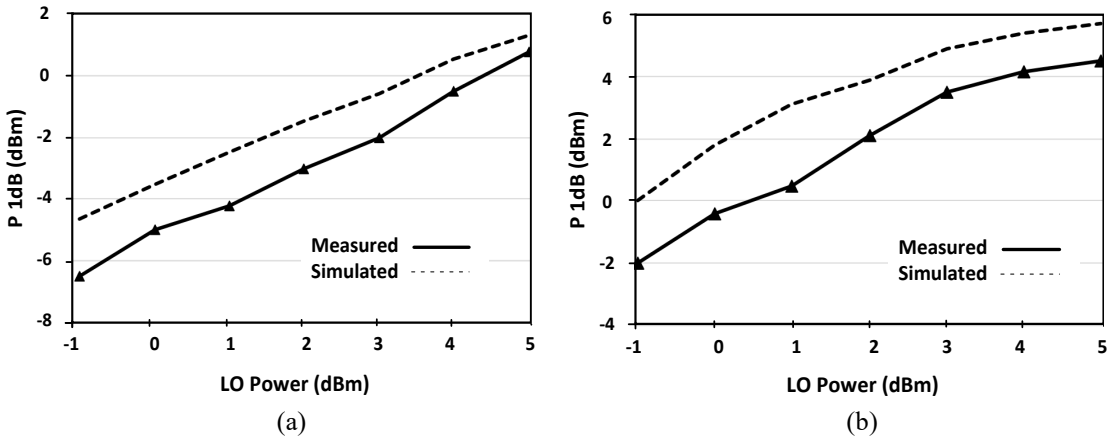


Figure 4.5: Measured and simulated OP_{1dB} versus LO power at LO frequency of 138 GHz and IF frequency of 2 GHz for (a) Cascode mixer - and (b) Darlington pair.

achieves a peak conversion gain of 2.1 dB and a saturation output power (P_{sat}) of 2.2 dBm when the LO power is set at 5 dBm.

In Figure 4.4, the graphs present both the simulated and measured results for conversion gain (*CG*) as a function of LO frequency, evaluated across various local oscillator (LO) power levels for cascode and Darlington pair mixer. The intermediate frequency (IF) is set at 2 GHz, with an input power level of -20 dBm. The data indicates that when the LO power is set to 5 dBm, the maximum measured conversion gain reaches 9.5 dB and 2.1 dB, peaking for cascode and Darlington pair mixer respectively.

Figures 4.5 (a) and Figure 4.5 (b) show measured/simulated OP_{1dB} of the mixer with LO power from -1 to 5 dBm. OP_{1dB} improved with higher LO power before the saturation of the mixer. This demonstrates that the linearity of the upconverters relies on the level of LO power as expected.

The OIP_3 measurement setup for the cascode mixer, shown in Figure 4.6 and the linearity of the mixer is examined in Figure 4.7. The measurement setup consists of an LO frequency source and two IF sources. It includes an R&S® FSWP Phase Noise Analyzer, which covers a frequency range of 1 MHz to 50 GHz (extends up to 325 GHz using external mixers) along with a D-band harmonic mixer for high-frequency measurements. Figure 4.7 shows the measurement results along with the simulation in a two-tone test procedure at a LO frequency of 140 GHz, the two IF tones at 2 GHz are spaced by 100 MHz. From this figure, an 8 dBm IIP_3 and a 15 dBm *OIP3* can be observed.

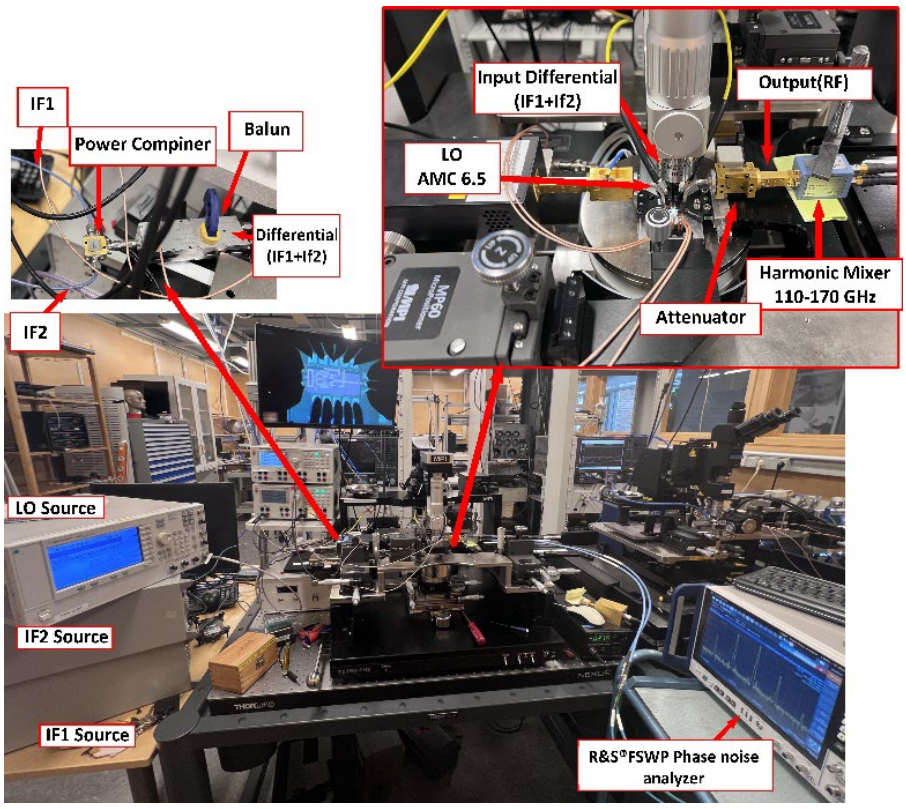


Figure 4.6: OIP_3 Measurement setup.

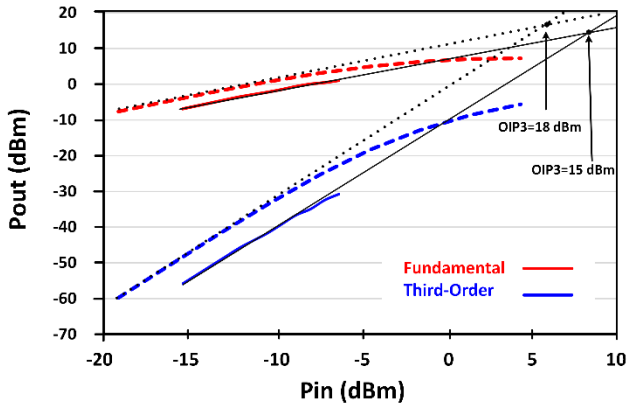


Figure 4.7: Measured fundamental and IM_3 tone output power versus input power of the proposed mixer at LO frequency of 140 GHz and IF frequency of 2 GHz with 100 MHz tones space. Simulation results (dashed line) are also included.

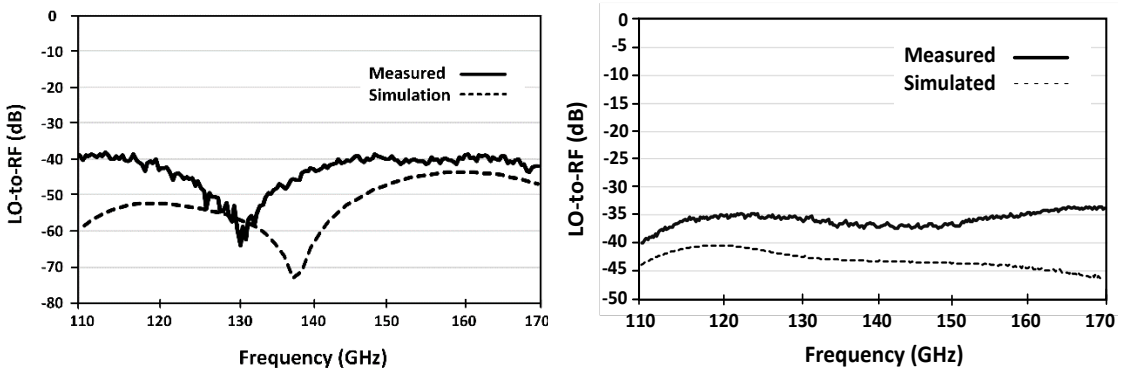
4.4 Isolation, Reflection Coefficients and power consumption

Port-to-port isolation is a key parameter in evaluating the performance of the mixer. Figures 4.8 (a) and Figures 4.8 (b) illustrate the measured isolation between the LO input and RF output ports for both the cascode and Darlington pair mixers.

For the cascode mixer, the transistor cascode configuration (T_1/T_2 and T_3/T_4), in conjunction with a balanced layout, effectively minimizes LO leakage and enhances isolation. The measured LO-to-RF isolation exceeds 38 dB across the operational bandwidth, ensuring minimal interference between ports. Additionally, LO leakage to the differential IF ports is negligible due to the incorporation of a low-pass filter at the IF outputs. For the Darlington pair mixer, the results shown in Figure 4.8 (b), confirm that from 110 GHz to 170 GHz, the LO-to-RF leakage remains greater than 34 dB. This performance is attributed to the mixer's balanced architecture, which effectively suppresses unwanted coupling and enhances isolation.

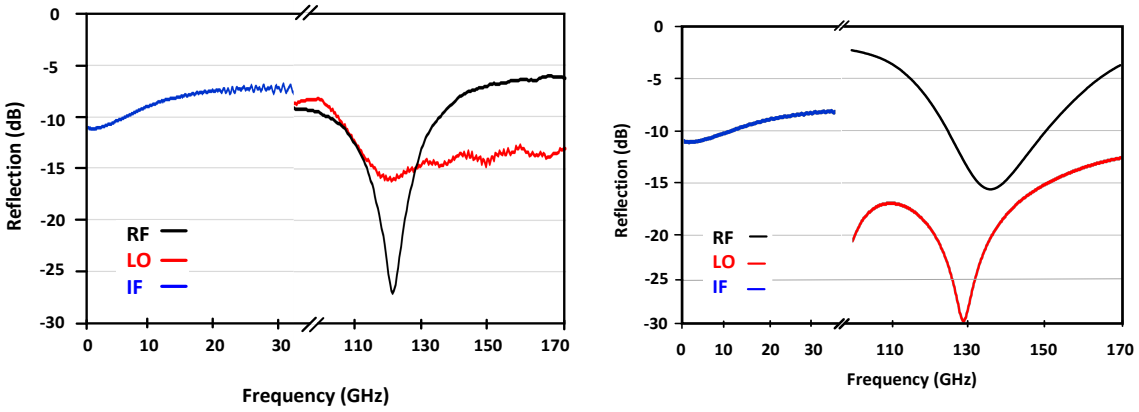
The reflection coefficients of the LO, RF, and IF ports were evaluated using a Keysight PNA-X N5247A with WR 6.5 extenders. The results, presented in Figure 4.9, demonstrate excellent impedance matching across all ports, which is essential for maximizing power transfer and minimizing signal reflections. These measurements validate the design's impedance matching strategy and confirm its effectiveness in real-world operating conditions.

The simulation and measurement results for the cascode mixer's total current drawn from a 3V DC supply at different LO power levels are presented in Figure 4.10 (a). These results correspond to an LO frequency of 140 GHz and an IF frequency of 2 GHz. As observed, the current increases with rising input IF power. At saturation (P_{sat}), the current varies between 15 mA and 23 mA, depending on the LO power level. The maximum power consumption of the mixer, when driven by an LO power of 5 dBm, is 69 mW.



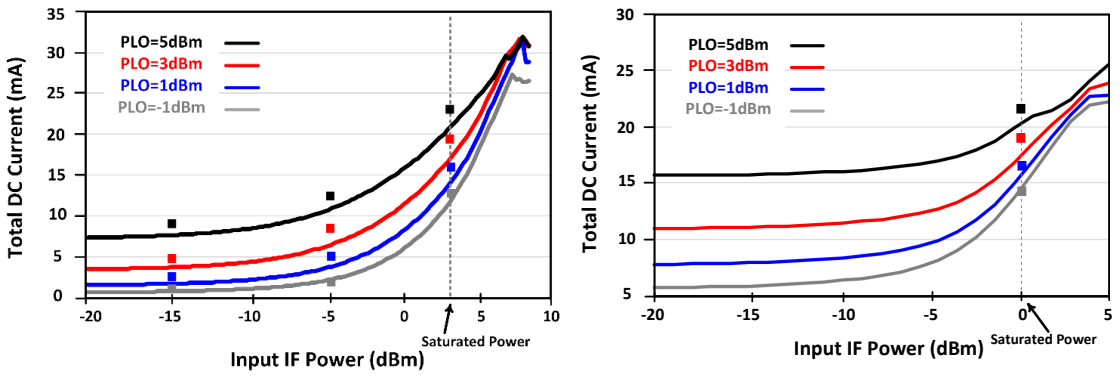
(a) (b)

Figure 4.8: Measured and simulated LO-to-RF port-to-port isolation. (a) Cascode and (b) Darlington pair mixer.



(a) (b)

Figure 4.9: Measured reflection of IF, LO, and RF ports. (a) Cascode and (b) Darlington pair mixer.



(a) (b)

Figure 4.10: Simulated (solid) and measured (squares) DC currents of the mixer versus input IF power at 138 GHz LO and 2 GHz IF frequency for (a) cascode mixer and (b) Darlington pair mixer.

Similarly, Figure 4.10 (b) illustrates the total current consumption of the Darlington pair mixer, operating from a 1.4V DC supply, across different LO power levels at an LO frequency of 138 GHz and an IF frequency of 2 GHz. The results indicate that the current increases with input IF power. At P_{sat}, the current ranges from 14 mA to 22 mA,

depending on the LO power level. The maximum power consumption of the Darlington mixer reaches 31 mW at an LO power of 5 dBm.

4.5 Performance Comparison and FOM Evaluation

Table II provides a comparison of the performance of the up-conversion mixers presented in this work with other published literature within a comparable frequency range. References [33], [34], [35], [36], and [37] relate to up-conversion mixers, while [40], [41], [42] and [43] involve mixers followed by power amplifiers. Almost all the mixers listed in the table use the Gilbert architecture.

The cascode up-conversion mixer stands out for its superior linearity (P_{1dB}), high saturation power (P_{sat}), and excellent LO-to-RF port isolation. Additionally, it has the smallest active chip area among state-of-the-art designs, as highlighted in Table II, while also demonstrating lower power consumption. On the other hand, the Darlington mixer, though exhibiting lower gain and output power compared to the cascode mixer, offers wider bandwidth and is better suited for low-power and low-voltage applications. Notably, according to Figures 4.3 and 4.10 for the same output power of 2 dBm, the Darlington pair mixer consumes only 31 mW of DC power, whereas the cascode up-conversion mixer requires 45 mW. Although the designs presented in [34] and [37] operate with 9 mW and 32 mW of DC power, respectively, the Darlington pair mixer achieves higher P_{1dB} and P_{sat}, making it a more power-efficient choice while maintaining strong linearity and performance.

The figure of merit (FOM) [44], [45] has been assessed to ensure an equitable comparison between the presented mixer and others. The FOM considers conversion gain (CG), linearity (P_{1dB}), and DC power usage (P_{DC}) as the key factors dominating the performance of up-conversion mixers.

$$FOM(dB) = 10log\frac{10^{\frac{CG}{20}} . 10^{\frac{P_{1dB}}{20}}}{\frac{P_{DC}}{1\,mW}} \tag{4.1}$$

The presented cascode mixer has demonstrated the best performance in FOM, attributed to its low DC power dissipation and high linearity compared to all previously documented works listed in Table II.

4.6 Summary

This chapter presented the measurement setup and performance evaluation of the proposed cascode and Darlington pair up-conversion mixers designed for D-band (110–170 GHz) applications. The mixers were fabricated using the 130-nm SiGe HBT B11HFC process and optimized for compact chip area and high output power. A comprehensive measurement setup was implemented to evaluate conversion gain, output power, isolation, and power consumption, ensuring accurate characterization through careful calibration and de-embedding techniques. The cascode mixer demonstrated a maximum

conversion gain of 9.3 dB with a saturation output power of 5.8 dBm, while the Darlington pair mixer achieved a peak conversion gain of 2.1 dB and a P_{sat} of 2.2 dBm. Additionally, port-to-port isolation measurements confirmed strong LO-to-RF suppression, exceeding 38 dB for the cascode mixer and 34 dB for the Darlington pair mixer, highlighting their effectiveness in reducing unwanted signal leakage. Power efficiency comparisons revealed that for the same output power, the Darlington pair mixer consumed lower DC power than the cascode design, making it more suitable for low-power applications. The performance of both mixers was benchmarked against state-of-the-art designs, demonstrating competitive figures of merit in linearity, isolation, and power efficiency. These results validate the proposed architectures as viable solutions for next-generation D-band wireless communication systems.

TABLE II
PERFORMANCE SUMMERY AND COMPARISON WITH THE PRIOR-ART UP-CONVERTER

	Topology	Technology (f_t/f_{max})	Frequency (GHz)	Max. CG (dB)	Psat (dBm)	P_{1dB} (dBm)	LO-RF Isolation (dB)	P_{DC} (mW)	Chip Area (mm^2)	FOM
[33] SSCL 24	Gilbert Cell Up conv.	55-nm SiGe (320/400)	112-150	15	6.3	4.5	-	70-140	1.07	-11.72
[34] MWCL 17	Gilbert Up conv.	40-nm CMOS (195/254)	105-135	-4	-9	-11.5	35	9†	0.63	-17.29
[35] MTT15	Gilbert I/Q Up conv.	250nm InP HBT (350/650)	115-155	6	2.5	-2	27	78	0.25*	-16.92
[36] IJMWT 18	Gilbert I/Q Up conv.	130-nm SiGe (230/280)	119-152	9.8	-1	-4	31	53	0.22*	-14.34
[37] MTT 17	Gilbert Cell I/Q Up conv	130-nm SiGe HBT (350/450)	170-210	-10	-6	-10	-	32	0.7	-25.05
[38] SSCL 24	Single-ended Passive Up conv.	65-nm CMOS (200/250)	110-160	-11.5	-11	-12.5	20.4	-	0.35	-
[39] RFIT 23	double-balanced	40-nm CMOS 195/250	115-145‡	-11.5	-7.5	-7.3	71.5	8.1	0.54	-18.84
[40] ESSC 19	Gilbert Cell I/Q Up conv. PA	130-nm SiGe (350/450)	140-220	10	6.5	-1	-	302	1.4	-20.3
[41] RFIC 18	I/Q Up conv. 2 stg. PA	40-nm CMOS (195/254)	110-125	13.5	-	4.5	-	271	1.51	-15.33
[42] RFIC 19	Gilbert Cell I/Q Up conv. 4 stg. PA	22-nm FDSOI (347/371)	132-139	18	2.8	-	24.7	196	1.44	-
[43] JCN 21	Gilbert Cell I/Q Up conv. 6 stg. PA	130-nm SiGe (230/280)	115-145	23	0	-2	-	240	1.54	-13.3
Mixer1	**Cascode Up conv.**	**130-nm SiGe (250/370)**	**126-152**	**9.5**	**5.4**	**4.9**	**38**	**32†-69‡**	**0.22/0.07***	**-11.04**
Mixer2	**Darlington Up conv.**	**130-nm SiGe (250/370)**	**119-155**	**2.1**	**2.2**	**0.9**	**34**	**31**	**0.26/0.088***	**-13.36**

* Core area † Without LO Power ‡ Graphical Estimation

Chapter 5

Conclusions and future work

This thesis has addressed critical challenges in designing high-performance up-conversion mixers for D-band (110–170 GHz) communication systems, which are vital for next-generation wireless technologies such as 5G, 6G, and beyond. The key contributions of this work include the development and implementation of two novel up-conversion mixer architectures: the cascode mixer and the Darlington pair mixer. The cascode mixer, utilizing a double-mixing technique within a balanced cascode topology, achieved high linearity, robust LO-RF isolation, and enhanced output power. Meanwhile, the Darlington pair mixer, leveraging the Darlington pair configuration, demonstrated improved current gain and bandwidth while maintaining low power consumption. The proposed mixers were benchmarked against state-of-the-art designs, demonstrating superior figures of merit in terms of linearity, isolation, and power efficiency. The cascode mixer, in particular, stood out for its high linearity and low power consumption, positioning it as a strong candidate for high-performance D-band communication systems.

The advancements presented in this thesis have significant implications for the future of wireless communication. The proposed mixer architectures effectively address key challenges in D-band operation, such as high linearity and energy efficiency, which are crucial for emerging applications like autonomous vehicles, augmented reality (AR), and high-throughput satellite communications. By enabling efficient frequency conversion in the D-band, these designs contribute to the development of ultra-high-speed and energy-efficient communication networks. Moreover, their compact and power-efficient nature makes them suitable for integration into a wide range of devices, from consumer electronics to advanced imaging systems. The ability to operate at high frequencies with minimal distortion and power consumption opens new possibilities for applications in radar, medical diagnostics, and security systems, further broadening the impact of this research.

5.1 Future Work

Building upon the contributions of this thesis, several promising directions for future research are identified. One potential avenue is the extension of the operational bandwidth of D-band mixers. This could be achieved by incorporating tunable circuit components or advanced filtering techniques, enabling consistent performance across the full D-band spectrum. Additionally, further investigation into advanced packaging strategies and thermal management solutions is warranted. The use of materials with enhanced thermal conductivity, along with the integration of on-chip cooling mechanisms, could significantly improve the reliability and long-term stability of high-frequency circuits.

Furthermore, it is important to note that a phase quadrature mixer, derived from the proposed balanced cascode topology, has already been successfully implemented and integrated into a fully functional transmitter system. The system has undergone measurement and demonstrates state-of-the-art performance. A dedicated manuscript detailing the system-level design, integration, and measured results is currently in preparation. This work further validates the practical viability of the proposed mixer architecture and its compatibility with other transceiver building blocks in high-frequency communication systems. Building upon this foundation, future work will focus on extending the mixer design to even higher frequency bands, such as the H-band, to address the growing demand for ultra-high-speed wireless communication applications."

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