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Enhancing the performance of high-power DUV-LEDs with sloped sidewall by introducing N-electrode holes and interrupted mesa

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Abstract: This study introduces innovative structural enhancements in deep ultraviolet LEDs (DUV-LEDs) to optimize Performance. By implementing a 46.9° sloped mesa sidewall, we have designed what we believe to be two novel structures: an n-electrode hole structure that extends the active region and an interrupted mesa structure that significantly enlarges the sidewall area. We investigated the effects of these structures on DUV-LED performance independently and demonstrated that both single structure devices surpass the performance of conventional DUV-LEDs. Notably, the interrupted mesa structure yields a more substantial performance enhancement at higher injection currents, while the n-electrode hole structure excels at lower currents. Meanwhile, this paper also prepared two kinds of DUV-LEDs with parallel and staggered rows of mesa and n-electrode holes by combining the above two single structures on the same device. Compared with the single structure device, the performance of these combined structure devices is further improved, in which the performance of the DUV-LEDs with staggered rows of mesa and n-electrode holes is even better, the external quantum efficiency (EQE) and wall plug efficiency (WPE) of 9.19% and 7.13% at 250 mA operating current, which is an improvement of 9.6% and 4.4%, respectively, compared with that of the conventional DUV-LEDs. Furthermore, the enhancement in performance will be augmented with an increase in current, due to the efficient conversion of active area to sidewall area. At 500 mA, the optical power of the staggered-array device is increased by 10.6% compared to conventional DUV-LEDs; at 1000 mA, the optical power is increased by 17.7%.

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1. Introduction

AlGaIn-based deep ultraviolet light-emitting diodes (DUV-LEDs) are emerging as the optimal replacement for traditional mercury lamps, thanks to their compact size, extended lifetime, tunable wavelength, low energy consumption, and mercury-free composition [1–3]. These attributes have showcased their vast potential across various applications, including sanitization, medical diagnostics, signal communication, and ocean purification [4,5]. Despite these advantages, the external quantum efficiency (EQE) of DUV-LEDs, particularly those designed for high-power applications, remains critically low. Contributing factors include significant dislocations within the chip, substantial light absorption by the chip material, intense transverse magnetic polarization of light, and notable differences in refractive index between the chip material and air [6,7].

Overall, the performance of deep UV LEDs is mainly limited by both internal quantum efficiency (IQE) and light extraction efficiency (LEE). The IQE is mainly limited by the high Mg activation energy and the asymmetric flow of electrons and holes in the p-AlGaIn hole source layer (HSL), which leads to a very low injection efficiency of holes [8]. Recent studies have shown that tunneling-based UV-LEDs can effectively mitigate the asymmetric flow of electrons and holes and improve the injection efficiency of carriers into the active region [9–11], and the graded p-AlGaIn layer can also solve the injection efficiency problem well [12,13]. These improvements can dramatically increase the internal quantum efficiency of UV-LEDs, even beyond 80%. In terms of LEE, several innovative approaches have been implemented in the structural design of these LEDs. Techniques such as nano-patterned sapphire substrates [14–16], over-etched p-GaN layers [17], n-GaN surface texturing [18], and side-wall optical waveguide modulation [19] have been explored. We made a data benchmark table of the relevant parameters of high-performance UVC LEDs reported in recent years, as shown in Table 1 [20–27].

Table 1. Benchmark table of high-performance UVC LED performance reported in recent years.

References	Structure	LOP@100mA	EQE@100mA	Wavelength
Shatalov et al. [20]	Reducing threading dislocation density	≈28.2 mW	≈6.92%	278nm
Takano et al. [21]	Mg contact layer/Rh mirror electrode/PSS/resin coating	18.3 mW@20 mA	20.3%@20 mA	275nm
Maeda et al. [22]	Highly Reflective Ni/Al p-Type Electrodes	33 mW	9%	279nm
Kuo et al. [23]	Mesh p-GaN/ITO	5.64 mW@20 mA	6.3%@20 mA	280nm
Zhang et al. [24]	Ag-nanodots/Al reflective electrode	6.7 mW	≈1.5%	280nm
Qian et al. [16]	Internal-roughed sapphire	≈13.8 mW	≈3.05%	275nm
	Internal-roughed sapphire + SiO ₂ -antireflection film	≈14.5 mW	≈3.25%	
Zheng et al. [25]	Single layer nano-pattern arrays	~	≈3.4%	273nm
	Double layer nano-pattern arrays	~	≈2.95%	
Peng et al. [26]	Chip sidewall geometries	12.99 mW	2.854%	277nm
Liao et al. [27] ~	Ni/Au electrodes	17.29 mW	≈3.8%	275nm
	Ni/Rh electrodes	19.6 mW	≈4.25%	
	Ni/Rh/Ni/Au electrodes	19.75 mW	4.33%	
	This work	43.66 mW	9.72%	275nm

In the relevant optimization scheme, the sidewall optical waveguide modulation technique offers significant advantages in cost-effectiveness, ease of implementation, and the extent of performance enhancement [28]. Recent advancements in research on sidewall optical waveguide modulation schemes for DUV-LEDs have yielded significant progress. Innovations include the realization of multi-angle sloped sidewalls [29–31], in-depth optical path simulations within the chip [32–34], and optimized selection of materials for the sidewall reflective layers. The core advantage of the optical waveguide modulation scheme lies in its ability to utilize sidewall reflections to enhance the EQE of DUV-LEDs. However, a critical challenge remains: as the chip size increases, the proportionate area of the sidewall significantly decreases. Enlarging the sidewall area could inadvertently result in the loss of the device's active area. Therefore,

achieving an optimal balance between the sidewall reflection area and the active area is crucial for further enhancing the performance of DUV-LEDs that rely on sloped sidewall reflections. Addressing this challenge is pivotal in advancing the application of this promising technology in various high-performance optical devices.

This paper details the introduction of two novel structural for DUV-LEDs, based on a 46.9° mesa sidewall angle. We designed and fabricated an n-electrode hole structure, aimed at expanding the active area, and an interrupted mesa structure, intended to significantly enhance the reflective area of the device sidewalls. Results from our study indicate that both the n-electrode hole and the interrupted mesa structures substantially improve the performance of DUV-LEDs, and provide a 5.1% increase in radiant flux at 500 mA. Additionally, we explored the synergistic effects of these two structures by integrating them into a single device and optimizing the layout of the mesa and n-electrode holes. Two configurations were prepared: parallel and staggered arrangements. Our data reveal that the device with the staggered arrangement of mesa and n-electrode holes outperforms all other designs presented in this study, the EQE and WPE of 9.19% and 7.13% at 250 mA operating current, which is an improvement of 9.6% and 4.4%, respectively, compared with that of the conventional DUV-LEDs. This superior performance is attributed to the efficient conversion of the active area to sidewall area and enhanced current spreading capabilities, demonstrating the potential of this integrated approach for advancing DUV-LED technology.

2. Experiments

This paper uses a commercially available DUV LED epitaxial wafer with a peak wavelength of 275 nm, and the epitaxial structure includes a 10 nm p^+ -GaN contact layer, a 30 nm p - $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ injection layer, a 40 nm $\text{Al}_{0.7}\text{Ga}_{0.3}\text{N}$ EBL layer, a 48 nm $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}/\text{Al}_{0.48}\text{Ga}_{0.52}\text{N}$ MQW layer (3 pairs of 13 nm quantum barrier/3 nm quantum well), a 1100 nm n - $\text{Al}_{0.55}\text{Ga}_{0.45}\text{N}$ contact layer, 1600 nm n - $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ layer, 80 nm n - $\text{Al}_{0.71}\text{Ga}_{0.29}\text{N}$ transition layer, 2500 nm AlN layer.

In the pre-experiments, we used $2\text{ }\mu\text{m}$ RZJ304 photoresist, $2\text{ }\mu\text{m}$ EPG516 photoresist and 250 nm SiO_2 as a mask for the mesa etching, which formed sidewall angles of 30.1° , 46.9° and 70.7° , respectively. The etching gas mixtures used in the etching included chlorine, boron trichloride, and argon at flow rates of 150 sccm, 5 sccm, and 5 sccm, respectively, with the chamber pressure maintained at 3 mTorr, and with an upper RF power of 400 W and a lower RF power of 150 W.

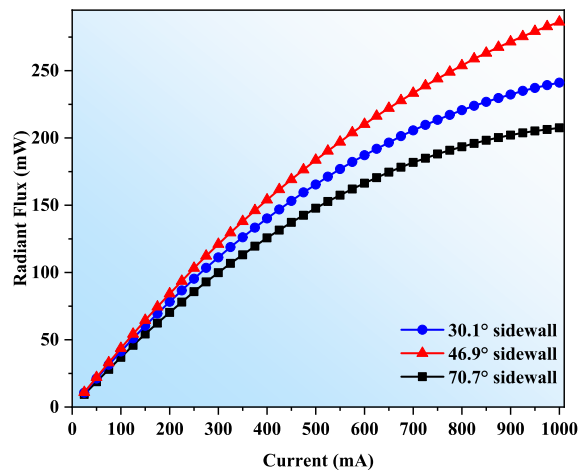


Fig. 1. Radiant flux for same structure devices with 30.1° , 46.9° , and 70.7° mesa sidewalls.

The radiant fluxes of DUV LEDs with these three sidewall angles were measured, and the results are shown in Fig. 1. The experimental results show that the device with 46.9° sidewall has higher optical performance, which is in line with the previously reported results that 41° – 49° sidewalls can be more favorable to enhance the light extraction ability of the device [32]. Therefore, we chose 46.9° as the sidewall angle of the device in the experiments of this paper, and the cross-section of the simplified mesa model and the scanning electron microscope image of the sidewall angle are shown in Fig. 2.

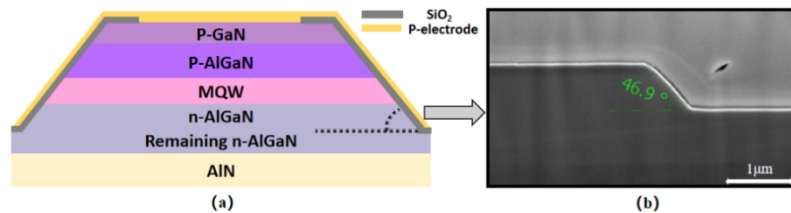


Fig. 2. Schematic of the (a) mesa section and (b) mesa sidewall angle of the device.

This study outlines the fabrication processes of DUV-LEDs with various structural designs, as depicted in Fig. 3. These designs include conventional structure, n-electrode hole structure, interrupted mesa structure, and both parallel and staggered combination structures. For ease of reference and subsequent analysis, these five DUV-LED structures are designated as LED I, LED II, LED III, LED III, and LED IV, respectively. It is worth noting that the novel structure mentioned above is formed by changing the geometrical design of the mesa on the basis of the conventional structure, and all the LEDs designed in this paper have the same overall size ($1176\mu\text{m} \times 1168\mu\text{m}$). The conventional LEDs include four $221\mu\text{m} \times 1000\mu\text{m}$ mesas, and the interrupted mesa structure increases the sidewall area of the device by splitting the mesa in the conventional LEDs to form sixty-four $221\mu\text{m} \times 47.5\mu\text{m}$ mesas; the n-electrode hole structure converts the strip-shaped n-electrode grooves in conventional LEDs into fifteen n-electrode holes of $58\mu\text{m} \times 33.5\mu\text{m}$, which ensures that the n-electrode injections are uniformly distributed throughout the entire chip area while retaining a portion of the active area that should have been etched away; by combining the interrupted mesa structure and the n-electrode hole structure described above and changing the arrangement of the two, a parallel combination structure and a staggered combination structure are formed.

The detailed preparation process includes: Isolation grooves are formed on the epitaxial wafer by etching, dividing the entire epitaxial wafer into a number of $1168\mu\text{m} \times 1176\mu\text{m}$ rectangles, which define the dimensions of the device, and the depth of etching is $4\mu\text{m}$, terminating at the AlN layer. After that, the epitaxial wafer was etched to form a fork finger and interrupted mesa structure with an etching depth of 700nm , terminating at the n-AlGaIn layer and then a SiO_2 protective layer of 500nm was deposited on the device surface for protection of the etch-formed mesa sidewalls, and the contact windows of the n/p electrodes were exposed by dry etching plus wet etching; Then total 130nm thick Cr/Ti/Al/Ni/Au/Ti was deposited to form the n ohmic contact and annealed; The p ohmic contact were formed by depositing total 50nm thick Ni/Rh/Ti at the windows of the p electrodes, and in addition the Ni/Rh/Ti film were also deposited on the surface of SiO_2 passivation which is on the sidewalls of the mesa, use the better UV reflective properties of Rh to form a reflective layer; Thereafter, a $0.81\mu\text{m}$ thick Pt/Ti/Au electrode covering layer was deposited on the n/p electrode to optimize the electrical characteristics; $1\mu\text{m}$ thick SiO_2 passivation layer was grown to protect the overall sidewall of the device after etching the isolation grooves and forming the contact window of the pad by etching; Finally, $4.7\mu\text{m}$ thick Au/Sn electrode pads were prepared for subsequent flip-flop soldering. The luminescence diagram of the novel device designed in this paper is shown in Fig. 4(a), while a

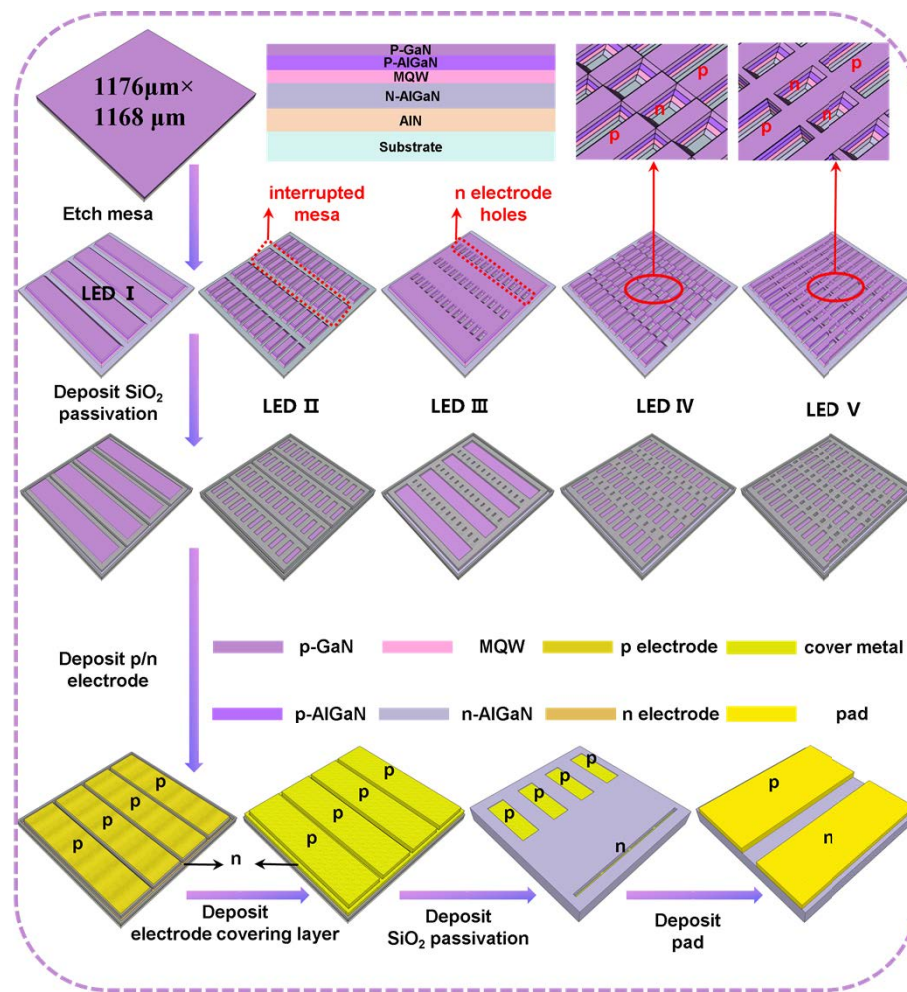


Fig. 3. Flow chart for the preparation of devices with different chip structures.

simple model has been built to facilitate the understanding of two types of arranging mesa with the n-electrode holes, as shown in Fig. 4(b).

3. Results and discussion

In this section, the performance improvement of single-structured devices and combined-structured devices will be discussed separately, and for the convenience of subsequent analysis, we list the key parameters of LED I - LED IV in Table 2. It is worth noting that the mesa area is highly correlated with the active area and the mesa edge length of the device can quantitatively illustrate the value of the sidewall area under fixed etching conditions, so we give the mesa area and the mesa edge length of different LEDs in Table 2 in response to the active area and sidewall area of the device. The EL spectra of LED I - LED IV are also shown in Fig. 5.

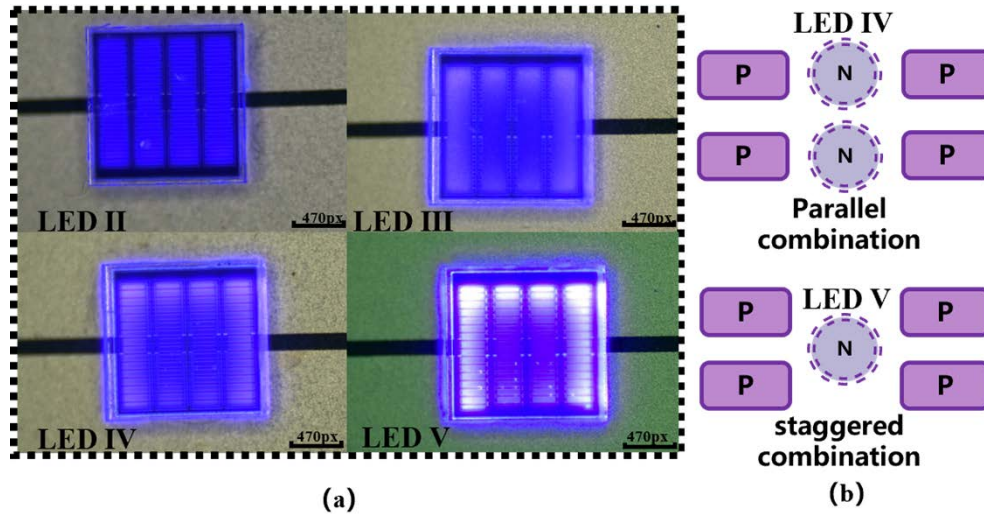


Fig. 4. (a) Device luminescence diagrams of LED II- IV and (b) distribution model of the mesa with n-electrode holes.

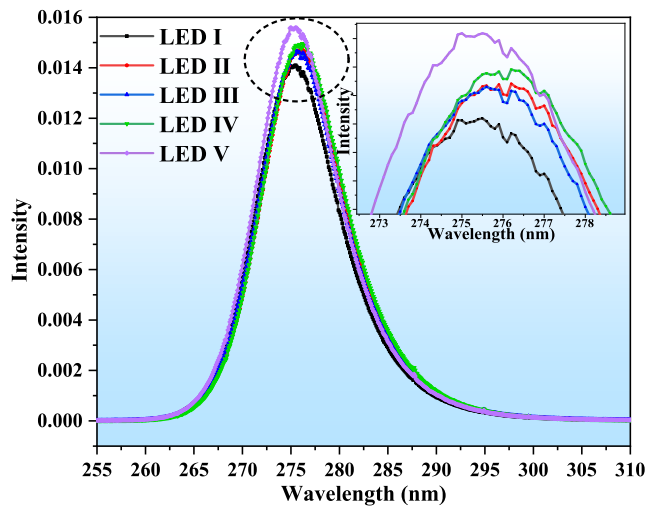


Fig. 5. EL spectrograms of LED I- IV at 500 mA.

Table 2. LED I - LED IV structure and size parameters.

Samples	LED I	LED II	LED III	LED IV	LED V
Mesa area (μm^2)	8.84×10^5	6.7×10^5	9.62×10^5	7.67×10^5	7.74×10^5
Mesa side length (μm)	9808	34368	11867	38032	37121
n electrode holes	wo	wo	w	w	w
Interrupted mesa	wo	w	wo	w	w

3.1. Performance analysis of DUV-LEDs with single structure

Figure 6(a) shows the radiant fluxes comparison of LED I, LED II, and LED III in the range of 0-1000 mA. The data show that both the n-electrode hole structure and the interrupted mesa structure can significantly enhance the luminescence performance of DUV-LEDs. The performance enhancement from LED II mainly comes from the increased sidewall area, which can be reflected by the edge length of the sidewall. The data in Table 2 shows that LED II has a sidewall edge length of $34,368 \mu\text{m}$ and a mesa area of $6.7 \times 10^5 \mu\text{m}^2$, while LED I has a sidewall edge length of $9,808 \mu\text{m}$ and a mesa area of $8.84 \times 10^5 \mu\text{m}^2$. The interrupted mesa structure increases the sidewall area by 250%, while only reducing the mesa area by 24.2%. In general, by changing the structure of the device to increase the sidewall area of the device will inevitably cause a reduction in the mesa area, and the mesa area is highly correlated to the active area. Therefore, even if the sidewall reflective area of the device is increased, if the lost mesa area is too large, the overall performance of the device will be degraded. The interrupted mesa structure can be retained in the active area as much as possible in the case of a substantial increase in the sidewall area of the device, in the sloped sidewall program, a larger sidewall area allows more light to be reflected through the sloped sidewall directly to the substrate for light extraction, which effectively improves the performance of the LED II.

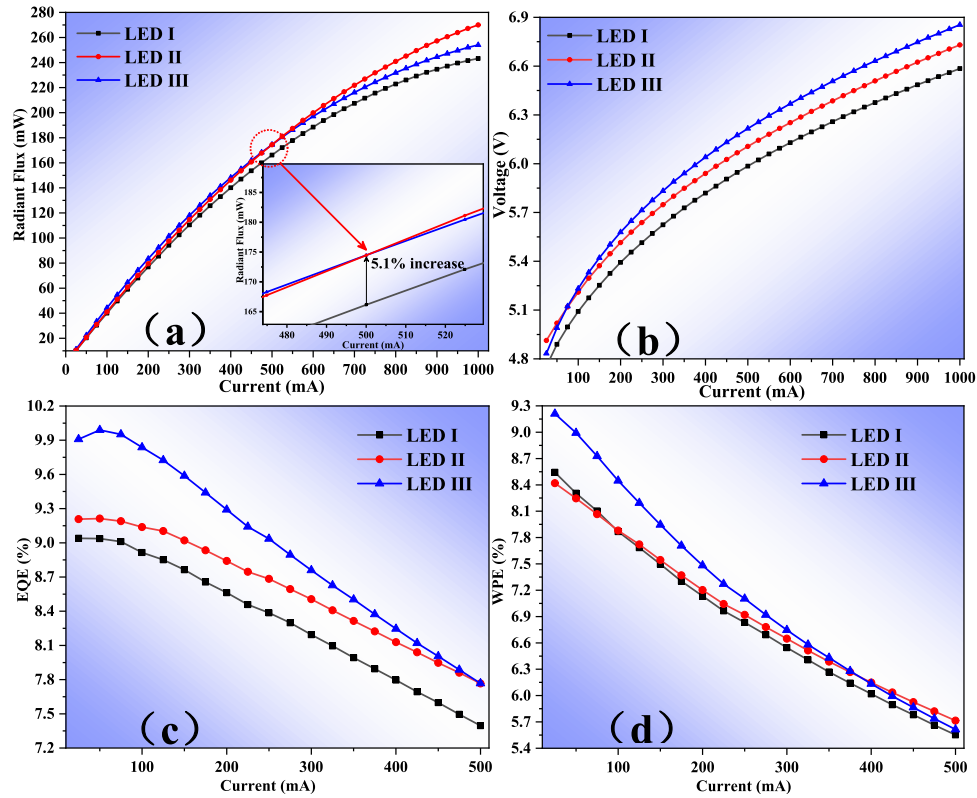


Fig. 6. Comparison of (a) radiant fluxes, (b) voltage, (c) EQE, and (d) WPE between two single optimized and conventional structures.

The performance improvement offered by LED III comes mainly from the expansion of the active area due to the n-electrode hole structure. n-electrode hole achieves dual functionality: enabling uniform current injection via the n-electrode across the semiconductor die; while simultaneously ensuring preservation of extra active regions that conventional fabrication

methods would otherwise remove. According to the data in Table 2, the mesa area of LED III is $9.62 \times 10^5 \mu\text{m}^2$, which is 8.8% more than that of LED I. At a 500 mA cutoff point, both LED II and LED III show a 5.1% improvement in radiant flux compared to LED I. Under lower current injections, LED III outperforms due to its larger mesa area. However, as current levels rise, the performance of LED III declines relative to LED II. This phenomenon may be the result of more severe heat accumulation problems in LED III. The high temperature-induced problems such as Al component fluctuation, carrier leakage, defect density increase, and stress change will lead to an increase in the nonradiative centers and a decrease in the ratio of radiative recombination in the quantum wells [35–37], which will lead to a sharp decrease in the internal quantum efficiency of the device, resulting in low performance of LED III at higher injection levels. To verify this thesis, infrared thermography measurements were performed on LED II and LED III at 250 mA, 350 mA, and 450 mA, respectively, using a water-cooled heatsink at 25°C and fixing the chip to the heatsink with a thermally conductive adhesive. As illustrated in Fig. 7, the average chip surface temperature of LED II escalated from 38.41°C to 52.73°C with current elevation from 250 mA to 450 mA, whereas LED III exhibited a more pronounced thermal response, increasing from 40.27°C to 59.32°C. This comparative analysis reveals that LED III demonstrates 22.5% greater temperature elevation under identical current increments compared to LED II (19.05°C vs. 14.32°C). The steeper thermal gradient observed in LED III confirms its exacerbated thermal management challenges, thereby corroborating the correlation between its accelerated performance degradation and thermal accumulation phenomena.

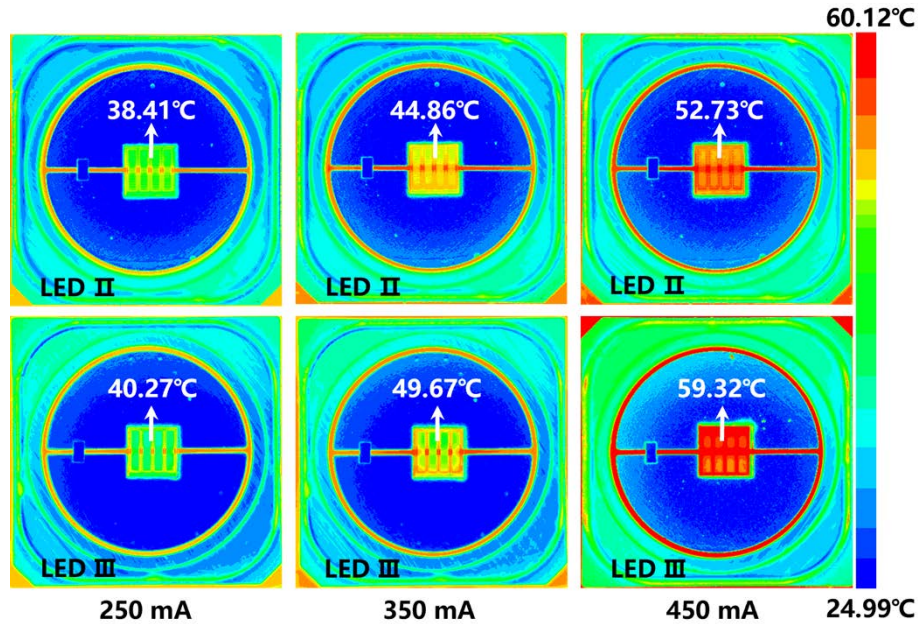


Fig. 7. Comparison of infrared thermal image results of (a) LED II and (b) LED III.

Figure 6(b) shows the voltages of the three devices, and the voltages of LED II and LED III are increased compared to LED I. The voltage increase of LED III originates from the decrease of the ohmic contact area between the p electrode and p-GaN, while LED II originates from the decrease of the ohmic contact area between the n-electrode and n-AlGaIn.

Figure 6(c) and Fig. 6(d) show the comparison of the EQE and WPE of the three LEDs in the range of 0-500 mA. From the figure, it can be seen that with the increase of current, the EQE of the three LEDs, although they all decrease, the decrease rate is obviously different. Among

them, the EQE of LED III has a significantly higher decline rate, while the EQE of LED II is smoother with the current change. This phenomenon also stems from the different temperature gradient with the current change, the temperature rise of LED III is significantly higher under the same current increment, so that its performance will degrade faster when the current increases. However, their EQE and WPE are better than LED I at 0-500 mA, and at 250 mA operating current, the EQE of LED II and LED III are 8.68% and 9.03%, and the WPE is 6.92% and 7.1%, respectively.

3.2. Performance analysis of DUV-LEDs with combined structure

Figure 8(a) shows the comparison of the radiant fluxes of LED I, LED III, and LED IV in the current range of 0-1000 mA, and the radiant fluxes of LED III and LED IV are enhanced by 7.5% and 10.6% respectively compared to LED I at an injection current of 500 mA. This enhancement exceeds that of LED II and LED III, which only have a single structure. The interrupted mesa structure increases the sidewall reflection area but sacrifices part of the active area. Conversely, the n-electrode hole structure increases the active area of the device without affecting the sidewall reflection area. The integration of n-electrode holes with the interrupted mesa allows the device to maintain both a high sidewall reflection area and a large active area, optimizing light output and efficiency. The active areas and sidewall edge length of LED IV and LED V are shown in Tab. II. Compared to LED I, the sidewall area of both increased by 290.5% (13.2% reduction in mesa area) and 278.5% (12.4% reduction in mesa area), respectively. The efficient conversion of mesa area to sidewall area means that the device can have a large sidewall area while keeping the active area as large as possible. The larger sidewall area allows more light to be reflected through the sloped sidewalls directly to the substrate for light extraction, which substantially boosts the LEE of LED III-V, especially under higher currents. At 1000 mA, the radiant flux of LED V shows an impressive increase of 17.7% compared to LED I.

The performance difference between LED IV and LED V is mainly due to the type of arrangement of the n-electrode holes with the mesa. The n injection point of the parallel structure is surrounded by six p injection points, but the spacing between the n/p injection points is not the same, which leads to the current component between the n/p injection points with the shortest spacing being significantly higher than that of the other positions, which is prone to causing local current crowding and triggering the thermal accumulation problem leading to performance degradation. Whereas the staggered structure of n-electrode holes and mesa changes the injection positions of electrons and holes, this adjustment allows an n injection point to be located immediately adjacent to four p injection points with the same spacing, which can lead to a more uniform current distribution between the n/p injection points and alleviate the current crowding. By conducting infrared thermal image measurements of LED IV and LED V at 250 mA, 350 mA and 450 mA respectively, we found that the chip temperatures of LED IV and LED V were almost indistinguishable at 250 mA, but the temperature difference increased to 1.27°C at 350 mA and 2.92°C at 450 mA, as shown in Fig. 9. As the size difference between LED III and LED IV is very small, the temperature change mainly stems from the difference in current injection and diffusion uniformity, this difference in the magnitude of the thermal difference with the change in current intensity confirms the superiority of the LED IV kind of staggered arrangement structure.

Figure 8(b) compares the voltages of LED I, LED IV, and LED V, showing that the voltage of the combined structure increases from that of the single structure. Nevertheless, at an operating current of 250 mA, LED V still exhibits the highest EQE and WPE among all LEDs designed in this paper, reaching 9.19% and 7.13%, respectively, which is an improvement of 9.6% and 4.4%, respectively, compared with that of LED I, as shown in Fig. 8(c) and (d). Notably, we found that the EQE drop with current seems to be faster in all devices, which may be related to the overshooting of energetic electrons into the p-type layer at high injection levels, an electron

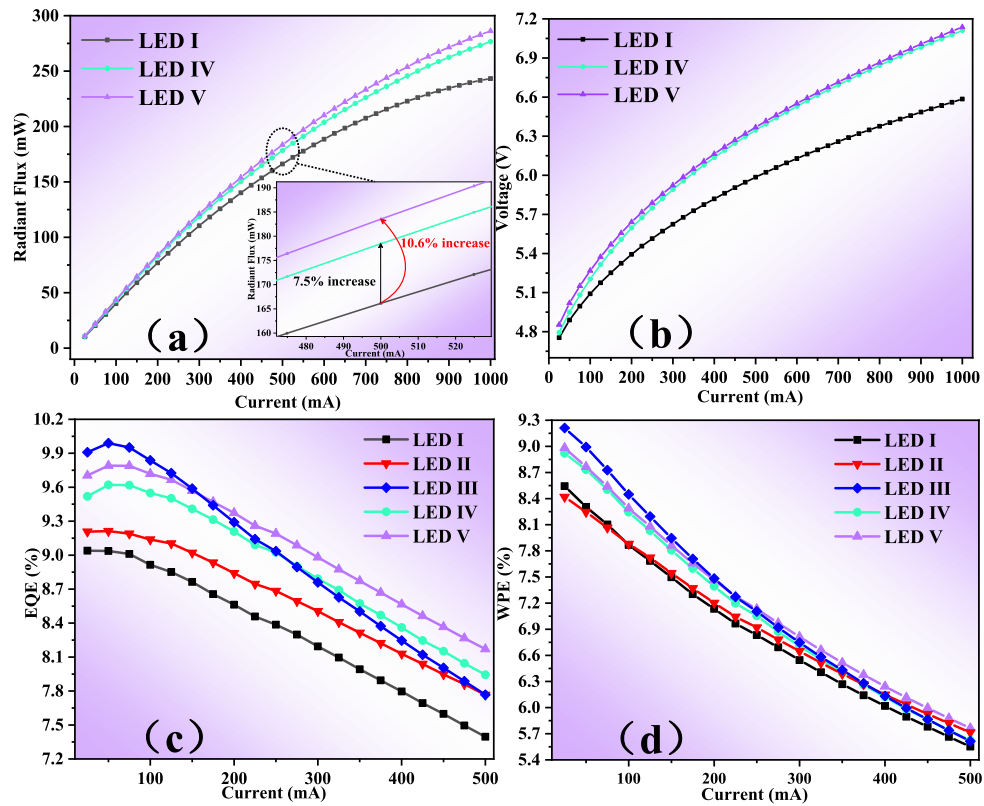


Fig. 8. Comparison of (a) radiant fluxes, (b) voltage, (c) EQE, and (d) WPE for the two combined structures and the conventional structure.

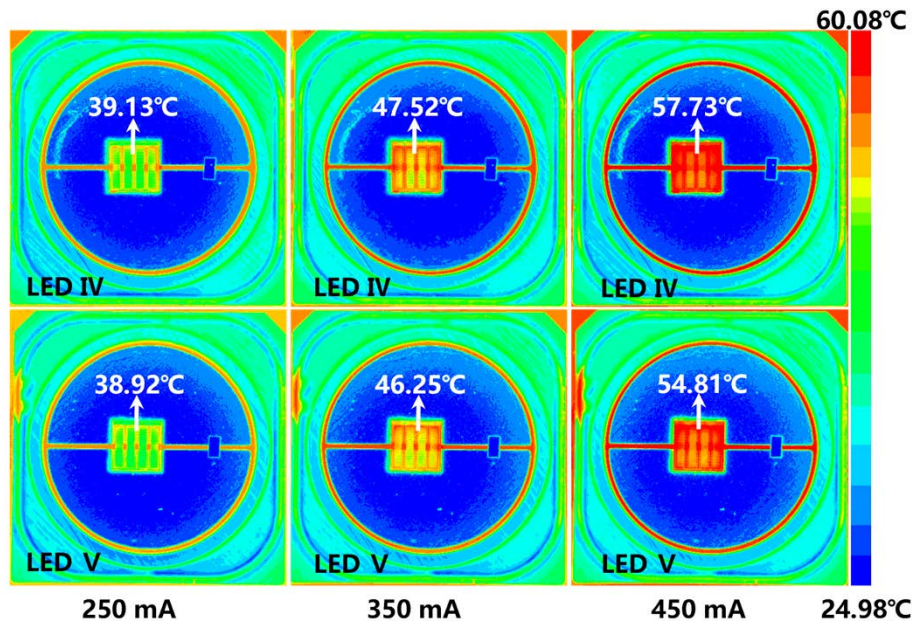


Fig. 9. Comparison of infrared thermal imaging results of (a) LED IV and (b) LED V.

leakage phenomenon that strongly compounds the efficiency of carriers in quantum wells [38,39]. The issue of EQE drop for single structure devices (LED II, LED III) has been discussed in the previous section. For the combined structure devices, we find LED V has better maintenance of EQE with current compared to LED IV. This stems from the fact that the staggered n-electrode holes and mesa position can make the shortest spacing between n and p injections the same, so that the main current paths can be uniformly distributed throughout the entire chip range, alleviating the performance degradation caused by the localized high temperature rise, which is also well verified in the infrared thermogram results in Fig. 9.

4. Conclusion

In this paper, high-power DUV-LEDs with n-electrode holes and interrupted mesa surfaces have been successfully designed and prepared, and the effects of a single n-electrode hole structure or interrupted mesa structure on the performance of high-power DUV-LEDs based on the sloped sidewall have been investigated. The interrupted mesa structure can increase the sidewall area of the device by 250%, while the n-electrode aperture structure is able to increase the active area by 8.8%, and these increases in sidewall reflective area and active area significantly optimize the performance of the device. Also, this paper successfully combines these two single structures and optimizes the arrangement of the mesa and n-electrode holes. The experimental data show that this combined structure device further improves the performance on the basis of the single structure device, especially the device with n-electrode holes staggered with the mesa exhibits the optimal performance due to its more side-wall reflective area, larger active area and better current spreading capability.

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Disclosures. The authors declare no competing interests.

Data availability. All data supporting the findings of this study are available within the paper.

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