

# **Characterization and Modeling of Dual-Input Doherty Power Amplifier for High Efficiency and Bandwidth**

Downloaded from: https://research.chalmers.se, 2025-06-08 06:28 UTC

Citation for the original published paper (version of record):

Basaglia, G., Zhou, H., Bosi, G. et al (2025). Characterization and Modeling of Dual-Input Doherty Power Amplifier for High Efficiency and

Bandwidth. 2025 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), In press. http://dx.doi.org/10.1109/INMMIC64198.2025.10975670

N.B. When citing this work, cite the original published paper.

research.chalmers.se offers the possibility of retrieving research publications produced at Chalmers University of Technology. It covers all kind of research output: articles, dissertations, conference papers, reports etc. since 2004. research.chalmers.se is administrated and maintained by Chalmers Library

# Characterization and Modeling of Dual-Input Doherty Power Amplifier for High Efficiency and Bandwidth

Gabriele Basaglia
Department of Engineering
University of Ferrara
Ferrara, Italy
gabriele.basaglia@unife.it

Han Zhou

Department of Microtechnology
and Nanoscience
Chalmers University of
Technology
Gothenburg, Sweden
han.zhou@chalmers.se

Gianni Bosi

Department of Physics

University of Milano-Bicocca

Milano, Italy
gianni.bosi@unimib.it

Valeria Vadalà
Department of Physics
University of Milano-Bicocca
Milano, Italy
valeria.vadala@unimib.it

Antonio Raffo
Department of Engineering
University of Ferrara
Ferrara, Italy
antonio.raffo@unife.it

Giorgio Vannini
Department of Engineering
University of Ferrara
Ferrara, Italy
giorgio.vannini@unife.it

Christian Fager

Department of Microtechnology and

Nanoscience

Chalmers University of Technology

Gothenburg, Sweden

christian.fager@chalmers.se

Abstract—This paper presents the improvement, in terms of efficiency, that can be achieved by a dual-input Doherty Power Amplifier (DPA) in relation to the more classical single-input configuration. The better results obtained from the dual-input solution are intrinsically connected to the independent control of the two inputs in terms of power and phase. In particular, above the power backoff point, the degree of freedom given by the control of the phase difference between the inputs allows one to operate in a condition of maximum efficiency at any output power level. To test the board and validate the results, a dedicated experimental setup for the characterization of the amplifier has been designed and realized. As will be demonstrated, the efficiency of a dual-input DPA is considerably improved compared to the single-input configuration.

Keywords—Doherty, dual-input, phase control, power amplifier, efficiency.

## I. INTRODUCTION

Doherty power amplifiers (DPAs) are one of the most important efficiency enhancement architectures in communication field. They are frequently adopted because they do not require phase modulation (Chireix [1]) or a sophisticated tracker with accurate synchronization (envelope tracking [2]). Thus, differently from other architectures, they work directly on a modulated RF input leading them to a commercial success [3], [4]. In this work, two different boards, i.e., a single-input and a dual-input DPA, were realized starting from an existing singleinput Doherty prototype design [5] which has been modified exploiting an upgraded, more efficient, version of its transistors. The two realized boards are mainly the same, apart from the input section, thus enabling a fair comparison between their performances and a true evaluation of the advantages in terms of efficiency given by the dual-input DPA. The idea behind the control of the phase is that for output power levels higher than the power back-off (the point at which the auxiliary amplifier comes into play and realizes the load modulation) the variation of the phase of the auxiliary signal can let an improvement of efficiency at the same output power level. In particular, it can be appreciated how the phase change at the auxiliary input can significantly increase efficiency up to 5-6% when compared to the single-input DPA configuration. In order to find the phase difference that consents to reach the best efficiency for each output power level, the dual-input board has been characterized using a VNA that has two internal sources with independent phase and power control.

#### II. DPA BOARDS REALIZATION

The single-input DPA design from which we started to develop a new dual-input version is the one presented in [5]. This is a symmetrical DPA with high efficiency and extended bandwidth reached with the use of an innovative load modulation network (through a black box method) which allows to cover frequencies from 1.6 GHz to 2.7 GHz. In the present work, a newer version of the transistor is chosen to improve the overall performance in terms of efficiency, output power and gain. The selected transistor is a 10-W Macom GaN HEMT, model CG2H40010F. Compared to the previous model (i.e., CGH40010), the new version shows increased small-signal gain (+2 dB at 2.0 GHz), saturated power (+4 W typical value, 17W total), and efficiency (70% versus the previous 65%). The output matching network is, basically, the same as the one designed for the previous board. The property of covering a high bandwidth is inherited from the previous design. After the project, the bias was experimentally tuned using an optimal combination of gate and drain voltages for each different frequency of the working bandwidth to obtain the best performances. The gate bias was set in the range from -2.45 to -2.35 V for the main amplifier (class AB) and from -9 to -5 V for the auxiliary gate (class C). The drain bias was set in the range from 25 to 27 V for the main amplifier and from 28 to 30 V for the auxiliary amplifier.

The dual-input board is identical to the single-input one apart from the input section: the single-input connector followed by a

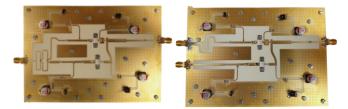


Fig. 1 Realized boards: single-input (left) and dual-input (right).

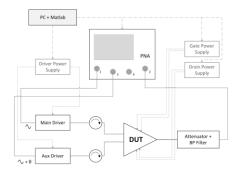


Fig. 2 Measurement setup for dual-input DPA.

Wilkinson power divider has been replaced with two connectors with direct access to both the amplifier branches.

#### III. MEASUREMENT SETUP

# A. Setup configuration

The DPA characterization requires a dedicated measurement setup that allows one to control the dual-input board to validate the simulation results. The setup adopted is depicted in Fig. 2 and includes the following instruments.

- 4-port VNA PNA-X N5247B (Keysight): enables the control of two internal sources independently in power and relative phase.
- Power Supply E36312A (Keysight): supplies the gate bias to the transistors.
- Two power supplies HMP4040 (Rohde & Schwarz): one is used to supply the drain bias to the transistors, and the other one is used to supply the bias for the drivers.
- Two power drivers ZHL-16W-43-S+ (Mini-Circuits): provide the correct input power to the DUT.

External attenuators (42 dB in total) were added to safely measure the power injected into the instrument by the amplifier. In addition, a low pass filter was added to filter out higher harmonic components. The measurements have been performed under continuous wave operation.

#### B. Setup considerations and choices

In the described setup, the control of the drivers and, consecutively, the power injected into the DPA, is made with an "open loop" control. Before building the entire setup, the drivers were characterized and a dedicated look-up-table (LUT) was built. The LUT associates the desired driver output power with the required input power from the PNA. This open-loop control is less accurate than a "closed loop" configuration but it permits

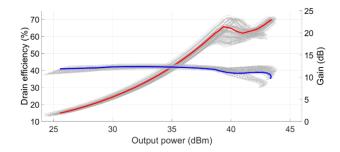


Fig. 3 Example of bias selection (at 2.5 GHz) to get the best performance in terms of drain efficiency (red) and gain (blu).

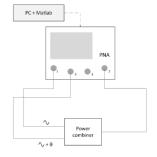


Fig. 4 Phase characterization setup.

to operate in a safer way for the PNA, avoiding the unexpected connection of high-power signals to its receivers.

#### C. DPA Bias Settings

In order to get the best results in terms of efficiency (having special consideration for a good gain level), for the different frequencies, also different bias conditions, mainly of the gate, were investigated. This was done because some changes in the bias could positively affect the board performance at different working frequencies. As reported in Fig. 3, at a specific frequency (2.5 GHz in the figure) only one bias condition was selected, among all the other curves achieved from different biases, to obtain good performance in efficiency and gain.

### D. Phase Control

The measurement of a dual-input DPA cannot be carried out without a control of the phase for the auxiliary input. The PNA has a functionality called Source Phase Control, i.e., an optional feature that provides a control of the phase difference between its two internal sources The disadvantage of using this "open loop" setting is that the phase is not under control at real time. So, to avoid any possible discrepancy between the phase set and the phase truly obtained from the PNA, a preliminary characterization of the phase control was performed by using the setup in Fig. 4 which is composed of a power combiner connected to the PNA. The idea for characterizing the phase is the following: a signal with fixed power and zero-phase is generated at port 1 of the PNA (measured with receiver R1), while another signal generated at port 3 (measured with receiver R3) is providing power with varying phase offset referred to the signal of port 1, where the offset goes from 0° to 360°. The combination of these two signals, at the output of the power combiner, is measured by receiver B at port 2. The received

signal is always maximum when the two sources are in-phase, whereas it is minimum when the sources have a phase difference

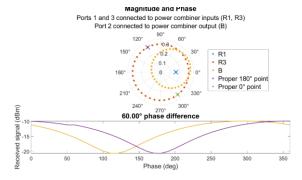


Fig. 5 Phase difference search.

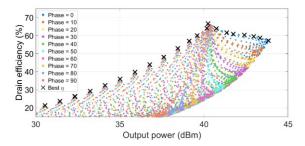


Fig. 6 Scatter plot of dual DPA drain efficiency points with different phases at 2.3 GHz (simulated).

of 180°. Selecting the minimum and maximum points and knowing the phase difference between port 1 and 3 set in the PNA, it is possible to characterize the true offset by subtracting the 180° offset angle, between source 1 and 3, and the angle of the received signal at which its magnitude is minimum. In Fig. 5, it is possible to observe an example of the offset calculation. The polar scattered plots report: the constant-phase signal generated at port 1 (measured by receiver R1), the phase-varying signal generated at port 3 (measured by receiver R3) and the combined signal at port 2 (measured by receiver B). Then, in the plot below, the magnitude of the combined signal is plotted against the phase, highlighting the minimum point at which the signals are out of phase. In the same figure, the magnitude of the combined signal is plotted with its minimum in correspondence of 180°, to emphasize the phase shift between the received signal and the desired one.

#### IV. EXPERIMENTAL RESULTS

As a demonstration of the obtained results, in Fig. 6 the efficiency at 2 GHz for different auxiliary phase settings, highlighted with different colors, is shown. The points associated with the highest efficiency values, for each level of output power, are selected and this process has been repeated for different frequencies within the DPA bandwidth. As an example, results are presented in Fig. 7 verifying that the improvement of the efficiency given by the phase variation. In the same figure, efficiency and gain of single and dual-input DPAs are plotted together. Marker colors identify the phase values highlighting the corresponding improvement.

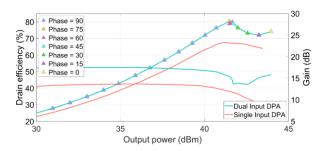


Fig. 7 Single and Dual-input DPA drain efficiency (on the left) and gain (on the right) comparison at 2.1 GHz (measured).

The dual-input DPA shows a maximum efficiency always higher than the single-input DPA. The first part of the curve has a constant phase of  $90^{\circ}$ . Then, to preserve a high efficiency, it is necessary to decrease the phase up to  $0^{\circ}$ . It can be noted that also the gain is increased, and the curve is not smooth. This is due to the fact that a finer measurement grid should have been done to get a more smooth profile, especially at higher output power levels.

#### V. CONCLUSION

The dual-input DPA architecture, if well and fine-tuned, can reach significantly higher efficiencies (up to 5-6%) than the single-input DPA. The single-input DPA architecture is however, cheaper and easier to use since it does not need any additional circuitry at the input, allowing a connection of the RF input directly in the input connector. Nevertheless, its auxiliary path offset is fixed preventing any tuning possibility to optimize its performance. Furthermore, it needs a power divider that introduces additional losses in the circuit, acting negatively on efficiency. The dual-input DPA is more expensive because it needs a control circuit to adjust the phase at the auxiliary amplifier but does not need the power divider avoiding additional losses at the input.

#### ACKNOWLEDGMENT

This work was supported by the EU program Erasmus+ and the Italian Ministry of University and Research (MUR) through the PRIN 2022 Project under Grant 2022REST9A (Next Generation EU). Macom is acknowledged for providing the discrete GaN transistor samples used.

### REFERENCES

- [1] H. Chireix, "High Power Outphasing Modulation," Proc. Inst. Radio Eng, vol. 23, n. 11, pp. 1370-1392, 1935.
- [2] A. A. M. Saleh and D. C. Cox, "Improving the Power-Added Efficiency of FET Amplifiers Operating with Varying-Envelope Signals," in IEEE Transactions on Microwave Theory and Techniques, vol. 31, no. 1, pp. 51-56, Jan. 1983.
- [3] F. F. Tafuri, "Linearity and Efficiency Enhancement Techniques for Mobile Communication Power Amplifiers," Aalborg University, 2014.
- [4] F. Giannini, P. Colantonio and R. Giofré, "The Doherty Amplifier: Past, present & future," 2015 Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMiC), Taormina, Italy, 2015, pp. 1-6.
- [5] H. Zhou, H. Chang e C. Fager, "Symmetrical Doherty power amplifier with high efficiency and extended bandwidth," 2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), pp. 1-3, 2023