A 10 W GaN/Si Doherty Power Amplifier Designed for 15 GHz 6G Band with 8 dB Backoff Efficiency

A 10 W GaN/Si Doherty Power Amplifier Designed for 15 GHz 6G Band with 8 dB Backoff Efficiency

Hossein Zaheri, Rob Vissers, Han Zhou, Gregor Lasser
Microwave Electronics Laboratory, MC2
Chalmers University of Technology
Gothenburg, Sweden
{zaheri, robvis, han.zhou, gregor.lasser}@chalmers.se

***Abstract*—This paper presents the design and implementation of a 10 W GaN-on-Si Doherty Power Amplifier (DPA) for operation in the 15 GHz 6G band. The DPA was fabricated using Infineon's RF GaN-on-Si MMIC process. An experimental (simulation) result shows a peak PAE of 30–37%, and 22–27% PAE at 8 dB backoff, 10 dB gain, and 2 GHz bandwidth. Thermally limited CW measurements confirmed high back-off efficiency with 24% PAE at 29 dBm output power at 14 GHz.**

***Index Terms*—6G, Backoff Efficiency, Doherty Power Amplifier, Gallium Nitride on Silicon, Ku Band.**

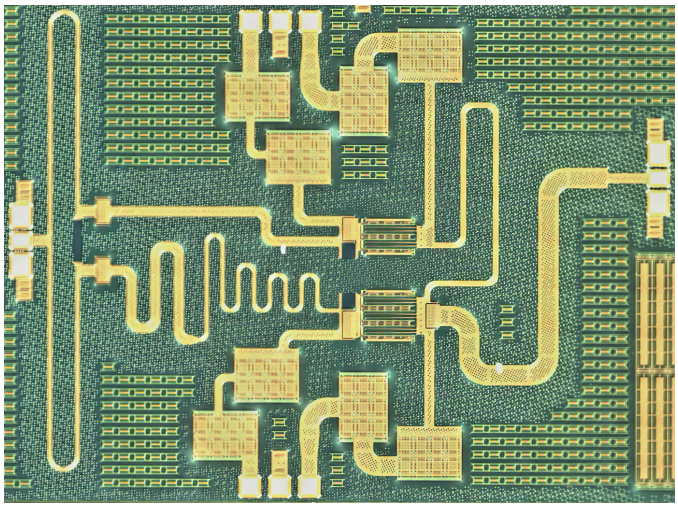
I. Introduction

The development of sixth-generation (6G) communication systems requires power amplifiers (PAs) that meet strict demands in efficiency, linearity, bandwidth, and manufacturing expenses. As the 6G spectrum expands into newer frequency ranges, the 7–15 GHz range is necessary to achieve the capacity-demanding use cases in future 6G networks and enables coverage and mobility that will be the main requirements for most 6G use cases [1]. Modern communication systems use spectrally efficient signals with high peak-to-average power ratio (PAPR). While maintaining high efficiency at large output power backoff levels is mandated, this becomes especially challenging at higher frequencies such as the 15 GHz band.

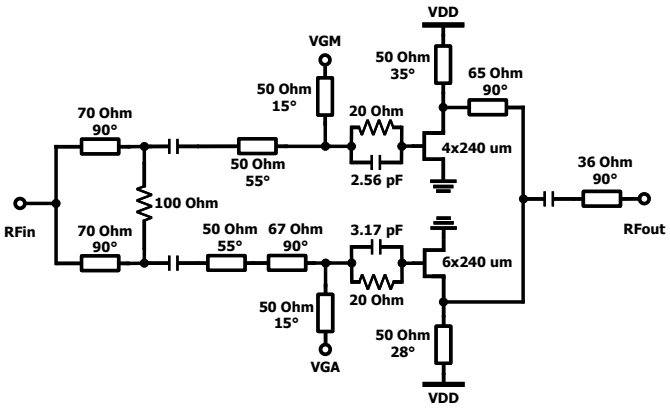
The DPA architecture has been one of the leading solutions that achieves high efficiency at large backoff levels using a load modulation technique. Despite having well-known drawbacks, such as limited bandwidth, DPAs are still popular for their simplicity and compactness [2].

While GaN-on-SiC DPAs are widely used in base stations, GaN-on-Si appears as a strong alternative due to its more practical and cost-efficient manufacturing process. Infineon's latest RF GaN-on-Si technology shows progress, especially in gain and bandwidth. These improvements are primarily due to a novel field-plate design in the active devices. Compared to older generations, this technology offers a 3 to 4 dB increase in gain, reduced frequency dispersion, lower parasitic feedback capacitances (Cgd) for improved stability, that is in favor of designing DPAs, and beneficial to reach the demands in 6G base stations.

This work was funded by ALL2GaN. The ALL2GaN Project (Grant Agreement No. 101111890) is supported by the Chips Joint Undertaking and its members including the top-up funding by Austria, Belgium, Czech Republic, Denmark, Germany, Greece, Netherlands, Norway, Slovakia, Spain, Sweden and Switzerland.



(a)



(b)

Fig. 1: Die photograph (a) and the schematic (b) of the 15 GHz asymmetrical Doherty power amplifier fabricated on Infineon's GaN-on-Si process with area of 3.3×2.4 mm^2. The transmission lines are reported with the characteristic impedance and the electrical length at 15 GHz.

This paper presents the design and implementation of a DPA at 15 GHz frequency band, with 8 dB backoff efficiency suitable for next generation base stations. The DPA circuit

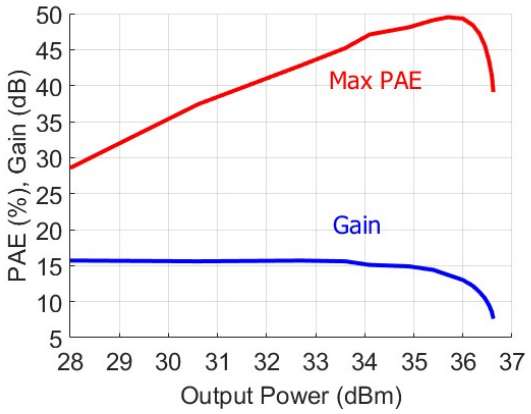


Fig. 2: Maximum PAE and the corresponding gain vs. output power for the $4 \times 240\ \mu m$ device biased at class-B, extracted from loadpull data.

was fabricated on Infineon's GaN-on-Si RF MMIC process. Fig. 1a shows the layout picture of the DPA with area of $3.3 \times 2.4\ mm^2$.

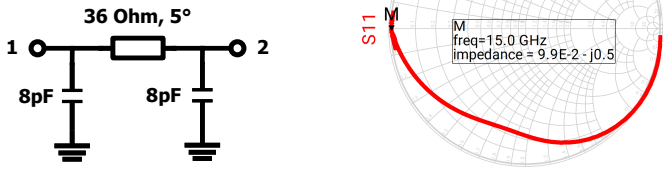
II. Design

To design the Doherty to have a peak in power added efficiency (PAE) at 8 dB output power backoff, a straightforward way is to use the ratio given in (1). Where Γ is the ratio between the devices, which in theory is the reversed ratio between optimum loads for the devices. And ε_b is the output voltage backoff in linear form that is $\varepsilon_b = 0.4$ for the required 8 dB Doherty structure. This will give a $\Gamma = 1.5$ [3].

$$\Gamma = \frac{I_p}{I_M} = \frac{1 - \varepsilon_b}{\varepsilon_b} \tag{1}$$

Fig. 2 depicts the loadpull simulation results on a $4 \times\ 240\ \mu m$ transistor with swept input power level, plotting the PAE and gain at the load which gives the maximum PAE, while the device is biased at the class-B configuration. This shows that the $4 \times 240\ \mu m$ device with maximum output power of 36 dBm is a good choice for the main amplifier of the Doherty that in loadpull can have 45% PAE at the desired backoff level (32 dBm). Therefore a $6 \times 240\ \mu m$ device is used to keep the required ratio from (1) and the required 40 dBm total output power at peak.

Silicon as substrate increase the loss of transmission lines compared to silicon carbide, and using complex passive circuits with additional transmission lines, especially at the power amplifier output, can cause significant power loss and reduce the efficiency. Therefore, minimum number of components were used in this work for matching and the Doherty combiner. As shown in Fig. 1b, after stabilizing the devices using parallel RC networks on the gate, short circuited stubs were used at the input and output of the main and auxiliary amplifiers to compensate the imaginary part of the output admittances. After this, the optimum loads for main and auxiliary amplifiers are 65 Ω and 43 Ω respectively at peak. Therefore, with a 65 Ω, 90° transmission line as the impedance transformer, a load of 65 Ω × ε_b = 26 Ω is required for the Doherty. This is then matched to 50 Ω using a 36 Ω , 90° transmission line.



(a) (b)

Fig. 3: The bypass capacitance used at the end of gate short stub (a) schematic and (b) S_{11} with port 2 open.

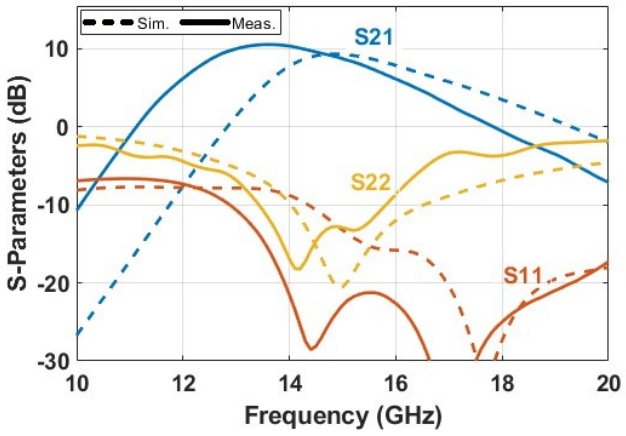
At the input of the main amplifier, with the proper choice of the stability RC values, we can maintain a 50 Ω-matched input using only one short stub. For the auxiliary amplifier on the other hand, after compensating the imaginary part of the admittance with a short stub, the input impedance is 90 Ω, which is then matched to 50 Ω using a quarter wavelength transmission line with characteristic impedance of 67 Ω. This transmission line at the same time compensates the phase difference of the Doherty output combiner.

A symmetrical Wilkinson divider is used at the input of the Doherty to prevent extra loss for the main branch and compensate for its compression at peak power level. Two 50 Ω lines were used to connect the Wilkinson to the amplifiers while the one at the auxiliary is meandered to have the same length.

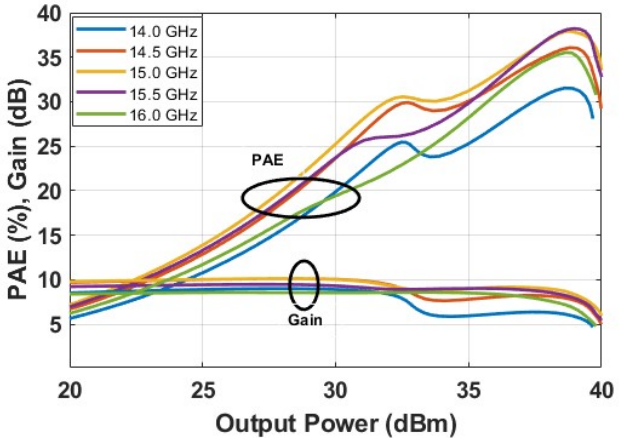
The successful use of short circuited stubs for matching requires proper bypass capacitors to achieve good RF-grounds at 15 GHz. However too large capacitors will have low self-resonant frequencies. Fig. 3 shows the bypass capacitor used at the drain supply that is followed by a short transmission line and another capacitor with the same size. Each capacitor is a 2 × 4 matrix of 5 × 5 fingers of Metal-insulator-metal (MIM) capacitors, with ground vias between each row and column of the matrix. The S_{11} in the smith figure shows near-short-circuit at 15 GHz which is expected from a proper bypassing. Similar approach was used for the short stub at the gate. Further bypassing is done on a printed circuit board (PCB) for low frequency stability purposes.

III. Results

The drain supply for both devices are set to 28 V for S-parameters, and gate bias for main and auxiliary amplifiers are set to -2.7 V and -4.2 V respectively. Fig. 4a shows the S-parameter results for the Doherty, where the operational bandwidth of 2 GHz is seen from S_{21}. A 1 GHz shift to lower frequencies is observed in the measurements compared to simulation. Fig. 4b shows the simulated PAE and large signal gain of the DPA versus the output power with 28 V supply voltage and Fig. 5 shows the simulated PAE and delivered power vs. frequency with 28 V supply voltage. The measurements were done in continuous-wave (CW). The chip was mounted on a 0.5 mm thick copper substrate together on

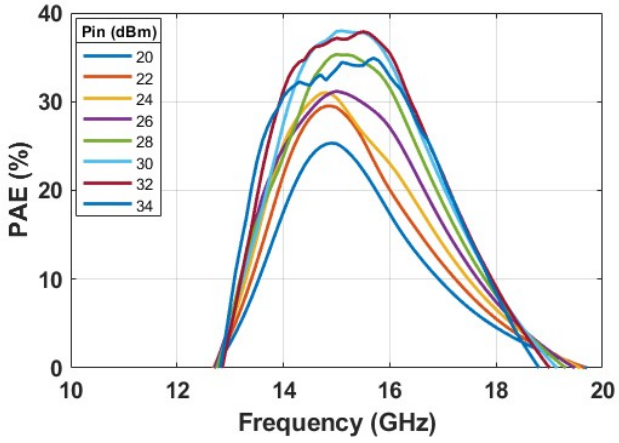


(a)

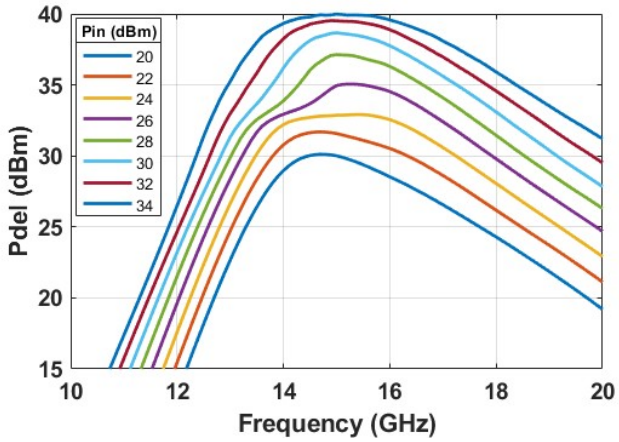


(b)

Fig. 4: The S-parameters simulation results versus measurements (a) and large signal simulation results (b) with 28 V supply voltage for the DPA.



(a)



(b)

Fig. 5: Simulated PAE (a) and output power (b) vs. frequency with 28 V supply voltage at different input power levels.

PCB (Fig. 6). Due to thermal reasons we could not obtain CW data above 29 dBm of output power (Fig. 7), so we here present results for a reduced drain voltage of 25 V with reduced drive power for the measurements. The PA will be characterized with a pulsed setup in a later stage. Large signal results also show the frequency shift, while approving the backoff power added efficiency from simulation. Results show this circuit has a reasonable gain of 10 dB, despite having only one stage of amplifiers for the main and auxiliary branches. The PAE at the 29 dBm output level is 18-24%. In simulation the peak PAE happens at 39 dBm output power, and the maximum output power is 40 dBm.

The results are compared with other GaN MMIC DPAs on silicon and silicon carbide substrates in TABLE I. The comparison highlights strong competitiveness with the state of the art GaN DPAs on both substrates.

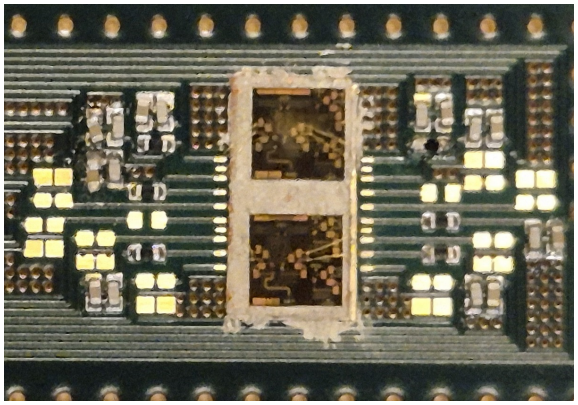


Fig. 6: DPA MMIC mounted on 0.5 mm thick copper sheet on PCB to improve heat conduction. DC pads are wirebonded to PCB, and the RF pads are directly probed. Two chips are mounted in the picture.

IV. Conclusion

The presented 10 W Doherty Power Amplifier was designed and implemented in an experimental RF GaN-on-Si process

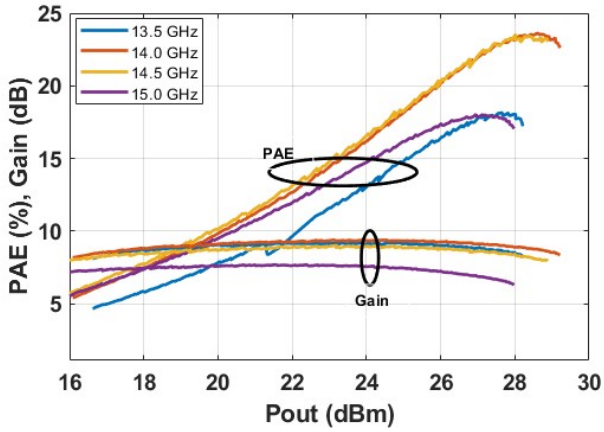


Fig. 7: Large signal measurement results with 25 V supply voltage for the DPA.

TABLE I: Comparison with the other GaN MMIC Doherty amplifiers

Ref.	**[4]**	**[5]**	**[2]**	**[6]**	**[7]**	***T.W.**
Substrate	Si	SiC	SiC	SiC	SiC	Si
Freq. (GHz)	17.3–20	14–15	10–14	14.5–17.2	10.7–12.7	14–16
P_{sat} (dBm)	38	36	34	34	43	40
PAE$_{peak}$ (%)	34–36	27	28–38	20–25	35–45	30–37
PAE$_{6dB}$ (%)	20–25	22	21–31	20–25	25–33	22–27
PAE$_{8dB}$ (%)	20–22	20	15–17	18–20	–	22–27
Gain (dB)	20	7	15	18	25	10

*This Work, simulation data.

from Infineon, using minimal number of passive components to avoid additional loss with silicon as substrate. This DPA shows the possibility of replacing the costly GaN-on-SiC MMIC technologies with the more cost-efficient process of GaN-on-Si for the next generation communication systems. However, the thermally less conductive substrate implies limitations, especially in terms of CW testing of dense MMIC PAs as was observed experimentally. CW measurements confirm a good backoff PAE of 24% at 29 dBm output power. According to simulation results DPA shows a peak PAE of up to 37%, reasonable PAE of up to 27% at 8 dB output backoff level, and over a 2 GHz operational bandwidth suitable for 6G base stations.

REFERENCES

[1] Ericsson, "6G spectrum: Enabling the future mobile life beyond 2030," Ericsson White Paper, May 2024.

[2] H. Zhou, V. Åberg, H. Chang, and C. Fager, "A GaN MMIC wideband continuous-mode Doherty power amplifier for 6G FR3 cmWave applications," in *Proc. 19th Eur. Microw. Integr. Circuits Con. (EuMIC)*, 2024, pp. 170–173.

[3] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*, ser. Artech House microwave library. Artech House, 2002, pp. 33–72.

[4] F. Costanzo, V. Camarchia, N. B. Carvalho, P. Colantonio, A. Piacibello, R. Quaglia, V. Valenta, and R. Giofrè, "A GaN MMIC stacked Doherty power amplifier for space applications," in *Proc. IEEE Topical Conf. RF/Microwave Power Model. Radio Wireless Appl. (PAWR)*, 2022, pp. 29–31.

[5] R. Quaglia, V. Camarchia, J. J. Moreno Rubio, M. Pirola, and G. Ghione, "A 4-W doherty power amplifier in gan mmic technology for 15-GHz applications," *Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 365–367, 2017.

[6] G. Naah, A. Piacibello, V. Camarchia, P. Colantonio, and R. Giofré, "Low-bias-complexity Ku-band GaN MMIC Doherty power amplifier," in *IEEE/MTT-S International Microwave Symposium - IMS*, 2022, pp. 1041–1043.

[7] S. Fakhfakh, T. Huet, A. L. Brun, B. Lefebvre, J.-F. Villemazet, E. Richard, and A. Chowdhary, "A 20-Watts, GaN MMIC Doherty power amplifier for Ku-band satellite communications," in *Proc. 18th Eur. Microw. Integr. Circuits Con. (EuMIC)*, 2023, pp. 345–348.