



RF-DAC-based PA Pre-Distortion using Expanding Non-Linear RF-DAC Scaling

Downloaded from: <https://research.chalmers.se>, 2025-06-08 17:16 UTC

Citation for the original published paper (version of record):

Åberg, V., Saad, P., Hou, R. et al (2024). RF-DAC-based PA Pre-Distortion using Expanding Non-Linear RF-DAC Scaling. 2024 19th European Microwave Integrated Circuits Conference, EuMIC 2024. <http://dx.doi.org/10.23919/EuMIC61603.2024.10732339>

N.B. When citing this work, cite the original published paper.

RF-DAC-based PA Pre-Distortion using Expanding Non-Linear RF-DAC Scaling

Victor Åberg^{#1}, Paul Saad^{\$2}, Rui Hou^{\$3}, Han Zhou^{#4}

[#]Chalmers University of Technology, Gothenburg, Sweden

^{\$}Ericsson, Stockholm, Sweden

¹abergv@chalmers.se, ²paul.saad@ericsson.com, ³rui.hou@ericsson.com, ⁴han.zhou@chalmers.se

Abstract— We present an RF-DAC-based transmitter that uses an expanding characteristic to linearize the PA. Implemented in 22 nm FDSOI CMOS, the transmitter operates with a carrier frequency of 12.5 GHz, achieving a sample rate of 7 GS/s. Measurements with >3.5 GSym/s wideband modulated 64QAM SC and OFDM signals show $\text{EVM}_{\text{RMS}} < 3.83\%$ and $\text{ACPR} < -32.4\text{ dBc}$ when using the RF-DAC-based predistortion. The 1 dB compression point is increased by 4.2 dB. For multi-GHz wideband modulated signals, a >0.6 percent unit EVM improvement and a >2.5 dB ACPR improvement are observed.

Keywords— CMOS, PA, RF-DAC-based predistorter, RF-IQ modulator, Wideband

I. INTRODUCTION

The broad and continuous spectra available at centimeter-wave (cmW) and millimeter-wave (mmW) frequencies are increasingly used in wireless networks. The 5G mmW bands are around 3 GHz wide [1], and for 6G, multiple bands, >1 GHz wide, in the 7–15 GHz range, are proposed [2]. Additionally, massive multiple-input-multiple-output (mMIMO) arrays at these frequencies use large numbers of densely packed antennas and transmitters with strict energy and thermal budgets [3]. To support spectrum-efficient modulation formats, these transmitters must be highly linear.

RF-DACs allow two critical functions to be realized in a single block, combining digital-to-analog (D/A) conversion and up-conversion [4], [5]. However, the output power is limited by the low supply voltages tolerated in modern CMOS technologies. For higher output power, or in large arrays where a dedicated RF-IQ modulator per antenna element may be infeasible, PAs still play an important role in the transmitter.

The inverse relationship between PA compression level and linearity is well known. To fulfill linearity requirements, the PA either has to operate at significant power back-off, or a predistorter (PD) is required to compensate for its non-linear characteristic. Predistortion is typically realized either using an analog PD (APD) [6]–[8], or a digital PD (DPD) [9]. APDs are generally wideband but suffer from significant losses and large footprints. DPDs perform the linearization in the digital domain, before the D/A conversion, allowing the entire transmitter to be linearized. They are adaptable but require computations to be performed on every sample, at the full modulator sample rate [9]. The cost of using DPD in a wideband mMIMO array will be significant [3].

Segmented non-linear self-linearized RF-DACs have been realized at a few gigahertz (single RF-DAC) [10], and at

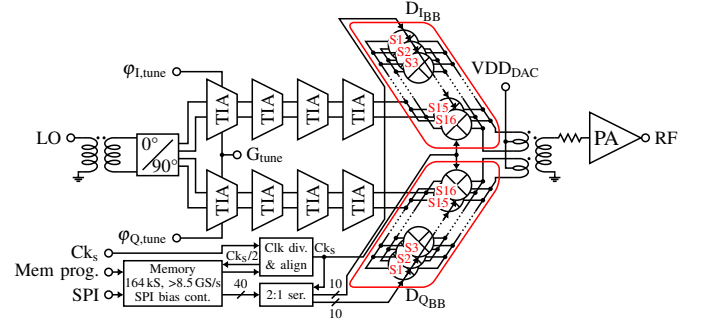


Fig. 1. Transmitter block diagram showing the full RF path and supporting circuitry for one of the two realizations. The RF-DACs are encircled in red.

mmW frequencies (complete IQ modulator) [11]. Predistortion of PAs using non-linear RF-DACs has been demonstrated by simulations in [12].

In this paper, we present the first realization of a fully CMOS integrated transmitter where segmented RF-DACs, having an expanding characteristic, are used for PA predistortion. A reference implementation using uniform RF-DACs is also included. Measurements show that the RF-DAC-based PD increases the output-referred 1 dB compression point by 4.2 dB. With modulated signals, the EVM is improved by >0.6 percent unit and the ACPR by >2.5 dB as the same output power level.

II. DAC-BASED LINEARIZATION

In a DAC-based PD, segmented RF-DACs, see Fig. 1, having an expanding scaling, realize the inverted AM/AM characteristic for the circuit being linearized. Figure 2a, shows the characteristics for the PA (blue), the expanding RF-DAC (orange), that, when combined with the PA, give a linear output (yellow). As the RF-DACs also suffer from compression, the scaling will compensate for the combined RF-DAC and PA compression; observe the difference between the cumulative DAC width (purple) and the RF-DAC output.

Although the expanding characteristic is realized using a segmented scaling that is fixed in hardware, there is still room for significant tuning [12]. The expanding characteristic is tuned by the LO amplitude and/or the RF-DAC supply voltage. In a Cartesian modulator, AM/PM compensation may be realized by activating unit cells in the Q(I)-DAC based on inputs to the I(Q)-DAC, shifting the phase of the output signals.

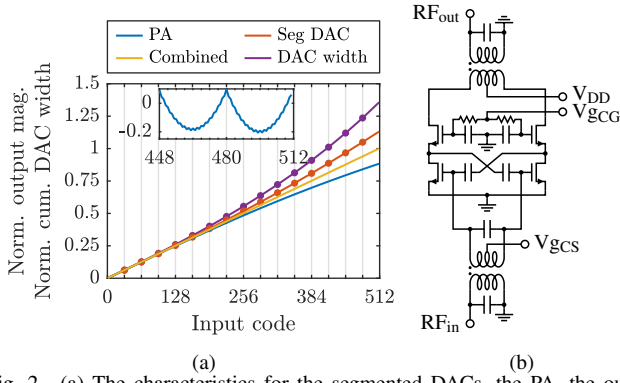


Fig. 2. (a) The characteristics for the segmented DACs, the PA, the output when they are combined, and the cumulative DAC width. The inset shows the integral non-linearity (in LSB) for the combined output. (b) Schematic for the PA; transistors have a length of 20 nm and a width of $8 \times 40 \times 1 \mu\text{m}$.

III. DESIGN

A complete transmitter block diagram is shown in Fig. 1. This includes the quadrature LO generation, the two 10b RF-DACs, the PA, and the on-chip waveform memory. Two transmitters have been realized; one uses an expanding segmented RF-DAC scaling to realize PD, while the other, used as a reference, uses a uniform scaling.

A. Quadrature LO generation

Accurate quadrature LO signals are of importance for precise generation of high-order QAM signals. The large capacitive load presented by the RF-DACs (a large total transistor width combined with the LO distribution to all unit cells) makes the generation of these signals challenging.

Here, the quadrature phases are generated using a current mode logic (CML) divider and then buffered using four-stage trans-impedance amplifier (TIA) buffers. Differential series inductors separate all stages [4]. The first TIA stage is tunable to allow control of the LO amplitude (to tune the expanding characteristic), and to reduce amplitude/phase imbalance.

B. Segmented RF-DAC

To realize the expanding characteristic, the RF-DACs are divided into 16 segments, each with a unique scale factor. The number of segments used is a trade-off between the control of the shape of the expanding characteristic and logic complexity.

For efficient operation at high sample rates, fast and minimalistic segment control logic are vital. The segment logic, shown in Fig. 3, is based on [11], with additional logic for the AM/PM compensation (encircled in red). The two logic gates realizing Seg_{en} and Seg_{on} are unique in each segment; the former is used to enable the segment while the latter activates all cells in the segment. The AM/PM compensation activates one LSB cell, in the corresponding segment in the other DAC, every 4th, 8th, or 16th code, depending on the L_P and M_P settings; the sign is set by Inv_S .

A 7.5 dB attenuator is placed before the PA to match the RF-DACs output power to the PA input power requirement. Without it, we would be able to linearize a PA requiring a significantly higher input power than the one used in this work.

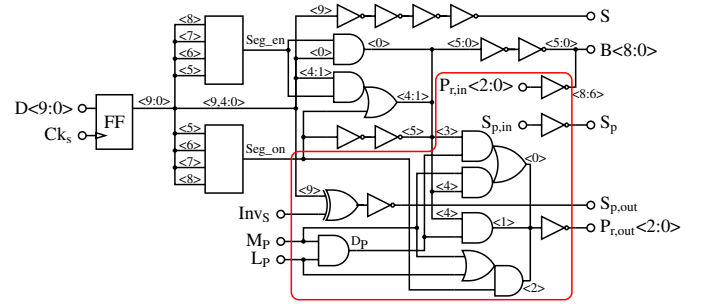


Fig. 3. Schematic of the segment control logic. The logic for AM/PM compensation is encircled in red.

C. Power amplifier

The power amplifier is designed as a differential pair with stacking and neutralization, see Fig. 2b. The differential configuration is necessary to mitigate parasitic crosstalk. The stacking of common-source (CS) and capacitively degenerated common-gate (CG) transistors allows the supply voltage to be doubled without degrading reliability. Neutralization of the CS pair improves the stability and gain at the high frequencies.

D. Matching networks

The impedance matching for both the PA and the divider input is realized using interleaved baluns located in the topmost metal layers. The balun connected to the output of the RF-DACs uses two individual primary coils, one per RF-DAC to enhance isolation, reducing the cross-modulation distortion. In addition to the single-ended/differential conversion, the balun inductance is used to resonate out circuit capacitance. MOM capacitors are used to tune the matching network.

E. Test circuitry

To evaluate the transmitters, various digital baseband I/Q signals must be provided at high sample rates. A 164 kS, >8.5 GS/s SRAM memory is connected to each transmitter, generating the signal on-chip. On-chip, digitally programmable bias sources are used to reduce the pad count.

IV. EXPERIMENTAL RESULTS

A chip photo is shown in Fig. 5, showing both transmitter realizations (using segmented and uniform RF-DACs), the waveform memory, and the isolated PAs. The chip is fabricated using GlobalFoundries 22 nm FDSOI CMOS and measures $2.5 \text{ mm} \times 2 \text{ mm}$. Each transmitter occupies $290 \mu\text{m} \times 1600 \mu\text{m}$.

Measurements were performed on both transmitters and on the standalone PA. All measurements were performed using a Keysight PNA-X vector network analyzer. The coplanar LO and RF pads are used as the calibrated reference plane.

A. Continuous-wave measurements

Figure 4a summarizes the static performance across carrier frequencies. Here, the peak output power (P_{SAT}), the image rejection ratio (IRR), and the integral non-linearity (INL) are shown for the transmitter using segmented RF-DACs. A peak output power of 15.8 dBm is measured at 11.5 GHz.

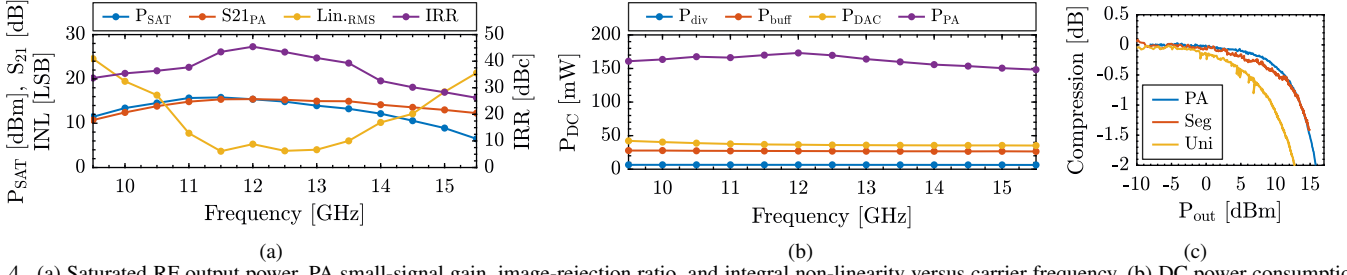


Fig. 4. (a) Saturated RF output power, PA small-signal gain, image-rejection ratio, and integral non-linearity versus carrier frequency. (b) DC power consumption for the divider, the TIA buffers, the RF-DAC (excluding digital circuits), and the PA versus carrier frequency. (c) Compression versus output power for the standalone PA (including attenuator), and both transmitters. For the transmitters, the same input code is simultaneously provided to both RF-DACs.

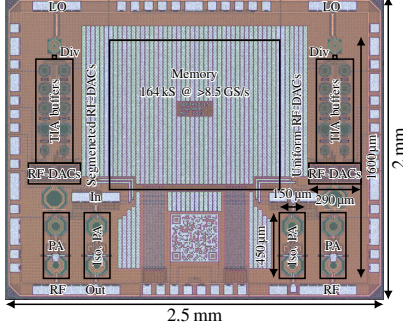


Fig. 5. Chip photo showing both transmitter realizations (using segmented and uniform RF-DACs), the standalone PAs, and the waveform memory. The TIA buffers and PA dominate the transmitter area while the waveform memory dominates the chip area.

The continuous wave (CW) 3 dB bandwidth is between 10–13.5 GHz for the full transmitter and 10.1–15.5 GHz for the PA. An IRR >35 dBc is measured across 10–14 GHz. The INL is measured using TIA bias settings optimized for 12 GHz. With a fixed TIA bias, the LO amplitude will vary with frequency, degrading the INL at both low and high frequencies. Tuning the bias makes it possible to achieve a low INL across the range. The small-signal PA gain (including attenuator) is also plotted here. The DC power consumption for the divider, the TIA buffers, the RF-DACs (excluding the digital circuits), and the PA is shown versus carrier frequency in Fig. 4b.

The compression is plotted versus output power for the PA, and both transmitters in Fig. 4c. For the transmitters, the same input code is here provided to both RF-DACs. With the segmented RF-DACs, the 1 dB compression point is increased by 4.2 dB compared to using uniform RF-DACs. No improvement is observed compared to the standalone PA. Individually applying the expansion to each quadrature component brings limited linearization capabilities when both RF-DACs are active; the INL is <5 LSB when only a single RF-DAC is used.

B. Wideband modulated measurements

The wideband modulated performance is evaluated for both transmitter realizations using both 64QAM single-carrier (SC) signals, up-sampled 2 \times using a digital RRC filter (factor 0.1), and multiple aggregated 400 MHz OFDM signals at 12.5 GHz.

In Fig. 6, constellation diagrams and output spectra are shown for 64QAM SC signals using both transmitter configurations. Similarly, Fig. 7 shows measurements, for 10 aggregated 400 MHz 64QAM OFDM signals. The LO magnitude for the reference transmitter is tuned such that the same output power is achieved for both transmitters. Due to measurement limitations, the ACPR reported for the SC signals is calculated using the noise power in a 400 MHz adjacent channel scaled to the signal bandwidth; the actual ACPR is likely better. In the constellation diagrams, we can notice some compression in the corners. This cannot be handled when applying the linearization to each quadrature component individually, and this residual non-linearity will limit the ACPR. For both SC and OFDM signals, the EVM is limited by gain flatness and memory effects.

With modulated signals at 7 GS/s, the PA consumes 148 mW, and the RF-DACs 8.2 mW for the analog parts and 11.5 mW/(GS/s) for the digital circuits. Divider and TIA buffers have the same power consumption as in the CW case.

Table 1 summarizes and compares the performance for both transmitters against other state-of-the-art RF-DAC-based transmitters. With RF-DAC-based PD, the output-referred 1 dB

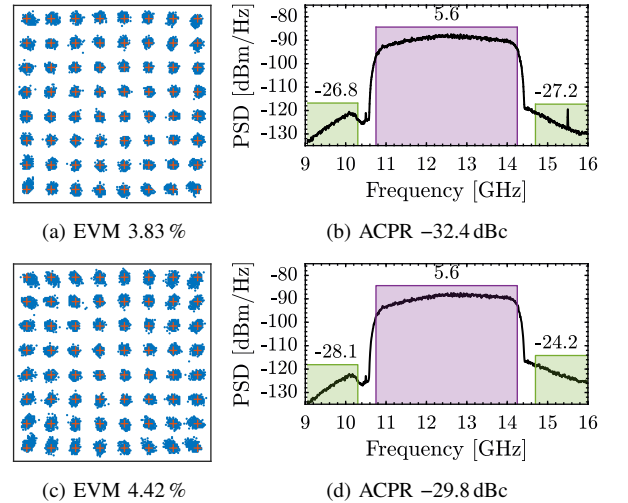


Fig. 6. Constellation diagrams and output spectra for SC-64QAM signals using segmented RF-DACs (a) and (b), and uniform RF-DACs (c) and (d). All achieve a data rate of 21 Gb/s with a BER <10⁻⁴, using a sample rate of 7 GS/s. Channel power presented in dBm.

Table 1. Performance comparison with published state-of-the-art RF-DAC-based transmitters supporting at-least 64QAM.

	This work				[4]	[5]	[11]	
	Segmented		Uniform					
Technology	22 nm SOI				45 nm SOI	28 nm	22 nm SOI	
Topology	Cartesian (expanding) + PA				Cartesian	Cartesian	Cartesian (expanding)	
Resolution [b]	2×10				2×6	2×10	2×10	
Frequency [GHz]	10–13.5				18–32	20–32	20–26	
Peak P _{SAT} [dBm]	15.8		14.6		19.9	19.02	3.47	
Modulation format	64QAM SC	64QAM OFDM ¹	64QAM SC	64QAM OFDM ¹	64QAM SC	64QAM SC	64QAM SC	64QAM OFDM ²
Sample rate [GS/s]	7		7		2 ³	2	11	9
OSR	2	-	2	-	1	4	5	-
EVM [% _{rms}]	3.83	3.61	4.42 ⁴	4.35 ⁴	4	3.59	6.42	6.43
ACPR [dBc]	-32.4 ⁵	-34.6	-29.8 ^{4,5}	-31.7 ⁴	-	-33.6	-28.9	-28.4
Data rate [Gb/s]	21	21.3	21	21.3	12	3	13.2	8.52
DPD	Expanding DAC scaling		No		Yes	2D LUT	3 rd order memoryless	
Area [mm ²]	<0.47		<0.47		2.41 ⁶	0.2	<0.47	

¹ 10 aggregated 400 MHz channels. ² 4 aggregated 400 MHz channels. ³ Highest sample rate achieving at least 64QAM. ⁴ Tuned to achieve the same output power as for the segmented DAC. ⁵ Computed for 400 MHz and scaled to signal bandwidth. ⁶ Including pads.

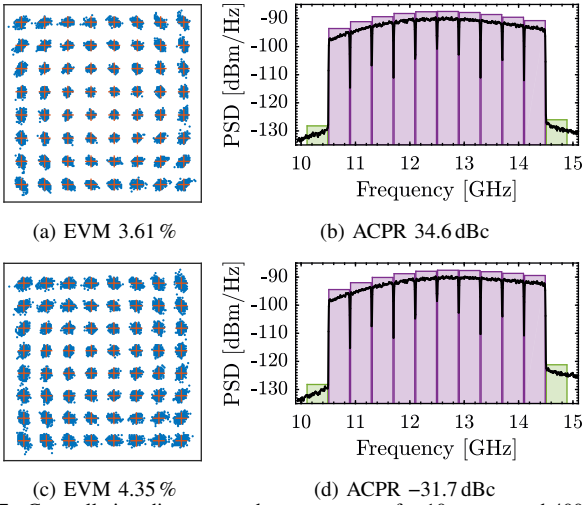


Fig. 7. Constellation diagrams and output spectra for 10 aggregated 400 MHz 64QAM OFDM channels using segmented RF-DACs (a) and (b), and uniform RF-DACs (c) and (d). All achieve a data rate of 21.3 Gb/s with a BER $<10^{-4}$, using a sample rate of 7 GS/s and an accumulated channel power of 0.9 dBm.

compression point is increased by 4.2 dB. With wideband modulated signals, the RF-DAC-based PD improves the EVM by >0.6 percent unit and the ACPR by >2.5 dB compared to the reference transmitter, while achieving the same output power.

V. CONCLUSION

We have presented a linearization concept that purely is based on the segmented RF-DAC scaling. The RF-DAC-based PD is evaluated against a transmitter using uniform RF-DACs, showing 4.2 dB improvement in the 1 dB compression point. A >0.6 percent unit EVM improvement and a >2.5 dB ACPR improvement are observed for multi-GHz wide 64QAM SC and OFDM signals, at the same output power level.

ACKNOWLEDGMENT

This research has been carried out in Gigahertz-ChaseOn Bridge Center in a project financed by Chalmers University of

Technology, Ericsson, Gotmic, Infineon, Kongsberg, Saab, and UniqueSec. We thank GlobalFoundries for chip fabrication, and Keysight for the PNA-X software.

REFERENCES

- [1] *Base station (BS) radio transmission and reception*, 3GPP, 2021.
- [2] E. Semaan *et al.*, “6G spectrum - enabling the future mobile life beyond 2030,” Ericsson, White Paper, 2023. [Online]. Available: <https://www.ericsson.com/en/reports-and-papers/white-papers/6g-spectrum-enabling-the-future-mobile-life-beyond-2030> (visited on 12/13/2023).
- [3] H. Huang, J. Xia, and S. Boumaiza, “Novel parallel-processing-based hardware implementation of baseband digital predistorters for linearizing wideband 5G transmitters,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 4066–4076, 2020.
- [4] S. Shopov, N. Cahoon, and S. P. Voignescu, “Ultra-broadband I/Q RF-DAC transmitters,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5411–5421, 2017, ISSN: 0018-9480.
- [5] H. J. Qian *et al.*, “A 20-32-GHz quadrature digital transmitter using synthesized impedance variation compensation,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1297–1309, 2020, ISSN: 1558-173X.
- [6] J. Potschka *et al.*, “A highly linear and efficient 28 GHz stacked power amplifier for 5G using analog predistortion in a 130 nm BiCMOS process,” in *IEEE Asia-Pacific Microwave Conference (APMC)*, 2019, pp. 920–922.
- [7] N. Deltimple, M. Potereau, and A. Ghiotto, “Fully integrated reflector-based analog predistortion for Ku-band power amplifiers linearization,” in *IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 363–368.
- [8] J.-H. Tsai *et al.*, “A 60 GHz CMOS power amplifier with built-in pre-distortion linearizer,” *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 12, pp. 676–678, 2011.
- [9] A. Katz, J. Wood, and D. Chokola, “The evolution of PA linearization: From classic feedforward and feedback through analog and digital predistortion,” *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 32–40, 2016.
- [10] M. Hashemi *et al.*, “An intrinsically linear wideband polar digital power amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, 2017.
- [11] V. Åberg *et al.*, “Ultrawideband RF-IQ modulator using segmented nonlinearly scaled RF-DACs and nonoverlapping LO signals,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 5, pp. 1899–1910, 2023.
- [12] V. Åberg *et al.*, “RF PA predistortion using non-linear RF-DACs,” in *IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2022, pp. 1–6.