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Sohrab Mohtat
Department of Electrical Engineering
Chalmers University of Technology
Göteborg, Sweden
sohrab.mohtat@chalmers.se

Massimo Bongiorno
Department of Electrical Engineering
Chalmers University of Technology
Göteborg, Sweden
massimo.bongiorno@chalmers.se

Mebtu Beza
Department of Electrical Engineering
Chalmers University of Technology
Göteborg, Sweden
mebtu.beza@chalmers.se

Jan R. Svensson
Hitachi Energy Research
Hitachi Energy
Västerås, Sweden
jan.r.svensson@hitachienergy.com

***Abstract*—The Double Wye Modular Multilevel Converter (YY-MMC) with energy storage connected on the DC-link is increasingly utilized in grid applications to facilitate renewable energy sources integration. This paper investigates the impact of pole-to-pole DC voltage and circulating current on the design requirements of a Full-Bridge YY-MMC (FB-YY-MMC). Starting with providing an overview of YY-MMC configuration and circulating current calculation, this paper tries to identify the optimal pole-to-pole DC voltage and the second-order circulating current amplitude and phase for minimizing the design parameters of the FB-YY-MMC, such as losses, semiconductor ratings, and submodule's capacitor size. Time-domain simulations validate the proposed optimal working points, offering valuable insights for optimizing FB-YY-MMC design requirements in grid applications.**

I. Introduction

Multilevel inverters have become crucial in energy conversion systems due to their advantages such as low voltage total harmonic distortion and small filter size [1]. Consequently, they are widely used in renewable energy systems, high-voltage DC applications, electric vehicles, as well as in grid-connected power electronic systems like active power filters, inverters, uninterrupted power supplies, and vehicle-to-grid connections [2]. Among them, the Modular Multilevel Converter (MMC) offers high efficiency, excellent dynamic performance, and robustness when connected to the weak grids [3]. The Double Wye MMC (YY-MMC) configuration incorporating Energy Storage (ES) on the DC-link have been deployed in grid applications, particularly to facilitate the integration of renewable energy sources [4]. In a YY-MMC configuration, each phase-leg comprises of upper and lower arms, with multiple series-connected submodules (SM) in each arm. These SMs can either be half-bridge (HB) or full-bridge (FB) converters, forming a HB-YY-MMC and FB-YY-MMC, respectively.

YY-MMC is associated with a number of challenges, which are mainly due to the high number of components [5]. With respect to single wye MMC (Y-MMC or cascaded FB converter), the YY-MMC gives the possibility of connecting a centralized ES to the converter common DC-link. However, this converter configuration introduces a circulating current due to the phase difference in SM's capacitor's voltage ripples of the upper and lower arm [6]. This circulating current is usually suppressed in most applications by a circulating current controller to reduce the losses. However, it can also be used to optimize the design parameters of the converter. Another degree of freedom that can be used to optimize the design requirement of the FB-YY-MMC is the pole-to-pole DC voltage. Unlike HB-YY-MMC in which the minimum required pole-to-pole DC voltage depends on the AC grid voltage, in FB-YY-MMC configuration, this parameter can be selected freely. This freedom also allows for further optimization of the converter. For example, [7], [8], and [9] investigate the effect of circulating current on SM's capacitor, current rating of switches, and power losses of HB-YY-MMC. In the references [10], [11], and [12] the effect of pole-to-pole DC voltage on capacitance requirement of a FB-YY-MMC are analyzed. As these previous investigations consider optimization on a given pole-to-pole DC voltage to optimize with respect to the circulating current or vice versa, the results are not optimal for the full spectrum of these two variables.

This paper explores the effect of both pole-to-pole DC voltage and circulating current on a FB-YY-MMC, and suggests the optimal points, which result in minimization of the losses, switch rating, and SM's capacitor size of the converter. First, the topology of the converter with its working principle is introduced. Next, an equation for the second-order circulating current is presented. Then, the design parameters of the converter and their dependence on the pole-to-pole DC

voltage and the second-order circulating current phase and amplitude are presented. Finally, the results of the analysis and some optimal working points of the converter are investigated and verified by time-domain simulations.

II. FB-YY-MMC Topology

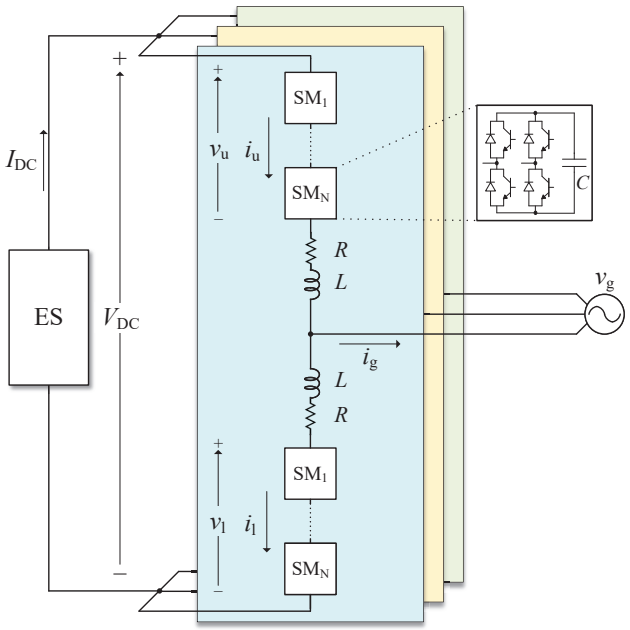


Fig. 1: Grid-connected FB-YY-MMC scheme.

The grid-connected FB-YY-MMC shown in Fig. 1 is composed of three phase-legs, each consisting of an upper and lower arm. There are N series-connected FB SMs and a filter reactor with inductance L and resistance R in each arm. An ES with pole-to-pole DC voltage of V_{DC} is connected to the converter's DC side, and the upper arm and lower arm voltages and currents are denoted as v_u, v_l, i_u and i_l, respectively.

The upper and lower arm currents of a generic phase can be written as

$$i_{u,l} = \pm\frac{i_g}{2} + i_c \tag{1}$$

where i_g is the current exchanged between the converter and the grid, and i_c is the current that circulates between the phase-legs and common DC link of the converter. In sinusoidal steady-state operation of the converter, the circulating current is composed of a DC term, which is assumed to be 1/3 of the DC current coming from the ES (I_{DC}), and even order harmonics that originate from the phase difference between the upper arm and lower arm capacitors' voltage ripples [13]. Therefore, the circulating current can be written as

$$i_c = \frac{I_{DC}}{3} + \sum_{n=2k}^{\infty} I_{cn}\cos(n\omega t + \varphi_{cn}), \quad k = 1, 2, \cdots \tag{2}$$

where I_{cn} and φ_{cn} are the amplitude and phase of the $2k$-order harmonic of the circulating current. It can be found that the dominating harmonic component of the circulating current is the second-order one and the other harmonics have much smaller amplitude [13]. Thus, in this analysis, it is assumed that circulating current is composed of a DC term and a second-order harmonic. Considering this and assuming that i_g is pure sinusoidal with fundamental frequency and amplitude I_g and phase φ_{ig}, the upper and lower arm currents can be found by combining (1) and (2)

$$i_{u,l} = \pm\frac{I_g}{2}\cos(\omega t + \varphi_{ig}) + \frac{I_{DC}}{3} + I_{c2}\cos(2\omega t + \varphi_{c2}) \tag{3}$$

The next step is to determine the second-order circulating current of FB-YY-MMC in steady-state. Similar to what have been done in previous works to caclualte the second-order circulating current for HB-YY-MMC [13], here, I_{c2} and φ_{c2} are found by calculating upper and lower arm capacitors' voltage ripples. The main difference between circulating current calculation for HB-YY-MMC and FB-YY-MMC is an extra parameter for FB-YY-MMC which is called DC modulation index (m_{DC}) in this analysis. While in HB-YY-MMC the DC value of the sum capacitor voltage of the arm is usually considered to be equal to V_{DC} [13] [14], because of the capability of FB SMs in negative voltage generation, the pole-to-pole DC voltage of FB-YY-MMC can be chosen freely [12]. The DC modulation index is thus defined as

$$m_{DC} = \frac{V_{DC}}{V_C^{\Sigma}} \tag{4}$$

where V_C^{Σ} is the DC value of the sum of the capacitor voltage of an arm of the FB-YY-MMC. Assuming the circulating current is only composed of a DC term and a second-order harmonic component according to [13], the FB-YY-MMC second-order circulating current amplitude and phase in sinusoidal steady state operation can then be calculated as

$$I_{c2}e^{j\varphi_{c2}} = \frac{\frac{3m_{DC}}{8\omega}\sin(\varphi_{ig})m_{AC}I_g - j\frac{3m_{DC}^2 - m_{AC}^2}{8m_{DC}\omega}\cos(\varphi_{ig})m_{AC}I_g}{\frac{4CR}{N} + j(\frac{8C\omega L}{N} - \frac{6m_{DC}^2 + 4m_{AC}^2}{12\omega})} \tag{5}$$

where the grid angular frequency and the SM's capacitance are denoted as C and ω, respectively. m_{AC} is the AC modulation index and $m_{AC} = \frac{2V_s}{V_C^{\Sigma}}$ in which V_s is the amplitude of the converter output voltage behind the filter. Here, it is assumed to be pure sinusoidal and equal to

$$v_s = V_s\cos(\omega t) \tag{6}$$

The maximum required arm voltage determines the needed number of SMs. The upper arm and lower arm generated voltages are [6]

$$v_{u,l} = \frac{V_{DC}}{2} \mp v_s \tag{7}$$

The number of SMs is found by dividing the maximum value of (7) by SM's rated voltage (V_n) [14].

$$N = \text{ceil}\left(\frac{\frac{V_{DC}}{2} + 1.05\widehat{V}_g\left(1 + \Delta V_g + I_{g,pu}\frac{Z_f}{2}\right)}{V_n}\right) \tag{8}$$

where Z_{f} is the per-unit value of the arm filter, $I_{\mathrm{g,pu}}$ is the per-unit value of the output rated current which is equal to 1, ΔV_{g} is the peak grid voltage variation, and $\widehat{V}_{\mathrm{g}}$ is the grid maximum voltage. It should be mentioned that in (8) a 5% margin is considered to guarantee a suitable dynamic behavior in the current control [4]. As can be seen in (8), for a given apparent power, the number of SMs is dependent on the pole-to-pole DC voltage and is shown in Fig. 2.

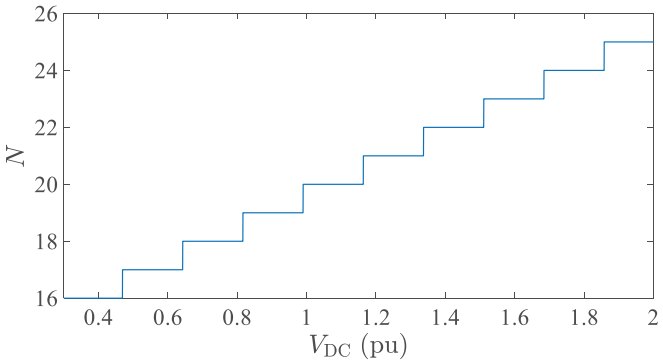


Fig. 2: The number of SMs of a FB-YY-MMC as a function of pole-to-pole DC voltage using the data in Table III.

III. Design Optimization

The optimization of the losses, semiconductor rating, and the SM's capacitor of the FB-YY-MMC will be investigated in this section. As discussed in Section I, the pole-to-pole DC voltage (V_{DC}) and the second-order circulating current amplitude and phase (I_{c2} and φ_{c2}) affect the losses (P_{l}) of the converter, the size of the SMs' capacitance (C), and the semiconductor current rating (I_{n}). Here, it will be shown that these parameters can be optimized by choosing specific values for V_{DC}, I_{c2}, and φ_{c2}.

A. Power losses

The losses of the FB-YY-MMC can be divided into three main parts: Conduction and switching losses, filter losses, and capacitance losses.

The conduction losses for a HB-YY-MMC have been presented in [15]. The same method has been expanded in this analysis to calculate the conduction losses for a FB-YY-MMC. The conduction losses are due to the losses that occur in the transistors and diodes of the SMs when the current is passing through them. To calculate the instantaneous conduction losses of a single transistor and diode, they are usually modeled by an offset voltage and an on-state resistor [17]. Defining p_{ct} and p_{cd} as the instantaneous conduction losses of a single transistor and diode, they are found to be

$$\begin{aligned} p_{\mathrm{ct}} &= V_{\mathrm{ce}} i_{\mathrm{ce}} + R_{\mathrm{ce}} i_{\mathrm{ce}}^2 \\ p_{\mathrm{cd}} &= V_{\mathrm{f0}} i_{\mathrm{f}} + R_{\mathrm{f0}} i_{\mathrm{f}}^2 \end{aligned} \tag{9}$$

where V_{ce}, R_{ce}, V_{f0}, and R_{f0} are the conduction offset voltage and on-state resistance of the transistor and the diode, and i_{ce} and i_{f} are the transistor and diode currents. The conduction losses of the arm of the FB-YY-MMC are dependent on the current path. The current path depends on the state of the switches, whether they are bypassed or inserted positively or negatively, and the direction of the current. Fig. 3 shows the current path for each SM with different states of the switches and when the arm current is positive. The same practice can be repeated for the negative arm current. Table I summarizes all the possible cases with the conduction losses corresponding to each SM.

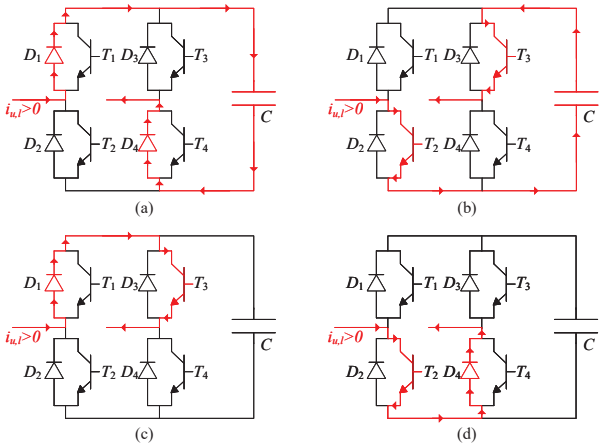


Fig. 3: The current path when the SM is (a) positively inserted, (b) negatively inserted, or (c) and (d) bypassed for the positive arm current.

TABLE I: Instantaneous conduction losses due to all the possible switching states for positive and negative current

	Transistor losses		Diode Losses	
Submodule State	$i_{\mathrm{u,l}} > 0$	$i_{\mathrm{u,l}} < 0$	$i_{\mathrm{u,l}} > 0$	$i_{\mathrm{u,l}} < 0$
Inserted positively	0	$2p_{\mathrm{ct}}$	$2p_{\mathrm{cd}}$	0
Inserted negatively	$2p_{\mathrm{ct}}$	0	0	$2p_{\mathrm{cd}}$
Bypassed	p_{ct}	p_{ct}	p_{cd}	p_{cd}

To calculate the total arm conduction losses, the number of inserted SMs should be determined; this is achieved by defining the upper and lower arm insertion indices as following

$$n_{\mathrm{u,l}} = \frac{\frac{V_{\mathrm{DC}}}{2} \mp V_{\mathrm{s}} \cos(\omega t)}{V_{\mathrm{C}}^{\Sigma}} \tag{10}$$

The insertion indices for an FB-YY-MMC is a number between -1 and 1 and determines the ratio between the inserted SMs and the total number of SMs in arm. It should be noted that the negative values of the insertion indices mean that the SMs are inserted negatively. From Table I and considering that the number of inserted and bypassed SMs are $N|n_{\mathrm{u,l}}|$ and $N - N|n_{\mathrm{u,l}}|$, respectively, the total arm conduction losses for the transistors and the diodes are found to be

$$p_{\text{ct,arm}} = \begin{cases} N(1-|n_{\text{u,l}}|)(V_{\text{ce}}|i_{\text{u,l}}| + R_{\text{ce}} i_{\text{u,l}}^2) & i_{\text{u,l}} \geq 0 \\ N(1+|n_{\text{u,l}}|)(V_{\text{ce}}|i_{\text{u,l}}| + R_{\text{ce}} i_{\text{u,l}}^2) & i_{\text{u,l}} < 0 \end{cases}$$
$$p_{\text{cd,arm}} = \begin{cases} N(1+|n_{\text{u,l}}|)(V_{\text{f0}}|i_{\text{u,l}}| + R_{\text{f0}} i_{\text{u,l}}^2) & i_{\text{u,l}} \geq 0 \\ N(1-|n_{\text{u,l}}|)(V_{\text{f0}}|i_{\text{u,l}}| + R_{\text{f0}} i_{\text{u,l}}^2) & i_{\text{u,l}} < 0 \end{cases} \quad (11)$$

The total conduction losses of the FB-YY-MMC in steady-state are found by averaging the sum of the instantaneous conduction losses of the transistor and diode and multiplying it by the number of arms as following

$$P_{\text{co}} = \frac{6}{T} \int_T (p_{\text{ct,arm}} + p_{\text{cd,arm}})\, dt \quad (12)$$

The switching losses of the MMCs are due to the switching of the transistors and diodes and are composed of three main contributions: transistor turn-on loss, transistor turn-off loss, and diode recovery loss. Because of different modulation techniques and sorting and balancing algorithms, finding switching losses is challenging for a generic MMC. Here, the switching losses due to essential switching, as defined in [15] are calculated. Assuming the nearest level modulation, the number of inserted SMs and the number of switching in the fundamental period is found to be round$(Nn_{\text{u,l}})$ and $2N$. The switching energy losses at time instance t_{k} are defined as $E_{\text{sw}}(t_{\text{k}})$, and are dependent on the amplitude and the direction of the current, and the switching state. For example, Fig. 4 shows the current path for two cases in which, a SM is bypassed from a positively or negatively inserted state when the current is positive. It can be seen that when the state of the SM varies from a positively inserted state to any of the bypassed states, the associated switching loss is due to turn-on loss of a transistor and recovery loss of a diode. Furthermore, when it switches from a negatively inserted state to any of the bypassed states, the switching loss is due to turn-off loss of a transistor. The same analysis can be repeated for all the switching states and has been reported in Table II, where E_{rec} is the recovery loss of the diode, and E_{on} and E_{off} are the turn-on and turn-off loss of the transistor, which are found from the semiconductor device datasheet. It should be noted that in Table II the switching state is shown as the rate of change in the number of inserted SMs or $\frac{d\left(\text{round}(Nn_{\text{u,l}})\right)}{dt}$. When this rate is positive it means that either the SM is being bypassed from a negatively inserted state or being inserted positively from a bypassed state, and when it is negative it means that either the SM is being bypassed from a positively inserted stated or being negatively inserted from a bypassed state.

From Table II, the switching losses of a SM at moment t_{k} is found to be

$$E_{\text{sw}}(t_{\text{k}}) = \begin{cases} E_{\text{rec}}(t_{\text{k}}) + E_{\text{on}}(t_{\text{k}}) & i_{\text{u,l}} \frac{d\left(\text{round}(Nn_{\text{u,l}})\right)}{dt} < 0 \\ E_{\text{off}}(t_{\text{k}}) & i_{\text{u,l}} \frac{d\left(\text{round}(Nn_{\text{u,l}})\right)}{dt} > 0 \end{cases} \quad (13)$$

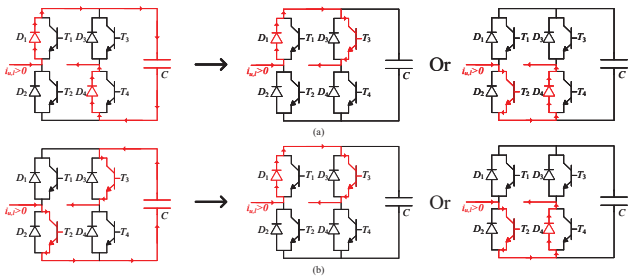


Fig. 4: The current path when the SM is bypassed from (a) a positively inserted state, or (b) negatively inserted state.

TABLE II: SMs switching energy loss based on the different switching states and current sign

$n_{\text{u,l}}$	$i_{\text{u,l}}$	$\frac{d\left(\text{round}(Nn_{\text{u,l}})\right)}{dt}$	Switching energy loss
+	+	−	$E_{\text{rec}} + E_{\text{on}}$
+	−	−	E_{off}
+	+	+	E_{off}
+	−	+	$E_{\text{rec}} + E_{\text{on}}$
−	+	−	$E_{\text{rec}} + E_{\text{on}}$
−	−	−	E_{off}
−	+	+	E_{off}
−	−	+	$E_{\text{rec}} + E_{\text{on}}$

The total switching losses of the FB-YY-MMC is calculated by summing the switching losses of the SMs in an arm of the FB-YY-MMC and multiplying it by the number of arms.

$$P_{\text{sw}} = \frac{6}{T} \sum_{k=1}^{2N} E_{\text{sw}}(t_{\text{k}}) \quad (14)$$

The filter losses (P_{fi}) are found by calculating the loss in the resistance of the filter. Taking into account a filter resistance of R as shown in Fig. 1 and calculating the Root Mean Square (RMS) of the arm current in (3), the filter loss is found to be

$$P_{\text{fi}} = 6RI_{\text{u,l,RMS}}^2 = R\frac{8I_{\text{DC}}^2 + 9\text{Ig}^2 + 36I_{c2}^2}{12} \quad (15)$$

To find the capacitance losses, the averaging principle introduced in [6] is deployed. Assuming the SM's capacitance losses are modeled by resistance R_{c}, the converter's capacitance losses are found by calculating the RMS current flowing through the equivalent capacitance of the arm. According to [6] and [12], this current is equal to multiplication of the insertion indices, in (10), by the arm current in (3). Thus, the converter's capacitance loss is calculated as

$$P_{\text{ca}} = \frac{6NR_{\text{c}}}{T} \int_T (n_{\text{u,l}} i_{\text{u,l}})^2\, dt = NR_{\text{c}} \Bigg(\frac{16m_{\text{AC}}^2 I_{\text{DC}}^2}{192} + \frac{9(4m_{\text{DC}}^2 + m_{\text{AC}}^2)I_{\text{g}}^2 + 72(2m_{\text{DC}}^2 + m_{\text{AC}}^2)I_{c2}^2}{192} + \frac{-144m_{\text{AC}}m_{\text{DC}}\cos(\varphi_{\text{ig}} - \varphi_{c2})I_{\text{g}}I_{c2}}{192} + \frac{+48m_{\text{AC}}\left(m_{\text{AC}}\cos(\varphi_{c2})I_{c2} - m_{\text{DC}}\cos(\varphi_{\text{ig}})I_{\text{g}}\right)I_{\text{DC}}}{192} \Bigg) \quad (16)$$

The total losses of FB-YY-MMC are found by summing all the mentioned losses in (12), (14), (15), and (16). Thus, the total losses are a function of V_{DC}, I_{c2}, and φ_{c2}, and are displayed in Fig. 5 using data in Table III. As the losses are a function of three variables, for simplicity of showing them in a 3D plot, the V_{DC} which results in optimization of the total losses of the FB-YY-MMC has been chosen in Fig. 5.

$$P_{\text{l}} = P_{\text{co}} + P_{\text{sw}} + P_{\text{fi}} + P_{\text{ca}} \tag{17}$$

TABLE III: The converter specifications and base values

Parameter	Symbol	Value
Arm Filter Resistance	R	72.83 mΩ
ES Rated Active Power	P_{n}	50 MW
Rated Reactive Power	Q_{n}	100 MVar
Rated Apparent (Base) Power	S_{b}	112 MVA
Line to Line Grid Voltage	V_{g}	33 kV
Grid Frequency	f	50 Hz
Base Current ($\frac{I_{\text{g}}}{2}$)	I_{b}	1.38 kA
Base Voltage (V_{s})	V_{b}	28.8 kV
SM's maximum voltage ripple (%)	ΔV	10
SM's Capacitor Resistance	R_{c}	20 $\mu\Omega$
Semiconductor Break-down Voltage	V_{bk}	4500 V
Semiconductor 100 Voltage FIT*	V_{100FIT}	2500 V
Semiconductor Rated Current	I_{n}	3000 A
Transistor Conduction Voltage	V_{ce}	0.8 V
Transistor Conduction Resistance	R_{ce}	0.7 mΩ
Diode Forward Voltage	V_{f0}	0.9 V
Diode Forward Resistance	R_{f0}	0.4 mΩ

*Usually, the semiconductor's nominal voltage is selected as the voltage corresponding to 100 FIT (100 failures in 10^9 operating hours) [16]

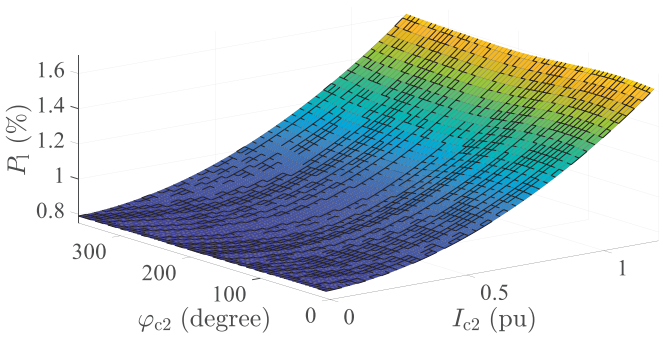


Fig. 5: Converter losses as a function of I_{c2} and φ_{c2}, for $V_{\text{DC}} = 1.81$ pu and specifications in Table III.

B. Semiconductor rating

The rated current of the semiconductor is determined by the absolute peak of the current flowing through it. Therefore, assuming steady-state mode of operation as mentioned in (3), the semiconductor rated current is calculated as in (18) and shown in Fig. 6 for the V_{DC}, which results in minimization of the semiconductor current rating using data from Table III.

$$I_{\text{n}} = \max\left(\left|\frac{I_{\text{g}}}{2}\cos(\omega t + \varphi_{\text{ig}}) + \frac{I_{\text{DC}}}{3} + I_{\text{c2}}\cos(2\omega t + \varphi_{\text{c2}})\right|\right) \tag{18}$$

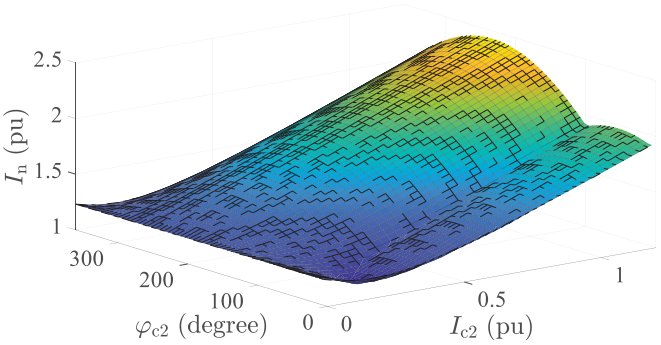


Fig. 6: Converter semiconductor current rating as a function of I_{c2} and φ_{c2}, for $V_{\text{DC}} = 1.94$ pu and specifications in Table III.

C. Submodule capacitor

The size of the SM's capacitance is found by finding the peak-to-peak value of the arm energy variation and setting a threshold for the capacitor's voltage ripple (ΔV). The arm energy variation is calculated by integrating the multiplication of the arm voltage in (7) and (3), and for an output voltage in (6) is found to be

$$\begin{aligned} w_{\text{u,l}} = \int_T v_{\text{u,l}} i_{\text{u,l}}\, dt &= \pm\frac{V_{\text{DC}} I_{\text{g}}}{4\omega}\sin(\omega t + \varphi_{\text{ig}}) \mp \frac{V_{\text{s}} I_{\text{DC}}}{3w}\sin(\omega t) \\ &\mp \frac{V_{\text{s}} I_{\text{c2}}}{2\omega}\sin(\omega t + \varphi_{\text{c2}}) + \frac{V_{\text{DC}} I_{\text{c2}}}{4\omega}\sin(2\omega t + \varphi_{\text{c2}}) \\ &- \frac{V_{\text{s}} I_{\text{g}}}{8\omega}\sin(2\omega t + \varphi_{\text{ig}}) \mp \frac{V_{\text{s}} I_{\text{c2}}}{6\omega}\sin(3\omega t + \varphi_{\text{c2}}) \end{aligned} \tag{19}$$

The SM's capacitance value is then calculated as [12]

$$C = \frac{\max(w_{\text{u,l}}) - \min(w_{\text{u,l}})}{N\Delta V V_{\text{n}}^2} \tag{20}$$

where V_{n} is the SM's rated voltage. Using the data from Table III, the SM's capacitance for the V_{DC} which results in the optimization of the SM capacitor and different values of I_{c2} and φ_{c2} is shown in Fig. 7.

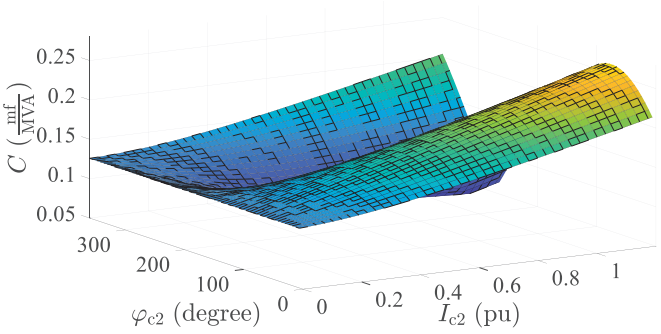
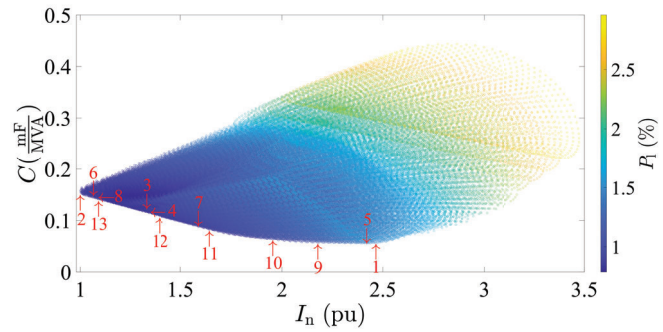


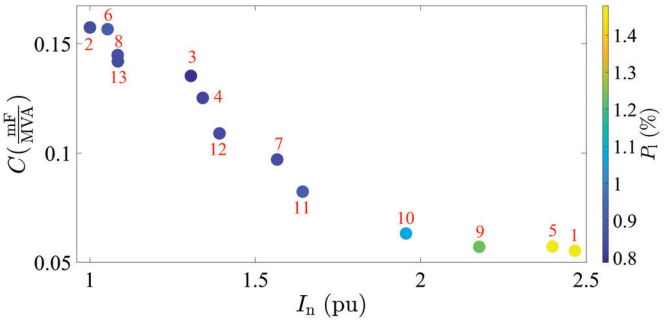
Fig. 7: SM's capacitance requirement as a function of I_{c2} and φ_{c2}, for $V_{\text{DC}} = 1.13$ pu and specifications in Table III.

IV. Analysis and Simulation Results

The set of all the possible points when V_{DC} is varied from 0.35 to 2 pu, I_{c2} from 0 to 1.2 pu, and φ_{c2} from



(a) All of the points



(b) The selected points

Fig. 8: All the possible points with their C, I_{n}, and P_{l} when V_{DC}, I_{c2}, and φ_{c2} varied, for a FB-YY-MMC with the specifications in Table III.

0 to 360°for the SM's capacitor size, semiconductor rating, and the losses of a FB-YY-MMC with specification in Table III are shown in Fig. 8. It should be mentioned that the chosen part number for the semiconductor device in Table III is 5SNA3000K452300 [18]. It can be seen that while the points with lower semiconductor rating result in low losses as well, they have relatively high capacitance. Out of all the points in Fig. 8a, 13 points have been selected and their corresponding parameters' values are introduced in Table IV and Fig. 8b. More specifically, Point 1, Point 2, and Point 3 are the optimized points for the SM's capacitor size, semiconductor rating, and losses, respectively. In Point 4 the circulating current is fully suppressed and V_{DC} is for the lowest SM's capacitor size as described in [12]. The same V_{DC} has been chosen for Point 5 to 8. In Point 5 and 6 the injected circulating current results in the minimum SM's capacitor size and semiconductor rating, respectively, when no limit has been set to the amplitude of the injected circulating current. The same is valid for Point 7 and 8; however, in these two cases, the amplitude of the injected circulating current is limited to 20% of the maximum arm current in Point 4. Point 9 to 13 are chosen from the Pareto-Frontier solutions, and they provide a trade-off between C, I_{n}, and P_{l}.

In Point 1, the capacitor's value and the number of SMs are significantly lower than Point 2 and Point 3 (the number of SMs for Point 1 is 19 from (8) compared to 23 and 22 for Point 2 and Point 3). However, because of the high amount of DC and circulating current, the semiconductor rating and losses are much higher. Point 4 to 8 have the same V_{DC} and the number of SMs are found to be 20. From Point 5 it can be seen that by injecting circulating current, the size of the capacitor can be reduced by 54%, but, the converter's semiconductor rating and losses increase drastically. Moreover, injecting circulating current can reduce the semiconductor rating by 22% (Point 6 with respect to Point 4) but increases the capacitor size and losses. By setting a limit for I_{c2}, it is still possible to have smaller capacitors or lower semiconductor ratings. For example, Point 8 shows a 20% reduction in semiconductor rating while the capacitor size and losses have not increased too much. Point 9 to 13 allow for a balance between the different design parameters. Point 9 and 10 require lower number of SMs (20 and 21, respectively) and lower capacitance but results in higher losses and semiconductor rating, while the inverse holds valid for Point 11 to Point 13. Because of the same V_{DC}, Point 11 to 13 have the same number of SMs and DC current. However, the relative high amount of injected circulating current increases the semiconductor rating and losses of Point 11 with respect to the other two points.

TABLE IV: Selected points and their specifications

Point	V_{DC} [pu]	I_{c2} [pu]	φ_{c2} [°]	C [$\frac{\text{mF}}{\text{MVA}}$]	I_{n} [pu]	P_{l} [%]
1	1.13	1.10	264	**0.06**	2.47	1.48
2	1.94	0.23	54	0.16	**1**	0.84
3	1.81	0.06	228	0.14	1.31	**0.79**
4	1.31	0	—	0.13	1.34	0.82
5	1.31	1.1	270	**0.06**	2.40	1.47
6	1.31	0.35	54	0.16	**1.05**	0.91
7	1.31	0.26	276	**0.1**	1.57	0.84
8	1.31	0.26	54	0.14	**1.08**	0.85
9	1.34	0.9	276	0.06	2.18	1.23
10	1.49	0.72	282	0.06	1.96	1.07
11	1.65	0.46	294	0.08	1.64	0.9
12	1.65	0.23	312	0.11	1.39	0.84
13	1.65	0.2	42	0.14	1.08	0.83

In order to verify the analysis, a time-domain simulation model as the one explained in [12] has been developed. The number of SMs and the SM's capacitor are considered to be fixed for all the points and are assumed to be 24 and 20 mF, respectively. The rest of the parameters are according to Table III.

First, the validation of (5) is investigated. For the rated active and reactive power exchange with the grid according to Table III, the circulating current for different pole-to-pole DC voltages has been determined. Fig. 9 shows the resulting circulating current for a pole-to-pole DC voltage as well as its harmonic components. As it can be seen, the circulating current of FB-YY-MMC is mainly composed of a DC term and a second-order component. The most significant component after the second-order is the 4th with the amplitude of around 0.31% of the DC term. The rest of the harmonics are lower than 0.2% of the amplitude of the second-order harmonic, verifying the initial assumption that the FB-YY-MMC circulating current is mainly composed of a DC term and a second-order harmonic component. Furthermore, according to (5) and (4),

the second-order circulating current component is dependent on both the exchanged active and reactive power, and the pole-to-pole DC voltage. Since the apparent power is assumed to be fixed in this analysis, the dependency of the second-order circulating current amplitude and phase on the pole-to-pole DC voltage has been investigated here. Fig. 10 shows the amplitude and phase of the second-order circulating current as a function of pole-to-pole DC voltage for validation of the theoretical analysis by the time-domain simulation. The base value for the current is the amplitude of the AC current exchanged with the grid ($\frac{I_g}{2}$). As can be seen, the simulation results are in agreement with the theoretical analysis. The maximum error is about 3%, due to the assumptions made in (5) and (7) and ignoring the voltage of the circulating current controller as explained in [12]. From Fig. 10 it can also be seen that the circulating current amplitude is significant with respect to its base value which is the the AC current exchanged with the grid ($\frac{I_g}{2}$). There is also a pole-to-pole DC voltage which leads to the minimum amplitude for the circulating current.

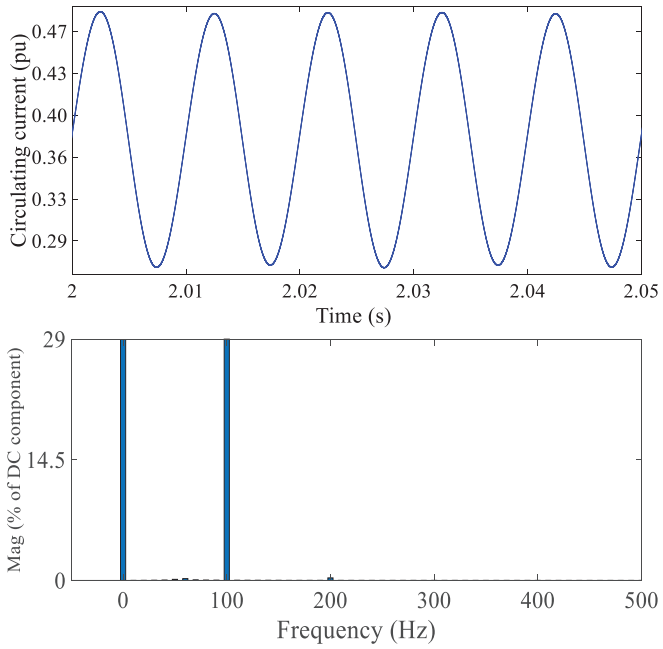


Fig. 9: The circulating current in time domain for $V_{DC} = 1.11$ pu (top) and its harmonic components (bottom).

Finally, Fig. 11 shows the sum capacitors' voltage ripple and arm absolute current for Points 1 to 3. As expected from Table IV, it is evident that the capacitor's voltage ripple and the arm maximum absolute current are minimized for Point 1 and 2, respectively. Moreover, Fig. 12 displays the simulation results for Point 11 to Point 13. The circulating current is controlled to the mentioned values in Table IV in three time-intervals. It can be seen that the highest voltage ripple occurs for point 13, meaning that a larger capacitance is needed for this point as suggested by Table IV, and the highest peak current occurs for Point 11. The RMS value of the arm current is also found to be 1.13 kA, 1.06 kA, and 1.05 kA for Point 11 to 13, respectively.

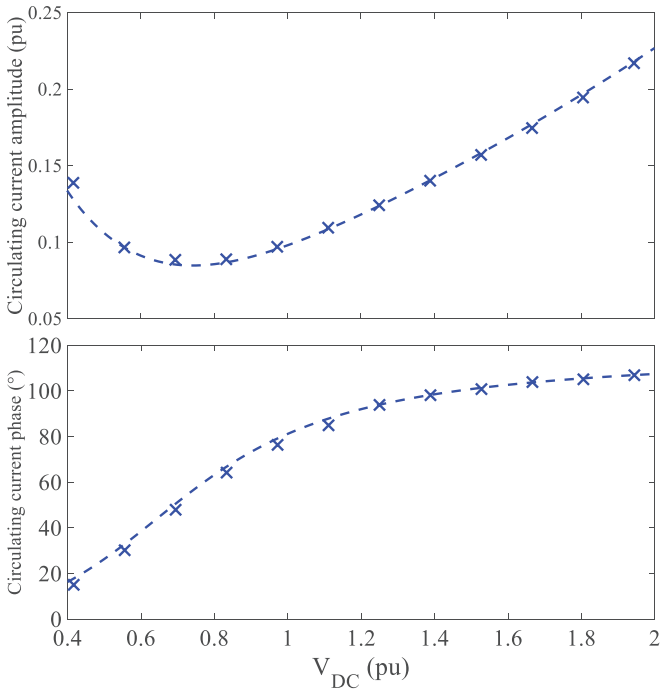


Fig. 10: The circulating current amplitude (top) and its phase (bottom) as a function of pole-to-pole DC voltage.

Moreover, the arm DC current is equal as the pole-to-pole DC voltage is equal for these three cases, therefore it can be said the high RMS current for Point 11 is responsible for its relatively higher losses as mentioned in Table IV.

V. Conclusion

In this paper the influence of pole-to-pole DC voltage and circulating current on the design parameters of a FB-YY-MMC has been investigated. First the converter's topology was analyzed and by investigating the internal dynamics of the FB-YY-MMC, the expression for the second-order circulating current was derived. Then, the design parameters like the number of SMs, losses, switch rating, and SM's capacitor size and their dependencies on the pole-to-pole DC voltage and the second-order circulating current amplitude and phase were investigated. It also suggested a number of points in which each of the design parameters are optimized or a trade-off between them have been suggested. These theoretical findings such as the equation for the second-order circulating current as well as the selected working points were validated through time-domain simulation, verifying the effectiveness of the proposed solution.

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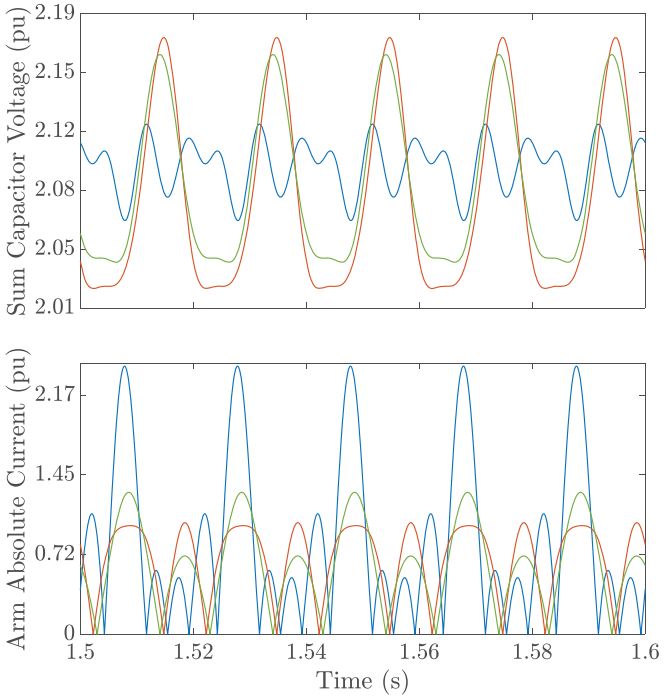

Fig. 11: Sum capacitor voltage ripple (top) and arm absolute current (bottom) for Point 1 (blue), Point 2 (red), and Point 3 (green).

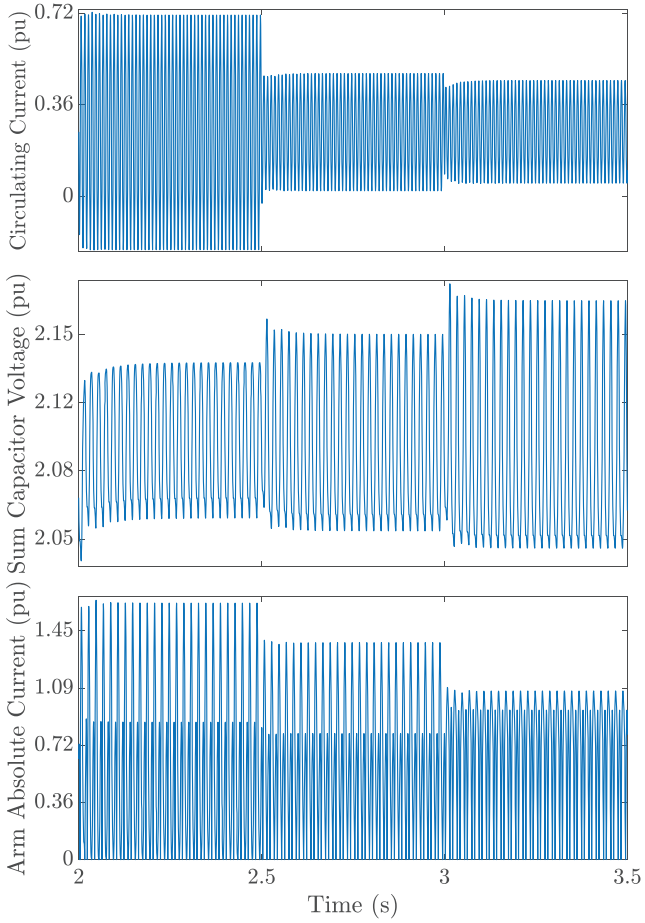

Fig. 12: Top: Circulating current; Middle: Sum of capacitor voltage of arm; Bottom: Arm absolute current for Point 11 (between 2 s and 2.5 s), Point 12 (between 2.5 s and 3 s), and Point 13 (between 3 s and 3.5 s).

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