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***Abstract*—This paper presents a dynamic gate bias (DGB) approach to improve the linearity of a Doherty Power Amplifier (DPA) designed for 5G FR1 applications, utilizing Gallium Nitride (GaN) transistors. The amplifier adopts a hybrid implementation on a printed circuit board (PCB), integrating transmission lines (TLs) and lumped discrete elements to optimize performance. Although the Doherty architecture is known for its efficiency advantages under back-off conditions, it encounters challenges such as gain compression at saturation of the main amplifier. To address this limitation, a dynamic gate biasing is used, enhancing the linearity and mitigating gain compression. The DPA fabricated on a Taconic RF-35 substrate with a dielectric constant of 3.5. The amplifier's performance is evaluated through both simulations and measurements. Key metrics, including gain, efficiency, and output power, are assessed for both DPA with standard gate bias and DPA with DGB for auxiliary amplifier, with measurement results demonstrating a peak drain efficiency of 55%, an output power of 43.5 dBm, average gain of 13 dB and a 2 dB improvement in gain compression in case of DGB approach. These outcomes confirm the DPA's suitability for high-linearity, high-efficiency applications within the 5G FR1.**

***Index Terms*—Power Amplifier, GaN Technology, Doherty PA, 5G FR1 Band, High Power, Linearity**

I. Introduction

The evolution of wireless communication systems, combined with the increasing complexity of modern modulation schemes, have placed significant demands on power amplifier (PA) design. To meet the requirements for higher output power and improved efficiency across a wide range of input power, high peak to average power ratio (PAPR), modern PAs must be designed for good efficiency not only at maximum output power but also at various power levels. Traditional PAs, designed for maximum output power, often struggle with modulated signals with varying envelop, leading to reduced efficiency in real-world applications, particularly in the context of 5G systems operating in the Frequency Range 1 (FR1). The Doherty Power Amplifier architecture [1], [2], known for its efficiency advantages under back-off conditions, is a promising solution for these requirements. However, traditional DPA designs often encounter significant gain compression at saturation, which can degrade performance in applications with high PAPR requirements.

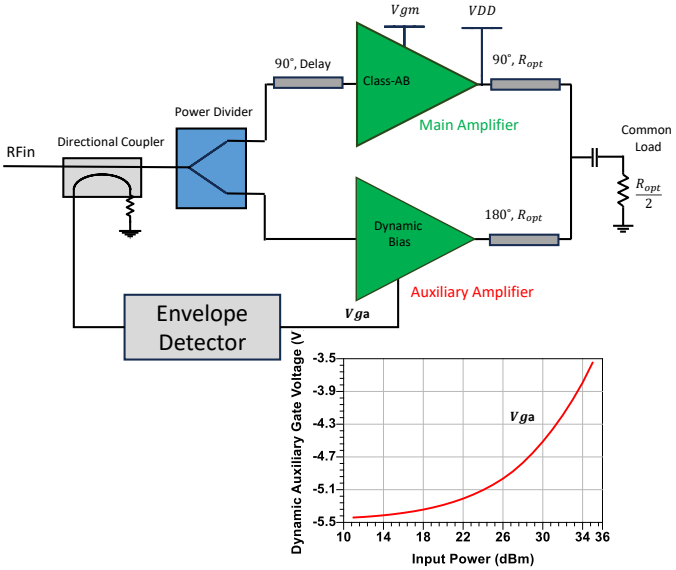

Fig. 1: A Doherty Power Amplifier architecture with dynamic gate biasing. An envelope detector generates the gate bias voltage for auxiliary device (Vga) using a sample of the input power level obtained through a directional coupler.

This paper addresses DPA gain compression at saturation of the main amplifier by applying a dynamic gate voltage, proportional to the input RF signal power, to the auxiliary amplifier of the designed DPA. This approach leverages the dynamic gate voltage technique to improve linearity and mitigate gain compression issues of the main amplifier at saturation [3], [4]. The DPA is implemented using a hybrid approach on a Printed Circuit Board (PCB), deploying GaN transistors, transmission lines (TLs), and lumped discrete elements on an RF-35 Taconic substrate to achieve an optimal balance between performance and design complexity. The choice of GaN technology, with its high power density, elevated breakdown voltage, and superior efficiency, plays a pivotal role in achieving the high-performance metrics required for next-generation communication systems.

This paper is organized as follows: Section II discussed about hybrid Doherty power amplifier design approach including device parasitic compensation and input stage design approach followed by a discussion on finding the gate voltage function. Section III outlines the fabrication process and presents the measurement results including S-parameter, Drain Efficiency and gain for both the conventional auxiliary gate bias DPA and the dynamic auxiliary gate bias DPA, with a comparative analysis. Finally, Section IV provides the concluding remarks.

II. Hybrid Doherty Power Amplifier Design Approach

The block diagram of dynamic gate bias DPA structure as shown in Fig. 1 consists of two amplifiers: a main amplifier, typically biased in Class AB, and an auxiliary amplifier, biased in Class C. In this configuration, the auxiliary amplifier remains inactive at lower input power levels and only turns on when the input power exceeds a certain threshold. This mechanism allows the DPA to maintain high efficiency by activating the auxiliary amplifier to provide additional power when necessary, thereby enhancing efficiency at back-off power levels.

In the theoretical framework of the Doherty amplifier, the ideal current generator assumption is employed. However, in practical implementations, power devices inherently exhibit parasitic reactances, which encompass both transistor-level and packaging parasitics. The equivalent output parasitic model for CG2H40010F is depicted in Fig. 2 with 1.93 pF shunt capacitor and 0.47 nH series inductor. To address these non-idealities, our design incorporates compensation techniques specifically tailored to mitigate these parasitic effects, a reactive compensation network is cascaded at the output of both the main and auxiliary devices as illustrated in Fig. 3. With this approach, the parasitic reactance of the device is mitigated [5]. Additionally, we implement a $\lambda/4$ impedance transformer to facilitate effective Doherty load modulation. This approach not only compensates for the parasitics and simplify design approach but also increase bandwidth of the DPA.

A two-stage Wilkinson power divider is employed to provide a wideband input for the DPA. This configuration ensures a balanced power split across a broad frequency range. To enhance the gain at back-off power levels, the input matching network is specifically designed for conjugate matching. The matching is optimized for a deep Class AB bias point, which allows for improved efficiency and linearity at lower output power levels, where the DPA operates most of the time.

In the DGB DPA structure, instead of biasing the auxiliary amplifier in the conventional Class C mode, a dynamic gate voltage, proportional to the input power signal, is applied to the auxiliary amplifier. This dynamic biasing shifts the auxiliary amplifier's operating point from Class C to Class AB as the input power increases. Consequently, in the saturation region, both amplifiers operate in Class AB mode, resulting in improved gain. This approach inherits the efficiency enhancement at lower input power levels from the conventional Doherty

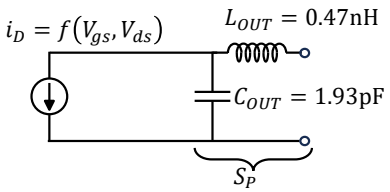

Fig. 2: CG2H40010F equivalent output parasitcs model.

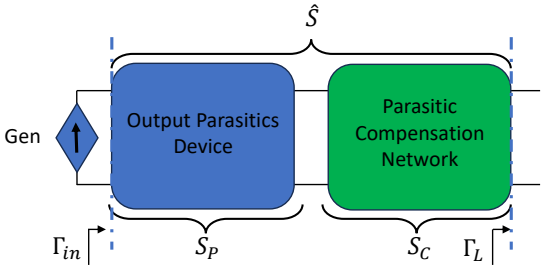

Fig. 3: Block digram of output parasitic compensation approach, including equivalent output parasitic of the device and parasitic compensation network.

amplifier while mitigating the gain reduction typically found at compression of the main amplifier thus improving linearity.

The gate bias function definition due to the memory effect of GaN devices and in general III-V semiconductor PAs is the challenging part of this architecture because the gate function cannot be defined from characterizing the PA for both static continuous-wave (CW) and dynamic signal measurements [6], [7]. The PA behaviour suffer from memory effect of dynamic gate voltage trajectory and to determine the gate function, we need iteration between PA performance and gate function adaption. To simplify the measurement process and determine the optimal gate voltage for the auxiliary device, various gate bias functions were applied during simulations. These functions were optimized to achieve a trade-off between gain linearity and efficiency profile. As shown in the lower left corner of Fig. 4, the gate bias functions were evaluated at different frequencies within the 2.7 GHz to 3 GHz range. By adjusting the gate bias of the auxiliary device, it was possible to tailor the performance across the frequency band, balancing linearity and efficiency.

III. Implementation and Measurement Characterization

The Doherty Power Amplifier implemented in this work employs a 1:1 symmetric configuration with a 6.0 dB output back-off performance. The design utilizes a 10 W GaN HEMT device, specifically the CREE CG2H40010F on a Taconic RF-35 substrate with dielectric constant of 3.5, substrate height H = 0.76 mm and metal thickness t = 0.035 mm. The design was developed using Advanced Design System software, to accurately predict the large signal performance of the high-power amplifier, non-linear transistor models and full electromagnetic simulations were conducted for the PCB to model the overall

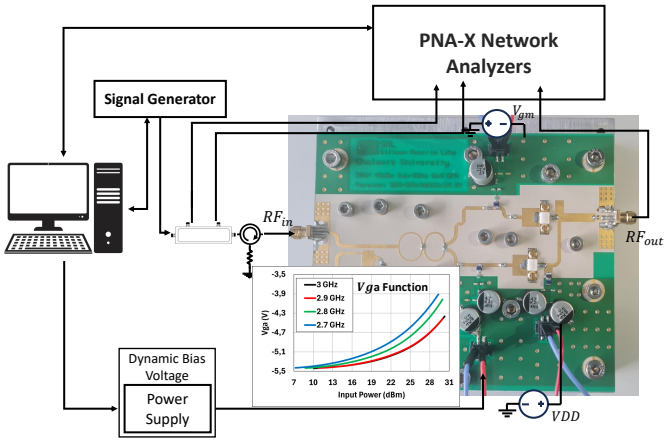

Fig. 4: Measurement setup and photograph of fabricated PCB for the designed Doherty PA, including the auxiliary gate voltage function (V_{ga}), evaluated across different frequencies in the range of 2.7 GHz to 3 GHz.

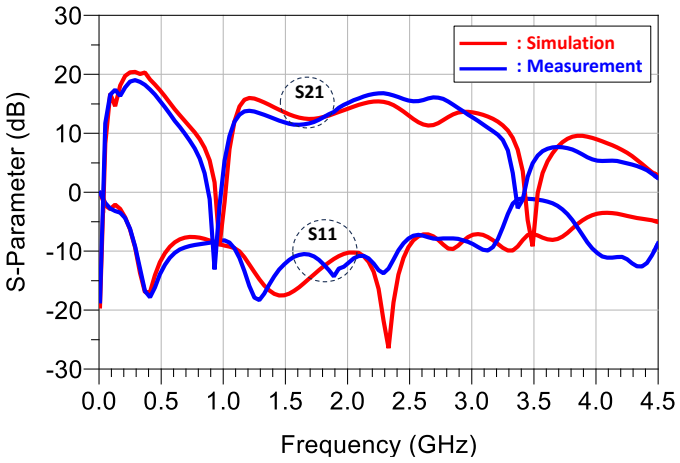

Fig. 5: Doherty PA S-parameter, A comparison between simulation (Red line) and measurement (Blue line).

performance of the DPA. Fig. 4 presents the measurement setup and circuit implementation of the symmetric DPA on a brass carrier for enhanced thermal dissipation. A two-stage Wilkinson power divider is employed at the input stage to ensure wideband input impedance matching.

The DPA is characterized through DC and small-signal measurements from 0.1 to 4.5 GHz, and CW single-tone excitation from 2.7 to 3 GHz in 100-MHz increment. Fig. 5 compares the simulated and measured return loss and small signal gain responses over the 0.1 to 4.5 GHz range, with supply voltages set to 28 V for both amplifiers, $V_{gm} = -2.3$ V ($I_{ds} = 160$ mA) for the main device, and $V_{ga} = -5.5$ V for the auxiliary. The amplifier demonstrates a small-signal gain exceeding 12 dB within the designed frequency band of 2.7 to 3 GHz, maintaining Doherty behavior with a return loss better than 8 dB, indicating excellent impedance matching. A good agreement is observed between the simulation and measurement results.

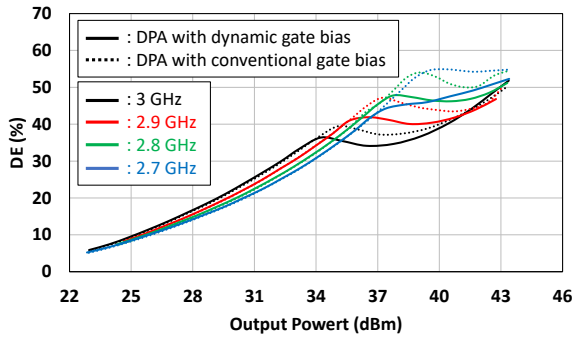

Fig. 6: Measured Drain Efficiency versus Output power for different frequencies in the range of 2.7 GHz to 3 GHz. A comparison between DPA with standard gate bias (Dashed lines) and DPA with DGB for auxiliary device (Solid line)

The characterization of the DPA under CW single-tone excitation was performed with two distinct biasing conditions for the auxiliary device.

In the first scenario, the main amplifier operates in Class-AB with $V_{gm} = -2.3$ V ($I_{ds} = 160$ mA), while the auxiliary amplifier is biased in Class-C with $V_{ga} = -5.5$ V, ensuring efficient operation across varying power levels. However, the gain compression from 6 dB OBO to peak output power exceeds 3 dB. To address this issue, an external dynamic bias voltage, proportional to the input power, is applied to the gate of the auxiliary amplifier. As the input power increases, the gate voltage is correspondingly increased. The dynamic gate voltage trajectory introduces memory effects that can degrade the performance of the PA. The proper gate voltage funtion defined using simulation and applied to the gate of auxiliary amplifier through PC-contorolled power supply and signal generator, depicted in Fig. 4. This approach enhances linearity and reduces gain compression in saturation region to below 1.5 dB, thereby improving the overall efficiency of the amplifier at higher power levels.

The measured drain efficiency and gain as functions of output power for CW excitation across the 2.7 to 3 GHz band, in 100 MHz increments, are presented in Fig.6 and Fig.7, respectively.

The characteristic high-efficiency profile of the Doherty amplifier is clearly visible for both the standard DPA and the DPA with DGB for the auxiliary amplifier in Fig. 6. The amplifier consistently achieved an output power exceeding 43 dBm across the measured 300 MHz bandwidth from 2.7 GHz to 3 GHz, demonstrating optimal device utilization. The drain efficiency ranged from 38% to 56% across a 6 dB output back-off, while at saturation, it achieved a drain efficiency between 50% and 55%.

Fig. 7 presents a comparison of the gain performance between the standard DPA and the DGB DPA across the 300 MHz frequency band. In the standard DPA, gain compression from 6 dB OBO to peak output power exceeds 3 dB, whereas in the DGB DPA, it remains below 1.5 dB across the 300 MHz

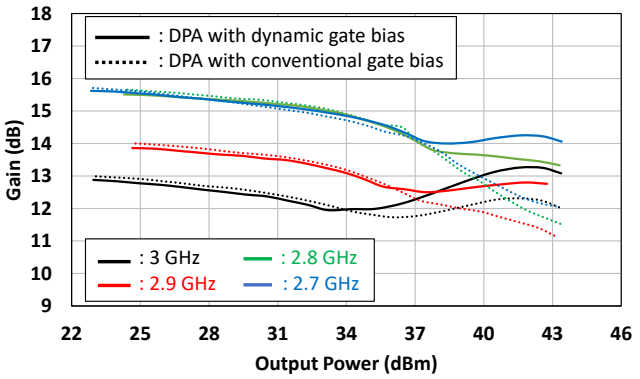

Fig. 7: Measured gain versus output power for different frequencies in the range of 2.7 GHz to 3 GHz. A comparison between DPA with standard gate bias (Dashed lines) and DPA with DGB for auxiliary device (Solid line)

bandwidth from 2.7 GHz to 3 GHz.

These results underscore the amplifier's capability to deliver high-efficiency performance over a broad frequency range, making it well-suited for modern wireless communication applications that demand energy-efficient operation across varying power levels. A comparison with published GaN DPA, which offers similar levels of gain and output power, is shown in Table I. The results underscore the effectiveness of the DGB in sustaining gain at saturation of the main amplifier.

TABLE I: Performance comparison

Parameter	**[2]**	**[4]**	**This work**
Technology	GaN HEMT CG2H40010F	GaN HEMT CG2H40045	GaN HEMT CG2H40010F
Bias Condition	Standard	Dynamic Gate Bias	Dynamic Gate Bias
Frequency (GHz)	3-3.6	1.94	2.7-3
BW (MHz)	600	-	300
$\mathbf{Gain_{sat}}$ (dB)	8.4	13	12.8
$\mathbf{Gain_{OBO}}$ (dB)	9.8	14.3	13.8
$\mathbf{P_{sat}}$ (dBm)	44	50.1	43.5
$\mathbf{DE_{sat}}$ (%)	60	68.1	60

Conclusion

This work demonstrates the successful implementation of a 5G FR1 GaN hybrid DPA incorporating a dynamic gate bias to improve the linearity of DPA at saturation of the main amplifier, achieving a peak power of 43.5 dBm, a large signal gain of 13 dB, and a drain efficiency of 60% at saturation. In conclusion, the DGB DPA demonstrates significantly improved gain performance compared to the standard DPA across the 300 MHz frequency band from 2.7 GHz to 3 GHz. The gain compression in the standard DPA, observed between OBO and peak output power, exceeds 3 dB. In contrast, the DGB DPA exhibits reduced gain compression, remaining below 1.5 dB throughout the 300 MHz measured frequency band. This enhancement highlights the effectiveness of the dynamic gate bias technique in improving linearity and mitigating gain compression of the main amplifier. The use of GaN transistors in the hybrid Doherty architecture has proven effective in addressing the challenges of high-efficiency amplification for modern communication systems. These findings confirm the viability of this approach for future high-performance, energy-efficient wireless applications.

Acknowledgment

This work was supported by the ALL2GaN Project through the EU Chips Joint Undertaking and its members, including the top-up funding by Austria, Belgium, Czech Republic, Denmark, Germany, Greece, The Netherlands, Norway, Slovakia, Spain, Sweden, and Switzerland, under Grant 101111890.

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