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In-Band Full-Duplex Antenna Beamforming and Synchronization for Self-Interference Mitigation: Multi-Tile RFSoC Testbed Design and Deployment

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***Abstract*—This paper presents a newly developed in-band full-duplex (IBFD) communication and sensing testbed utilizing digital beamforming on the advanced Xilinx ZCU216 Radio Frequency System-on-Chip (RFSoC) platform, featuring 16 DACs and 16 ADCs with 14-bit resolution divided into four tiles. Key design and deployment challenges include achieving precise phase synchronization across multiple RFSoC tiles (due to independent clocks causing random phase shifts) and mitigating self-interference (SI) caused by strong mutual coupling effects between closely spaced transmitting (Tx) and receiving (Rx) antenna arrays. To address these challenges, we employed a Tx beamforming algorithm for maximum antenna gain and an Rx beamforming method to maximize the signal-to-self-interference ratio (SSIR) at the receiver output. Specifications of two 1×5 Vivaldi antenna arrays (3–6 GHz), integrated into our RFSoC-based testbed, and the multi-tile synchronization (MTS) framework were established to meet IBFD performance requirements. The deployment involved implementing the beamforming algorithms, configuring the Tx and Rx arrays, and ensuring calibration and synchronization across RFSoC tiles. Experimental results demonstrate over 80 dB SI suppression with half-wavelength separation (@6 GHz) between the Tx and Rx arrays, highlighting the testbed's potential for applications in 6G integrated communication and radar sensing.**

***Index Terms*—Phased arrays, beamforming, in-band full duplex, 6G communication and sensing, RF SoC, measurements.**

I. Introduction

As communication systems continue to evolve, future networks face increasing challenges related to spectrum congestion. The rising demand for more efficient spectrum utilization necessitates the development of advanced traffic management and channel sensing techniques. One promising solution to this challenge is in-band full-duplex (IBFD) technology, which enables simultaneous transmission and reception on the same frequency channel, offering significant improvements in spectrum efficiency and data rates for wireless communication systems [1], [2]. IBFD has the potential to revolutionize a variety of applications, including increasing base station capacity by supporting concurrent uplink and downlink communication in next-generation cellular networks, providing real-time updates in automotive radar systems, and enabling continuous tracking of multiple targets in defense and surveillance operations [3].

However, IBFD systems face a significant challenge: self-interference (SI), which arises when a signal transmitted by the transmitter (Tx) couples into the receiver (Rx), especially in scenarios where Tx and Rx arrays are closely spaced [4]. This coupling complicates signal processing, affecting both performance and system integrity. Self-interference cancellation (SIC) is therefore a crucial aspect of IBFD design, particularly for maintaining high-quality signal reception.

The integration of RFSoC platforms, like the ZCU216 evaluation board, has enabled practical implementations of SIC techniques [7]. RFSoCs offer real-time processing capabilities and high levels of integration [6], making them well-suited for IBFD communication and sensing applications [5]. However, precise synchronization between the transmission and reception paths remains a key challenge due to phase shift introduced by phase-locked loops (PLLs) variations. Effective phase synchronization across all Tx and Rx channels is therefore essential for the success of digital beamforming and SIC. The RFSoC's MTS feature addresses this by aligning Tx and Rx paths across multiple DAC and ADC channels but requires precise calibration and timing, which depends on clock distribution and settings. A method in [10] estimates and compensates phase shifts in the entire propagation path, showing promising results for synchronizing two ZCU216 tiles. However, applying it to beamforming algorithms (e.g., phase-steering with a 1×4 patch antenna) revealed beam pointing errors of up to 10°, with asymmetries and smeared nulls (Figs. 8-10). These phase errors could worsen in larger arrays and more complex beamforming scenarios.

This paper provides a design and deployment framework for implementing digital Tx and Rx beamforming methods on the ZCU216 evaluation platform in IBFD scenarios with coupled Tx and Rx arrays. First, the features of the RFSoC are introduced in Sec. II. Afterwards, Sec. III discusses the MTS along with the appropriate clock distribution settings. In Section IV, the process of waveform generation is explained. As a case study, the Tx maxGain beamformer is implemented to maximize the antenna array's transmission gain in a desired direction [11]. At the same time, the

maxSSIR (signal-to-self-interference ratio) beamformer (see e.g. [12]), is implemented on the Rx side. The Rx beamformer increases the received signal power from the target direction while mitigating SI. In Sec. V, we evaluate the effectiveness of these beamforming techniques for a narrowband IBFD scenario, comparing numerical simulations with experimental measurements.

This work aims at establishing the foundation for developing a testbed for joint Tx [13] and Rx beamforming approaches, among which future integrated sensing and communication (ICAS) applications.

II. The RFSoC ZCU216

The Zynq UltraScale+ RFSoC ZCU216 board features 16× 14-bit DACs and 16× 14-bit ADCs, grouped into 4 tiles each. It supports direct RF signal conversion across a wide frequency range, from DC to 6 GHz. With sampling rates of up to 10 GSPS for the DACs and 2.5 GSPS for the ADCs, the board enables high-fidelity testing of advanced antenna designs for modern communication systems [1].

In addition to its high-speed data converters, the board integrates powerful real-time signal processing capabilities with programmable logic (PL), making it suitable for custom antenna system designs and complex signal processing tasks. Furthermore, the MATLAB control provides enhanced flexibility for rapid prototyping and custom waveform generation.

III. DAC and ADC Clock Synchronization

Each tile of 4 DACs/ADCs operates with its own PLL, leading to phase misalignment without synchronization. MTS ensures all tiles share a common clock for synchronized operation [9]. MTS involves setting up a shared reference clock and aligning sample clocks across tiles using the system reference (sysref) signal, which must meet specific conditions [9]:

1) The sysref must be an integer submultiple of the greatest common divisor of the DAC and ADC sampling rates, divided by 16.
2) It must also be an integer submultiple of all programmable logic clocks to ensure synchronous sampling.
3) The sysref frequency should be below 10 MHz.

Achieving MTS on the ZCU216 with Xilinx's default clock settings is challenging. Misaligned PLL dividers and improper sysref routing can cause synchronization issues. In fact, proper synchronization requires fine-tuning of the PLL settings, proper sysref routing (clock distribution settings), and using low-jitter clock sources, if external clocks are to be used. Tools like Vivado help align clock configurations (http://amd.com).

In our Vivado design, the CLK104 add-on card is programmed with a DAC and ADC reference clock of 300 MHz, a sysref frequency of 5 MHz, and a PL input clock of 300 MHz, as shown in Fig. 1. The DAC operates at a sampling rate of 9.6 GHz, while the ADC sampling rate is 2.4 GHz. Clock forwarding is employed to distribute the DAC PLL output from Tile 2 to all DAC tiles, and similarly, the ADC PLL output from Tile 2 is shared across all ADC tiles, ensuring that all channels remain phase-synchronized.

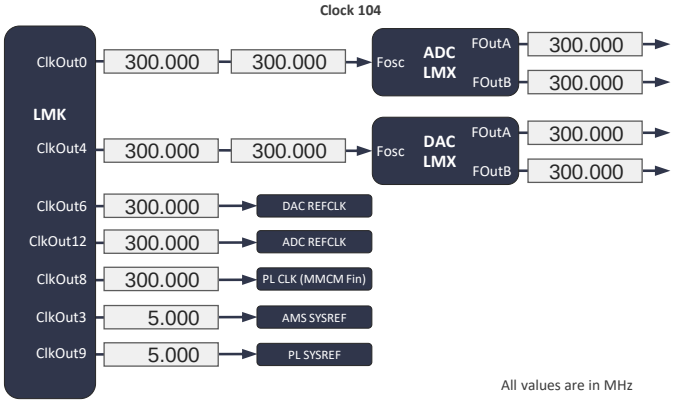


Fig. 1. Functional PLL clock settings used in the supplied GUI (*cf.* AMD's RF Data Converter Interface User Guide, at https://docs.amd.com).

IV. IBFD Testbed and Beamforming Algorithm

A. IBFD Testbed Configuration

Our test setup consists of an IBFD system with a 1×5 Tx and a 1×5 Rx Vivaldi antenna array, operating in the 3–6 GHz frequency range. Each antenna element is 3D-printed, silver-coated, and fed by a coaxial probe mounted on an aluminum ground plane [8]. The arrays are positioned side-by-side, with a maximum spacing of 0.5λ (@6 GHz) between individual elements and sub-arrays. The antennas are connected to a custom-designed PCB that includes commercial off-the-shelf (COTS) baluns[1], which convert unbalanced signals to differential inputs and outputs for the DACs and ADCs. These COTS baluns are connected to different tiles of the RFSoC, enabling independent data processing for each antenna.

The block diagram of the integrated antenna-RFSoC measurement platform, shown in Fig. 2, incorporates ADCs, DACs, PL, and digital processing system (PS) cores. A movable probe antenna is connected to either Amplifier 1 (Amp1, 50 dB gain) or Amplifier 2 (Amp2, 50 dB gain) to compensate for signal propagation losses.

The system starts by generating a discrete-time signal representing a continuous wave (CW) signal of frequency ω_c. The waveform generation can be achieved through the standard Xilinx GUI tool, however, for full flexibility we generate the time-domain samples with optimal spectral properties (spurious-free) through an in-house MATLAB function (see App. A). This *digital* signal is represented as $g[n] = \mathfrak{Re}\{U_\mathrm{t} e^{jn\omega_c/f_\mathrm{s}}\}$, where $n \in \mathbb{Z}$. The complex amplitude U_t is multiplied by the Tx beamforming vector $\mathbf{w}^{\mathrm{Tx}}$ to produce a 5×1 vector $\mathbf{U}_\mathrm{t}$. These signals are then converted to phase-synchronized *analog* voltage amplitudes $\mathbf{V}_\mathrm{t} \propto \mathbf{U}_\mathrm{t}$, passed through baluns, and transmitted via the Tx antennas. At the Rx array, the received voltages, after passing through baluns, form a 5×1 vector $\mathbf{V}_{\mathrm{sig}}$ and $\mathbf{V}_{\mathrm{int}}$, representing desired and interferer signals, respectively. Once digitized by ADCs, the

[1]Product No: X4BD40L1-50100G

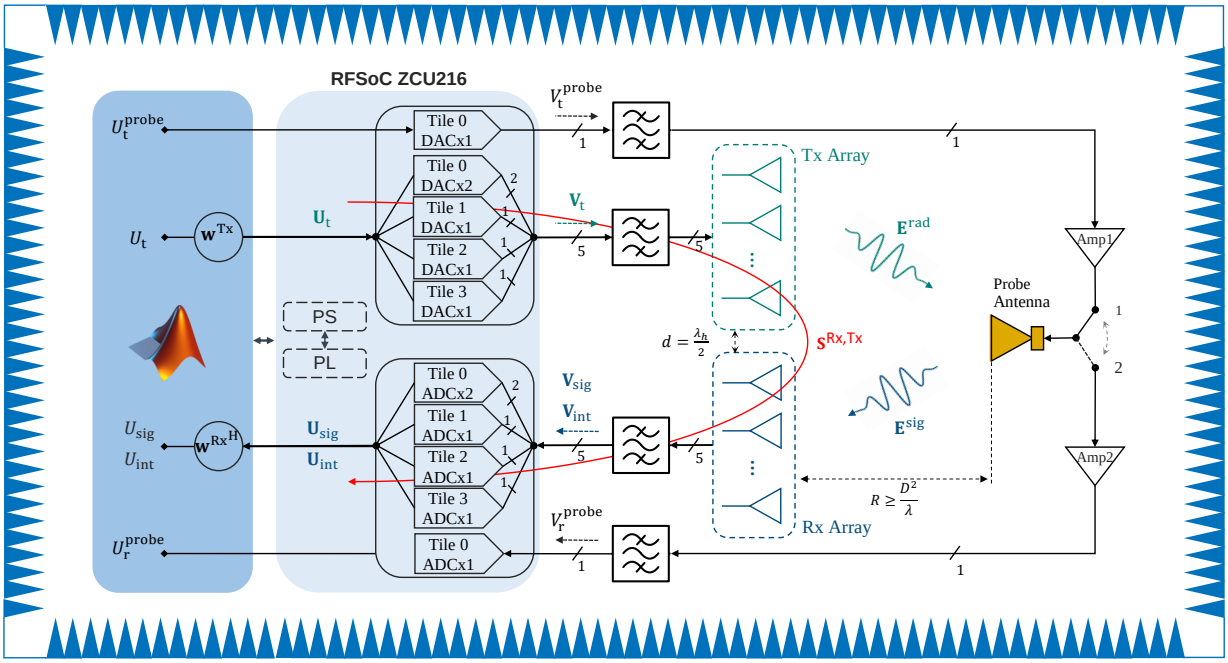


Fig. 2. Block diagram of the integrated IBFD antenna system - implemented RFSoC measurement setup, used for demonstration.

digital signal $\mathbf{U}_{\text{sig}} \propto \mathbf{V}_{\text{sig}}$ and SI $\mathbf{U}_{\text{int}} \propto \mathbf{V}_{\text{int}}$ are multiplied by the Rx beamforming vector $(\mathbf{w}^{\text{Rx}})^{\text{H}}$, yielding the final post-processed complex phasor amplitude U_{sig} and U_{int}. MATLAB is used to control the evaluation board, generate and capture time-domain waveforms, and perform the FFT for frequency-domain analysis.

B. Tx and Rx Beamforming Algorithm

Using the model in Fig. 2, the Tx beamforming vector $\mathbf{w}^{\text{Tx}}$ optimizes the excitation across the Tx array, while the Rx beamforming vector $(\mathbf{w}^{\text{Rx}})^*$ optimizes the reception at the Rx array. The time-averaged power flux density of the incident wave, corresponding to the desired signal, is denoted as $\mathbf{E}^{\text{sig}}$. The total input power at the Tx antenna ports, P_{in}, and the total received signal and SI power at the Rx beamformer port, P_{sig} and P_{int}, respectively, in an SI-dominated system (without considering noise), are given by:

$$P_{\text{in}} = \frac{\mathbf{V}_{\text{t}}^{\text{H}}\mathbf{V}_{\text{t}}}{2Z_0},$$
$$P_{\text{sig}} = \frac{\left|\left(\mathbf{w}^{\text{Rx}}\right)^{\text{H}}\mathbf{V}_{\text{sig}}\right|^2}{2Z_0}, \quad P_{\text{int}} = \frac{\left|\left(\mathbf{w}^{\text{Rx}}\right)^{\text{H}}\mathbf{V}_{\text{int}}\right|^2}{2Z_0}, \tag{1}$$

where $Z_0 = 50\ \Omega$ is the characteristic impedance, and $(.)^{\text{H}}$ denotes the Hermitian operator.

The total IBFD system isolation at the Rx beamformer port is defined as [14]:

$$\text{ISO} = \frac{P_{\text{in}}(\mathbf{w}^{\text{Tx}})}{P_{\text{int}}(\mathbf{w}^{\text{Tx}}, \mathbf{w}^{\text{Rx}})} = \frac{\mathbf{V}_{\text{t}}^{\text{H}}\mathbf{V}_{\text{t}}}{\left|\left(\mathbf{w}^{\text{Rx}}\right)^{\text{H}}\mathbf{V}_{\text{int}}\right|^2} \tag{2}$$

1) Tx maxGain Beamforming: In this section, we aim to find the optimal beamformer weight coefficient vector $\mathbf{w}^{\text{Tx}}$ that maximizes the Tx antenna array gain in a particular direction. After beamforming, the angular sampled total Tx antenna array pattern is defined as

$$\mathbf{E}_a(\mathbf{w}^{\text{Tx}}) = \begin{bmatrix} E_{co,a}(\theta_1) \\ \vdots \\ E_{co,a}(\theta_L) \end{bmatrix} = \mathbf{E}\mathbf{V}_{\text{t}}(\mathbf{w}^{\text{Tx}}) \tag{3}$$

where $\mathbf{E}$ be an $L \times 5$ matrix containing the angular sampled embedded element patterns. Each matrix element represents the embedded element pattern $E_{co,n}(\theta_l)$ at the sampled angles θ_l for $l = 1, 2, \ldots, L$. In order to maximize the power $|E_{co,a}(\theta_p)|^2$ in the direction θ_p, the optimal weight vector can be set as:

$$w_{\text{opt},n}^{\text{Tx}} = E_{co,n}^*(\theta_p), \quad n = 1, 2, \ldots, 5 \tag{4}$$

This solution, known as conjugate field matching, optimizes the array gain in the direction θ_p [11].

2) Rx maxSSIR Beamforming: Our goal is to find the optimal Rx beamforming weights that maximize the signal-to-SI ratio (SSIR), by optimizing the desired signal power from the intended direction while minimizing the interference power at the receiver's output. The SSIR is given by:

$$\text{SSIR} = \frac{P_{\text{sig}}}{P_{\text{int}}} = \frac{(\mathbf{w}^{\text{Rx}})^{\text{H}}\mathbf{V}_{\text{sig}}\mathbf{V}_{\text{sig}}^{\text{H}}(\mathbf{w}^{\text{Rx}})}{(\mathbf{w}^{\text{Rx}})^{\text{H}}\mathbf{V}_{\text{int}}\mathbf{V}_{\text{int}}^{\text{H}}(\mathbf{w}^{\text{Rx}})}, \tag{5}$$

To achieve the maximum SSIR, we solve for the weight vector by setting $\nabla_{(\mathbf{w}^{\text{Rx}})^{\text{H}}}\text{SSIR} = 0$ which leads to a generalized eigenvalue problem

$$\left(\mathbf{V}_{\text{sig}}\mathbf{V}_{\text{sig}}^{\text{H}}\right)\mathbf{w}^{\text{Rx}} = \text{SSIR}\ \left(\mathbf{V}_{\text{int}}\mathbf{V}_{\text{int}}^{\text{H}}\right)\mathbf{w}^{\text{Rx}}. \tag{6}$$

The optimal $\mathbf{w}_{\text{opt}}^{\text{Rx}}$ is the eigenvector of $(\mathbf{V}_{\text{int}}\mathbf{V}_{\text{int}}^{\text{H}})^{-1}(\mathbf{V}_{\text{sig}}\mathbf{V}_{\text{sig}}^{\text{H}})$ corresponding to its largest eigenvalue [12], and is normalized such that $(\mathbf{w}_{\text{opt}}^{\text{Rx}})^{\text{H}}\mathbf{w}_{\text{opt}}^{\text{Rx}} = 1$.

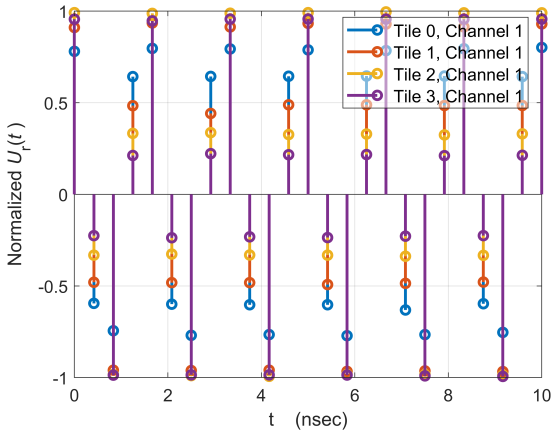


Fig. 3. Normalized ADC output data for loopback channels at different tiles.

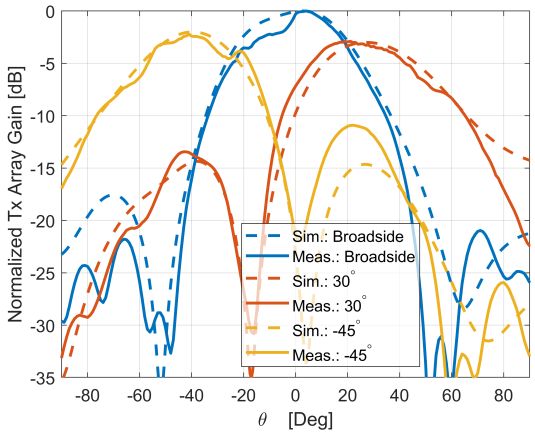


Fig. 4. Normalized max transmit antenna array gain pattern cut in the E-plane at different scan angles.

C. The Measurement Procedure

The measurement procedure consists of the following steps:

- **Tx EEP Measurements**: The probe antenna, connected to an LNA (switch position 2), measures $U_{\mathrm{r}}^{\mathrm{probe}}$ when each Tx element is excited with a 1 V CW signal, while the others are inactive. Each such scan samples a Tx EEP.
- **Rx EEP Measurements**: In switch position 1, the probe antenna transmits $U_{\mathrm{t}}^{\mathrm{probe}} = 1$ V. The voltages measured at the Rx elements correspond to the Rx antenna EEPs.
- **SI Measurement**: With the probe off, the Tx array excites with maximum gain beamforming in a given direction. The Rx voltages measure interference $\mathbf{U}_{\mathrm{int}} = \mathbf{S}^{\mathrm{Rx,Tx}}\mathbf{U}_{\mathrm{t}}$. Here, $\mathbf{S}^{\mathrm{Rx,Tx}}$ is the mutual coupling matrix,
- **Beamformer Optimization**: The Tx EEPs are used to optimize $\mathbf{w}^{\mathrm{Tx}}$ (see Sec. IV-B1), followed by optimizing $(\mathbf{w}^{\mathrm{Rx}})^*$ for SI cancellation (see Sec. IV-B2).

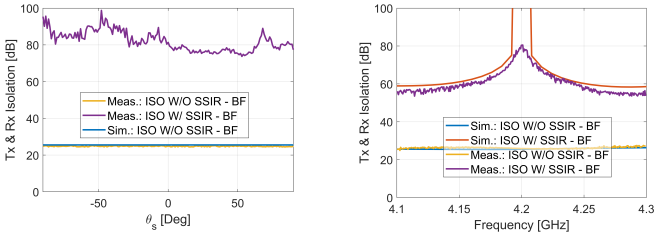
V. Performance Evaluation

A. Synchronization Results

The XM650 add-on card [9] is used for DAC-to-ADC loopback testing with Murata N79 band baluns and filters (http://murata.com/). MTS is applied, generating a 4.2 GHz single-tone signal across all DACs. Fig. 3 shows the normalized ADC data, confirming good alignment across channels. However, any change in the signal frequency requires fine-tuning of the PLL settings to maintain synchronization.

B. Beamforming Simulation and Measurement Results

1) Tx maxGain Beamforming: Array beam pattern simulations and measurements are conducted by varying the optimized beam weights, $\mathbf{w}_{\mathrm{opt}}^{\mathrm{Tx}}$, from $-90°$ to $90°$ in $1°$ steps. A single-tone signal is generated at 4.2 GHz, and the simulated and measured normalized maximum Tx array gain patterns in the E-plane at $-30°$, broadside, and $45°$ are shown in Fig. 4. There is a slight discrepancy between the simulated and measured Tx gains, particularly at positive angles, due to irradiating GND-plane edge absorbers, which are not accounted for in the simulation.



(a) (b)

Fig. 5. Simulation-measurement comparison: (a) Total Tx-Rx isolation with and without max-SSIR beamforming across the scan direction (Note: Simulated total Tx-Rx isolation with max-SSIR beamforming is not shown, as it reaches levels of $\approx$ 350 dB); (b) Total Tx-Rx realized isolation with and without max-SSIR beamforming over frequency.

2) Rx maxSSIR Beamforming: The receiver weight coefficients are optimized while the Tx antenna array is excited toward broadside with maximum gain. Fig. 5(a) shows the total IBFD system isolation across E-plane scan angles. Without beamforming, the intrinsic isolation is approximately 25 dB, but it exceeds 80 dB when Rx maxSSIR beamforming is applied. Fig. 5(b) illustrates the total IBFD system isolation over frequency for a fixed beamformer optimized at 4.2 GHz. A slight degradation in measurements is likely due to phase errors in the RFSoC DAC/ADC outputs and the system's dynamic range limit, with similar fluctuations observed outside the optimization frequency.

VI. Conclusion

This work presents a practical implementation of Tx and Rx beamforming for IBFD systems on the ZCU216 RFSoC platform, focusing on SI cancellation through optimized beamforming. The use of MTS to align phases between the DAC and ADC tiles is critical in ensuring coherent operation across multiple channels. Our setup, including a custom Vivaldi antenna array and a continuous waveform generator, serves as a comprehensive testbed for IBFD performance validation. Results show significant SI suppression, making the methods promising for real-world applications like wireless communication and radar. Future work will focus on developing advanced beamforming techniques to improve system robustness

in dynamic environments and further optimize SI cancellation mechanisms.

ACKNOWLEDGMENT

This work, conducted within the Advanced Digitalization program at the WiTECH Centre [DIGIARRAY project], is financed by VINNOVA, Ericsson, Saab, Satcube, and Chalmers. The authors would also like to acknowledge discussions with the following individuals, contributing to the DigiArray project: Ashraf Uz Zaman (Chalmers), Teanette van der Spuy and Lukas Nyström (Satcube), Darwin Blanco (Ericsson), Andreas Wikström and Magnus Isacsson (Saab).

APPENDIX A
CONTINUOUS WAVEFORM GENERATION FOR DAC

This section focuses on optimizing the sample-and-hold (S&H) output of the DAC to produce a spurious-free continuous waveform (CW) at frequency f_c with period $T_\mathrm{c} = 1/f_\mathrm{c}$. We start by defining the pulse function:

$$p(t) = \begin{cases} 1 & 0 \le t < T_\mathrm{s} \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

with $T_\mathrm{s} = 1/f_\mathrm{s}$, where f_s is the DAC sampling frequency. For N samples, over the entire time slot $0 \le t < T = NT_\mathrm{s}$, the S&H signal is defined as

$$u(t) = \sum_{n=0}^{N-1} Q_n p(t - nT_\mathrm{s}), \tag{8}$$

where $\{Q_n\}_{n=0}^{N-1}$ are coefficients to optimize. Since $u(t)$ is periodic, its complex Fourier series representation is:

$$u(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega_0 t}, \tag{9}$$

where $\omega_0 = 2\pi/T$, and $C_k = \frac{1}{T}\int_0^T u(t)e^{-jk\omega_0 t}\,\mathrm{d}t, \quad k \in \mathbb{Z}$. Then, we can obtain the Fourier coefficients:

$$C_k = \frac{1}{N}\mathrm{sinc}\left(\frac{k\pi}{N}\right)\sum_{n=0}^{N-1} Q_n e^{-jk\pi\frac{(2n+1)}{N}}, \tag{10}$$

showing a sinc amplitude tapering for the spectrum $\{C_k\}$ with increasing k. Next, we will optimize $\{Q_n\}$ to achieve the desired spectrum $\{C_k\}$, possibly counteracting the sinc-tapering effect and free of spurious frequencies.

Since $u(t)$ is real-valued, its real Fourier series

$$u(t) = B_0 + \sum_{k=0}^{\infty} B_k \cos(k\omega_0 t + \varphi_k), \tag{11}$$

where $B_0 = |C_0|$, $B_k = 2|C_k|$, and $\varphi_k = \arg\{C_k\}$. To synthesize the CW tone $g(t) = A\cos(\omega_\mathrm{c}t + \phi)$, we set $B_k = 0$ and $\varphi_k = 0$ for all k except $k = k_\mathrm{c} = 2\pi f_\mathrm{c}/\Delta f = 2\pi N f_\mathrm{c}/f_\mathrm{s}$, where $B_{k_\mathrm{c}} = A$ and $\varphi_{k_\mathrm{c}} = \phi$. This desired spectrum for $\{C_k\}$ is obtained by solving the matrix equation

$$\mathbf{XQ} = \mathbf{U}, \tag{12}$$

where the elements of $\mathbf{X}$ and $\mathbf{U}$ are defined as

$$X_{kn} = \frac{1}{N}\mathrm{sinc}\left(\frac{k\pi}{N}\right)e^{-jk\pi\frac{(2n+1)}{N}} \tag{13a}$$

$$U_k = \begin{cases} Ae^{j\phi} & k = k_\mathrm{c} \\ 0 & \text{otherwise} \end{cases} \tag{13b}$$

for $k, n = 0, 1, \ldots, N-1$. The least-squares solution is

$$\mathbf{Q} = \mathbf{X}^\dagger\mathbf{U}, \tag{14}$$

giving the optimal Q_n amplitudes for the S&H signal.

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