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A simplified and high yield method for Micro-LED integration: Substitution of metal bumps with conductive photoresist in high-precision mass transfer

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ABSTRACT

With the rapid development of Micro-light-emitting diode (Micro-LED) technology, its application in the display field is promising. However, the precise electrical connection between Micro-LEDs and driver substrates remains a key challenge to achieve their large-scale commercialization. Conventional metal bump preparation processes usually rely on complex lift-off techniques, which not only increase the complexity of the process steps, but also face operational risks and are difficult to meet the demands of smaller pixel sizes and pitches. To this end, this study proposes an innovative approach using photoresist bumps instead of conventional metal bumps for the electrical connection between Micro-LEDs and driver substrates. By customized conductive photoresist as a conductive medium and combined with a proven photolithography process, it is possible to accurately prepare photoresist bumps to a predetermined position on the driver substrate without the need for a complex metal deposition process. This method significantly simplifies the tedious steps in the conventional process and improves the preparation efficiency and process stability. In the study, we combined the laser transfer technique with the photoresist bumping method to successfully transfer micro-LEDs with a size of 30×15 μm^2 from a sapphire substrate to a transparent 1.98-in. low-temperature polycrystalline silicon thin-film transistors (LTPS-TFT) driver substrate with high precision and good process repeatability. The technology simplifies the process while effectively reducing costs, providing technical support for the large-scale production and commercial application of Micro-LED display technology. In addition, the method relies on mature lithography technology and has the advantage of compatibility with existing semiconductor manufacturing processes, which has a strong potential for industrial promotion. Although this study focuses on the transfer process of Micro-LEDs, the proposed technological solution also has a wide range of application prospects, especially in the high-precision transfer and conductive bump preparation of other micro/nano devices.

1. Introduction

With the continuous advancement of display technologies, Micro-light-emitting diode (Micro-LED) has gradually emerged as one of the most promising next-generation display technologies in the semiconductor display field. Compared to traditional display technologies such as liquid crystal display (LCD) [1–3], quantum dot light emitting diodes (QLED) [4–6], and organic light-emitting diode (OLED) [7–9], Micro-LED offers numerous significant advantages [10–14], including self-emissive properties, fast response times, low power consumption, high brightness, and long lifespan. These advantages make Micro-LED a highly promising technology across various application fields. For instance, Micro-LED can be applied not only to large-size displays [15] but also to small devices, such as smartwatch screens [16]. Additionally, Micro-LED holds potential applications in emerging fields such as visible light communication [17–19]. However, despite its numerous advantages, the commercialization of Micro-LED technology is still not fully realized. One of the key challenges in the development of Micro-LED

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displays lies in the need to precisely control each Micro-LED through a complex driving substrate. Currently, existing technologies are unable to directly epitaxially grow Micro-LEDs on the driving substrate; epitaxial growth [20] is typically performed on sapphire substrates. This limitation presents a significant challenge for integrating Micro-LEDs with driving substrates. At present, the integration of Micro-LEDs with driving substrates mainly relies on mass transfer [10,13,14,20,21] technology. This technology involves the precise transfer of millions of Micro-LEDs from sapphire substrates to driving substrates with a displacement accuracy of less than 2 μm. As a result, mass transfer technology is considered the core challenge in the development of Micro-LED display technology.

Currently, common mass transfer technologies include laser transfer [10,14,22–24], stamp transfer [20,25,26], and electromagnetic transfer [27,28] (Indicators of these technical routes are compared in Table S1, Supporting Information). In most processes, the first step typically involves using laser technology to transfer Micro-LED chips from the growth substrate to temporary substrate. In the second step, the chips are precisely transferred from the temporary substrate to the driving substrate using specific transfer methods. For instance, in stamp transfer technology, custom stamp molds with pillar structures matching the spacing of the driving substrate are required to pick up and release the chips [26]. In contrast, electromagnetic transfer technology requires programmable magnetic control modules to generate magnetic forces, and Micro-LED chips must be specially prepared with a magnetic alloy layer to facilitate the process [28]. Compared to these methods, directly utilizing laser transfer technology in the second step to move chips from the intermediate substrate to the driving substrate offers significant efficiency advantages. Laser transfer eliminates the need for additional physical handling steps, enabling programmable chip alignment and the precise arrangement of Micro-LED chips at any desired spacing on the target substrate. This capability greatly enhances overall transfer efficiency. During this transfer process, the electrical connection between the Micro-LEDs and the driving substrate is a critical aspect, as it directly determines the functionality and stability of the chips. These electrical connections typically rely on conductive materials, with metallic bumps (e.g., indium [29,30], gold [31,32], tin [33–35]) being the most commonly used. To precisely fabricate these metallic bumps on the pads of the driving substrate, traditional processes often employ complex lift-off [36,37] techniques, which involve steps such as photolithography, deposition, and resist removal. However, this approach poses operational risks, such as incomplete removal of metal films along with the photoresist. In addition, as the pixel size gradually decreases and the pixel pitch decreases, the bumps need to achieve finer control over their size while maintaining sufficient density, which undoubtedly increases the difficulty of the lift-off process. Under laboratory conditions, due to conservative temperature settings and limited processing throughput, the deposition and resist removal steps may take more than 12 h. In industrial environments, this time can be significantly reduced to within 2 h through process optimization. However, despite the reduction in processing time, the overall efficiency and stability of the process are still constrained. Therefore, simplifying the fabrication process for metallic bumps is essential for improving overall process stability and efficiency. By optimizing this critical step, it is possible to reduce operational complexity while enhancing the production efficiency of Micro-LED display technologies, thereby accelerating their commercialization and large-scale application.

To address the integration challenges of Micro-LEDs with driving substrates, this study proposes an innovative approach that employs high-resolution conductive photoresist bumps to replace conventional metal bumps for electrical interconnection. By leveraging mature photolithography processes, the conductive photoresist can be precisely patterned on designated areas of the LTPS-TFT substrate, eliminating complex lift-off and metal deposition steps. This simplification reduces processing time by approximately 80 %. This method is integrated with laser transfer technology to accurately place 30 × 15 μm^2 Micro-LEDs from a sapphire wafer onto a 1.98-in. transparent LTPS-TFT substrate with alignment precision better than 1.5 μm. In addition to simplifying the process flow and reducing fabrication complexity, this approach offers improved efficiency, lower cost, and strong compatibility with standard semiconductor manufacturing processes. While this work focuses on Micro-LED transfer, the proposed method is broadly applicable to other micro/nano devices requiring precise and reliable electrical interconnections.

2. Method

2.1. Photoresist bump preparation

The process for fabricating conductive photoresist bumps on the LTPS-TFT driving substrate is shown in Fig. 1. First, the conductive photoresist is uniformly coated onto the surface of the driving substrate using a spin-coating method. Subsequently, the process proceeds with pre-baking, exposure, and development steps to form conductive photoresist bumps with a precisely arranged array structure. Compared to traditional lift-off processes, this method eliminates the need for metal deposition and the removal of photoresist, reducing the number of complex steps involved. By utilizing mature photolithography technology, the bump fabrication can be accomplished with ease, significantly simplifying the overall process. This improvement not only reduces process steps and operational complexity but also enhances fabrication efficiency and the stability of the process. The conductive photoresist employed in this study is a commercially available material sourced from Toray Industries, Inc. Although its cost is higher than that of conventional non-conductive photoresists, it eliminates the need for metal deposition and lift-off processes, thereby simplifying the overall fabrication procedure and improving production efficiency. Furthermore, based on over 80 experimental trials, the material exhibits excellent batch-to-batch consistency and stable electrical performance, underscoring its reliability for practical applications.

2.2. Laser transfer preparation chip on carrier (COC)

The process of transferring Micro-LED chips from the sapphire substrate to the carrier is shown in Fig. 2. First, the Chip on Wafer (COW) is temporarily bonded to Carrier 1 (Laser transfer materials 1, LTM-1). Subsequently, a laser is used to irradiate and separate the sapphire substrate from the Micro-LED chips, resulting in COC 1. Next, laser irradiation is applied again to the LTM-1 material, transferring the chips from Carrier 1 to Carrier 2 with the desired spacing, thereby achieving the preparation of COC 2, which provides the necessary material for the subsequent bonding process.

2.3. Bonding

Fig. 3 illustrates the bonding process of Micro-LEDs. In the previous steps, the photolithographic adhesive bump-driven substrate and the COC 2 structure obtained through laser transfer were first prepared. Subsequently, an accurate bonding process was used to combine these two components, establishing the electrical connection between the Micro-LED chip and the driver substrate. During this process, a bonding device is employed to precisely align the COC 2 and the driver substrate, ensuring that each Micro-LED chip is successfully bonded to the driver substrate, thus enabling proper chip driving. The key aspect of this step is ensuring a reliable connection between the chip and the substrate, which is essential for maintaining the stability and functionality of the display performance.

3. Results and discussion

The Micro-LED is prepared on sapphire and its type is flip-chip structure. The driver circuit is prepared on polyimide substrate and

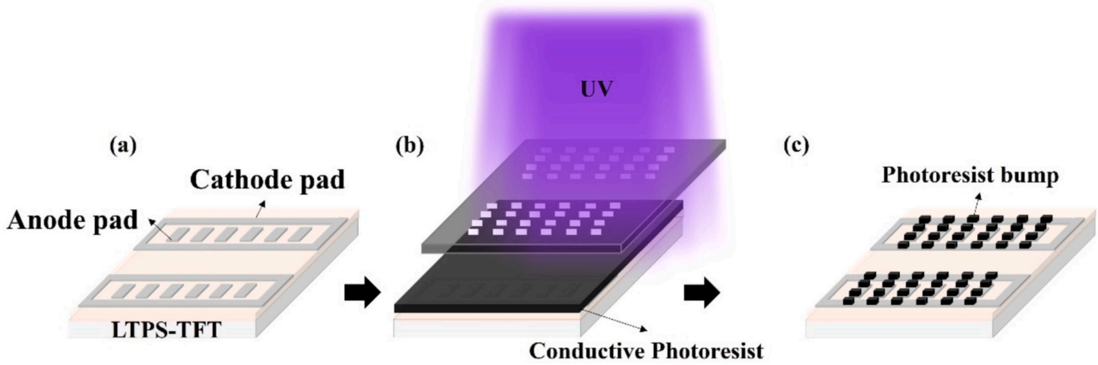

Fig. 1. Schematic of the process for preparing photoresist bumps. Spin-coating of conductive photoresists on (a) LTPS-TFT backplane, (b) UV exposure and (c) development.

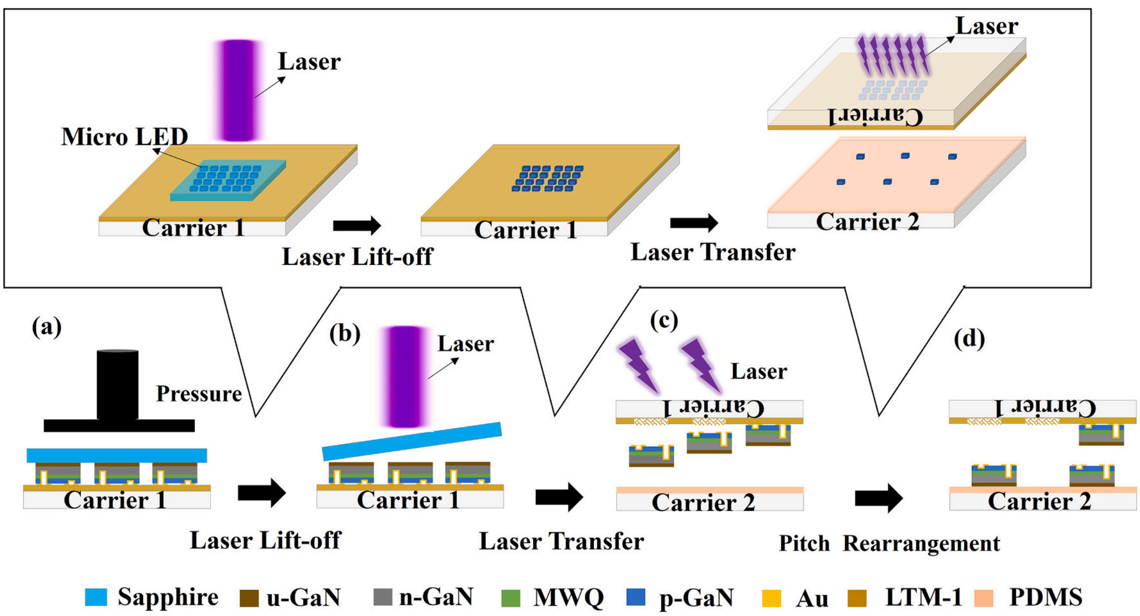

Fig. 2. Schematic diagram of the process for the preparation of COC 2. The (a) COW is temporarily bonded to carrier 1, followed by (b) laser stripping of the sapphire substrate, and again using (c) laser irradiation of LTM-1 on the carrier to achieve a specific pitch transfer to the chip to (d) obtain the COC 2.

the type of the driver circuit is LTPS-TFT. The cross-sectional schematic, top-view schematic image of the flip-chip Micro-LED and the optical image of the fabricated flip-chip are shown in Fig. 4a-c, respectively. The size of the Micro-LED chip in this paper is 30 × 15 μm^2.

3.1. Photoresist bump preparation

The preparation of photoresist bumps was firstly optimized in terms of parameters on a glass substrate, and the relevant results are shown in Fig. 5. The main components of photoresist bumps are conductive carbon black and photosensitive resins which are organic substances. After curing and exposure in the photolithography process, these organic components will be evaporated, so that the proportion of organic substances in the photoresist bumps is significantly reduced. In the development process, the unexposed organic substances will be dissolved by the development solution, and if the development process is not properly controlled, it may lead to excessive dissolution of the photoresist bump, which may trigger the bump to fall off. Therefore, the preparation of photoresist bumps requires high development conditions, especially the precise control of the development time at a fixed temperature and concentration.

The optimization of the development time is especially critical when the temperature is stabilized at 30 °C. Through experiments, we found that the best results were achieved when the development time was controlled between 30 and 35 s. Specifically, as shown in Fig. 5a, when the development time is 25 s, the photoresist bumps are not developed enough, resulting in the interconnection of the bumps corresponding to the two electrodes of the chip, which leads to a short circuit. On the contrary, as shown in Fig. 5b, when the development time is extended to 40 s, overdevelopment occurs, and part of the photoresist bumps fall off. Ideal development occurred at 32 s, as shown in Fig. 5c, when no photoresist bumps were detached or interconnected. The photoresist bumps were further characterized using scanning electron microscopy (SEM) and the results are shown in Fig. 5d. We acknowledge that in our experiments, the development time is indeed highly sensitive. This sensitivity primarily arises because, in our laboratory setting, we do not have access to dedicated spray development equipment, which would typically ensure a more uniform and controlled development process in an industrial environment. Instead, our current development method relies on manual processes, leading to a narrower process window. In addition, the cross-section of individual photoresist bumps on the glass substrate was observed using focused ion beam (FIB), and the internal elements of the bumps were analyzed by energy dispersive spectroscopy (EDS), and the results are shown in Fig. 6. The results show that the

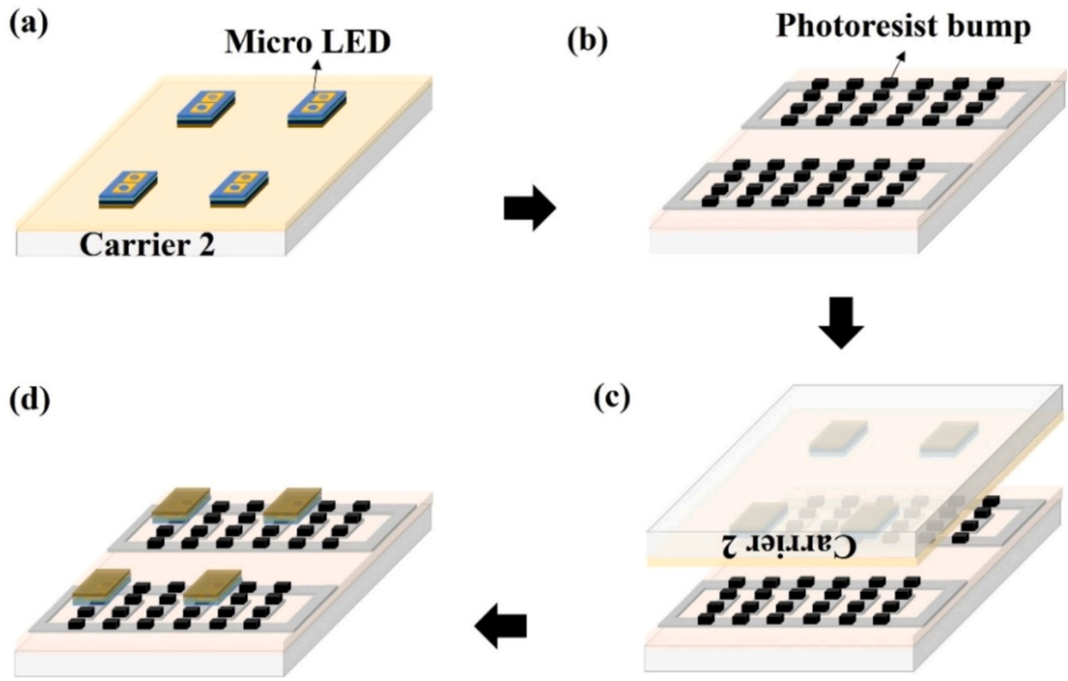

Fig. 3. Schematic diagram of the COC2 on driver substrate bonding process. (a) The COC2 prepared by laser transfer and (b) the driver substrate with photoresist bumps already prepared are (c) bonded in precise alignment by the bonding equipment, and (d) the chip is successfully transferred to the driver substrate.

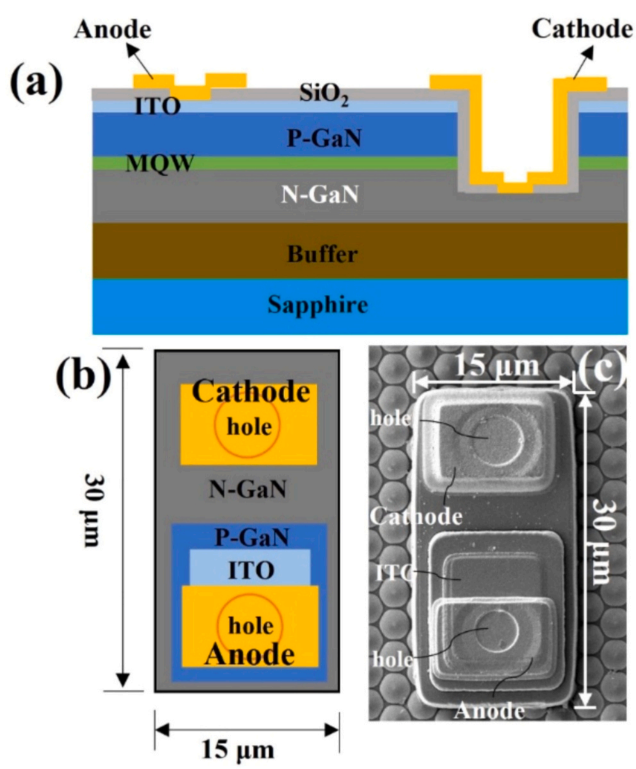

Fig. 4. Schematic cross-section of flip chip LED structure (a) with the top view (b) and optical image of Micro-LEDs (c) with a chip size of 30 × 15 μm^2.

height of the photoresist bumps on the glass substrate is about 3 μm, and the percentage of carbon (C) and oxygen (O) elements inside the bumps are 74.37 % and 25.63 %, respectively. After optimizing the suitable photoresist bump parameters on the glass substrate, we carried out the preparation of photoresist bumps on a formal LTPS-TFT driver substrate, and the results are shown in Fig. 7. Through the photolithography process, the photoresist bumps are uniformly distributed on the LTPS-TFT driver substrate. The uniformity of the photoresist bumps was measured to be 2.6 % according to Eq. 1 [22,38,39], where H_m is the maximum value of the bump height, H_l is the minimum value of the bump height, and H_a is the average value of the bump height. The variance of the photoresist bump is about 0.0015 μm^2 with a standard deviation of 0.0362 μm. This result proved the effectiveness and stability of the preparation method.

$$Uniformity = \frac{H_m - H_l}{2H_a} \times 100\% \tag{1}$$

3.2. Chip transfer

We use laser technology for the transfer of Micro-LED chips, which is a two-stage process. The first stage is to transfer the chip from the source substrate (sapphire) to a temporary substrate and to separate the sapphire substrate from the chip; the second stage is to transfer the chip from the temporary substrate to the target carrier 2.

In the first stage, in order to ensure a mismatch-free transfer of the chip array onto the temporary substrate, the COW first needs to be pre-bonded to the temporary substrate. Next, a laser focus is used to irradiate the interface between the buffer layer and the sapphire, where the buffer layer is mainly composed of U-shaped gallium nitride (GaN). After laser irradiation, GaN decomposes into liquid gallium and nitrogen, which results in the separation of the chip from the sapphire substrate by the reaction equation:

$$2GaN \rightarrow 2Ga(l) + N_2(g) \tag{2}$$

In the second stage, the chips have been transferred to a temporary substrate. However, since the chip arrays are more closely pitch on 4-in. wafers in order to improve wafer utilization during the fabrication of COWs, the pitch of the chip rows on the temporary substrate is still too dense and does not correspond to the pitch required for subsequent transfer. To solve this problem, we use laser irradiation of a temporary substrate (LTM-1), which is a photosensitive material that expands under lase r irradiation, to push the chips apart and transfer them to a target carrier 2 with a predetermined pitch. Through this expansion

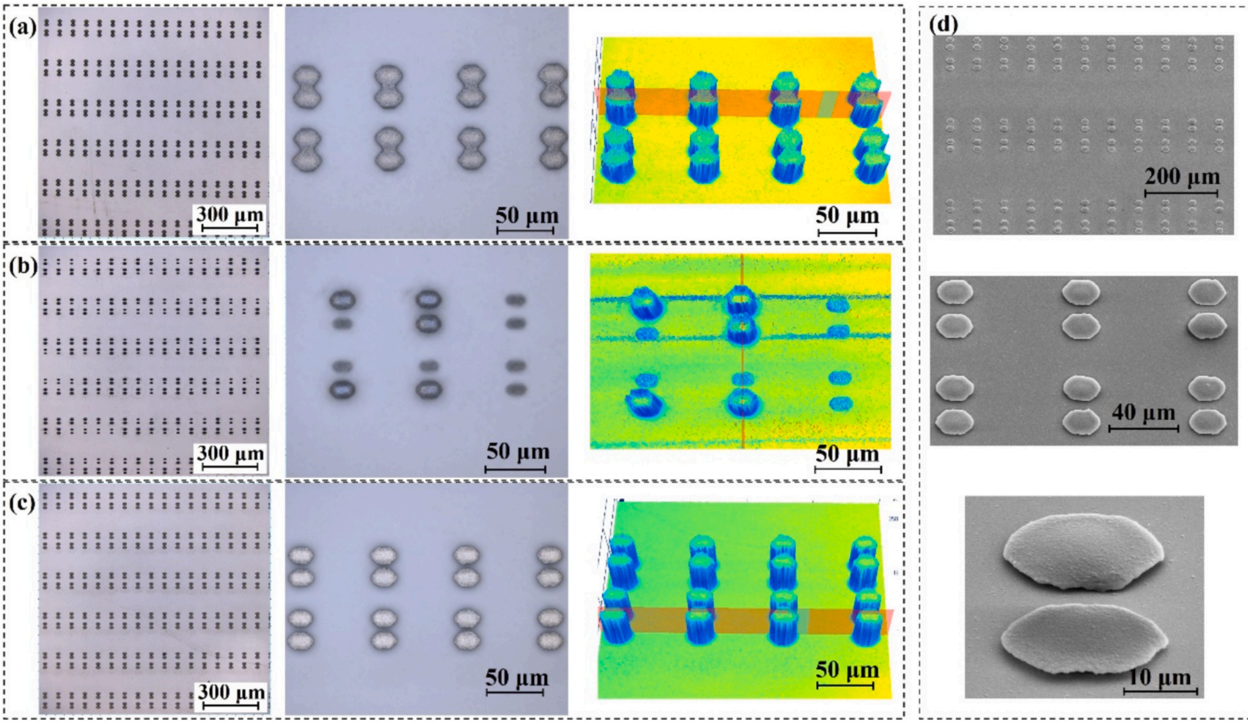

Fig. 5. The results of the preparation of photoresist bumps on glass with different development times ((a) 25 s, (b) 40s and (c) 32 s, respectively) are shown. The left figure shows the low-magnification microscope image, the middle figure shows the high-magnification microscope image, and the right figure shows the 3D imaging results. Also shown in (d) are SEM images of good photoresist bumps.

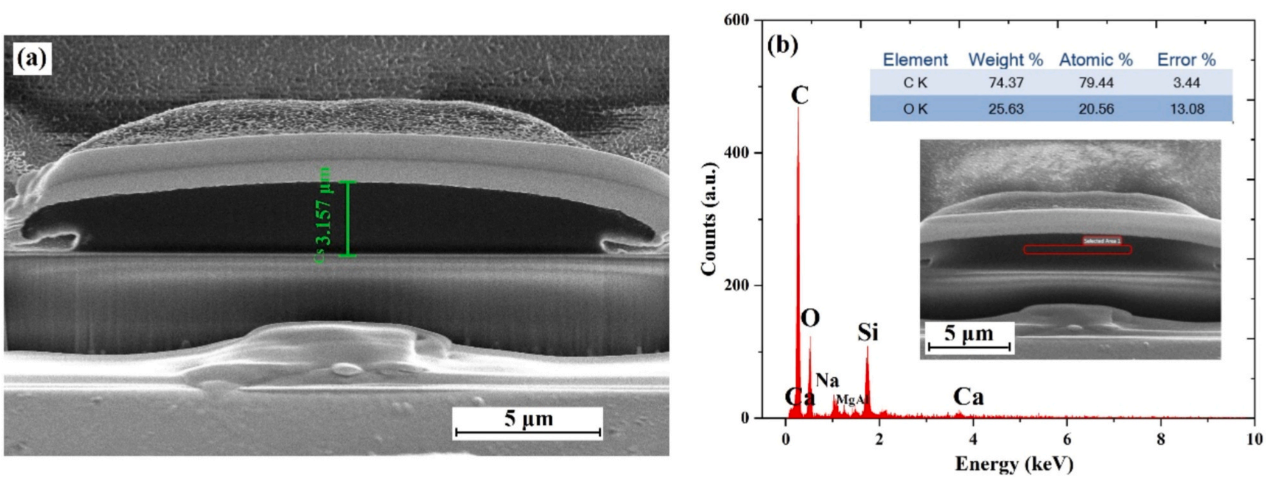

Fig. 6. A (a) cross-section of a single bump on the glass and a plot of (b) the results of the EDS analysis inside the bump are shown.

effect caused by laser irradiation, the position and spacing of the chips can be precisely adjusted to achieve on-demand transfer.

The experimental results of the transfer process are shown in Fig. 8. Fig. 8a shows the 4-in. COW sample we used and its microscopic image; Fig. 8b shows the image after cutting the COW into small pieces and bonding it to a temporary substrate and the sapphire substrate has been removed, and shows the microscopic image of the chip array on the temporary substrate; Fig. 8c shows the process of transferring the chip from the temporary substrate to the target carrier 2, and the figure includes both macroscopic view and microscopic image. To verify the feasibility of the adopted transfer process, we measured the I-V characteristics of the chip before and after the transfer, and the results are shown in Fig. 8d. At the same time, we also measured the I-V characteristics of multiple regions of the chip to assess the uniformity of the transfer process. In order to demonstrate these test results more intuitively, we show the I-V curves with a representative turn-on voltage as the vertical coordinate, and the results are shown in Fig. 7e, which further validate the feasibility and uniformity of the transfer process.

In the first stage of chip transfer, we achieved a transfer yield of approximately 99.99 % without any displacement problems. During this stage, we successfully transferred approximately 190,000 chips, of which only about 19 were damaged or missing (The process of detecting missing/damaged chips is detailed in Section S3 and Fig. S2, Supporting Information). The transfer yield for the second stage was 100 %, with 6400 chips successfully transferred, within 1.5 μm of displacement, and without any damage or missing chips. In order to ensure the final transfer quality and yield of 100 %, we repaired the bad dots found during the transfer process. The repair process is shown in Fig. 9: first, a

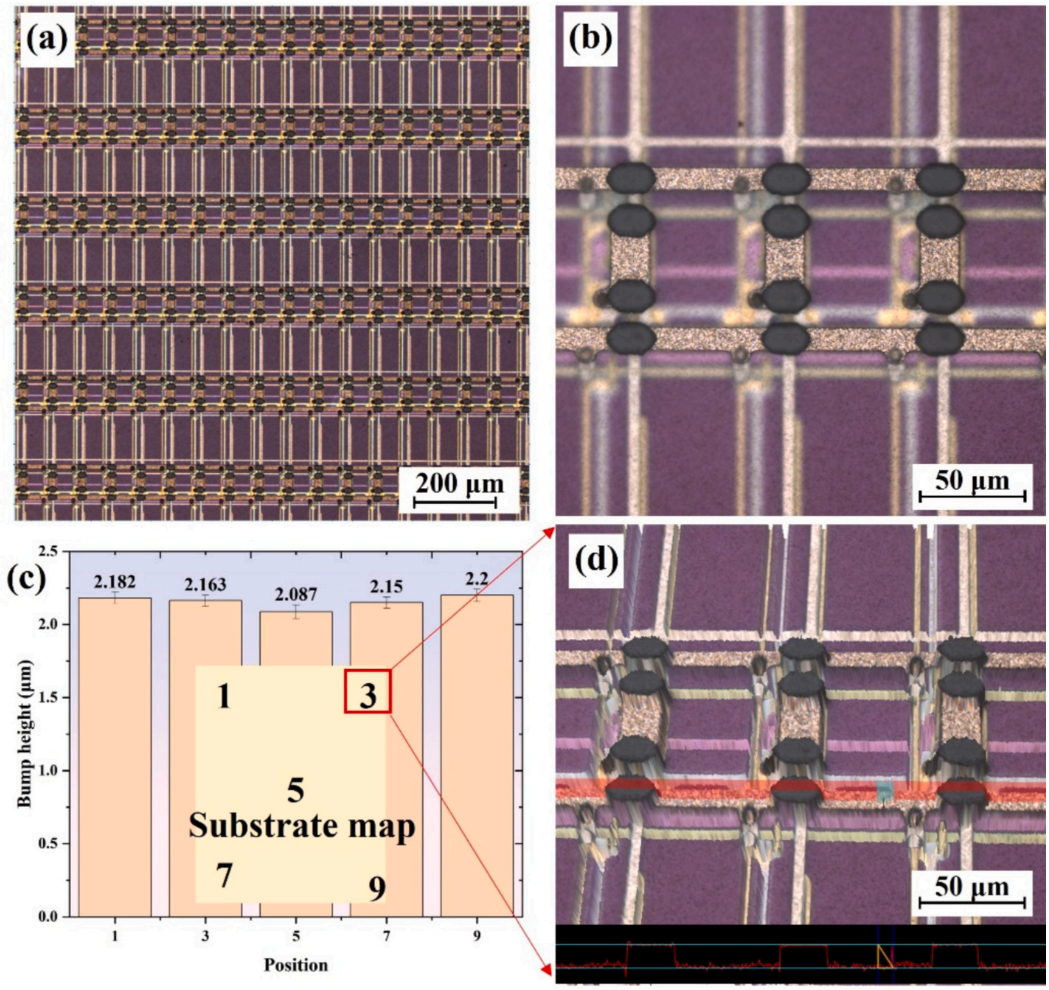

Fig. 7. The results of preparing photoresist bumps on LTPS-TFTs are shown. Optical microscope images at (a) low and (b) high magnification, as well as (c) photoresist bump height distribution and (d) 3D images on the substrate are shown, respectively.

laser with a wavelength of 532 nm was used to accurately remove the damaged chip, and then a new chip was added in the original position until all the damaged or missing chips were repaired and the chip was intact. This repair process effectively improves the overall transfer yield and further ensures the integrity and functionality of the chip.

3.3. Bonding of the chip to the driver substrate

After the successful preparation of the photoresist bump and COC 2 as mentioned above, the next step is to bond the two in high precision alignment. For this purpose, we have adopted a high-precision bonding device that supports simultaneous heating of COC 2 and LTPS-TFT. This heating mechanism enables precise control of the bonding temperature to optimize the bonding effect. In the specific operation, we heated the LTPS-TFT driver substrate to 40 °C and preheated the photoresist bumps to ensure that they are appropriately flexible and do not harden too much during the bonding contact. At the same time, the COC 2 was heated to 180 °C to ensure that the chip could heat the photoresist bumps during the bonding process so that they would melt and fully fuse with the chip. After completing the temperature preset, we accurately aligned the COC 2 with the LTPS-TFT driver substrate, and then applied a pressure of 1.2 MPa for bonding. After the bonding was completed, the system was cooled down to room temperature to ensure that the photoresist bumps were firmly adhered to the chip. Subsequently, the Carrier was separated from the LTPS-TFT substrate and the chip was successfully bonded to the LTPS-TFT driver substrate. The key parameters (e.g., temperature and pressure) in the bonding process were analyzed in detail and the possible abnormalities were summarized, and the results are shown in Fig. 10.

The results of the bonding experiment are shown in Fig. 11. We first tried the bonding operation on glass, and the results are shown in Fig. 11a. The red box markings show that the Micro-LED chip was successfully bonded to the photoresist bumps with a displacement offset of less than 1.5 µm. Subsequently, the chip was bonded to the LTPS-TFT driver substrate under the same bonding conditions, and the results are shown in Fig. 11b. The SEM image after bonding is shown in Fig. 11c, and the overall bonding effect is good, although the blurring of some areas is due to the blurring of the poor conductivity SEM observation due to the undeposited metal on the surface at the time of observation. To further verify the appropriateness of the bonding conditions, we performed a FIB cross-section observation of the bonded Micro-LED chip, and the results show that the chip electrodes are in intact contact with the photoresist bumps, as shown in Fig. 11d.

After the chip has been successfully bonded to the LTPS-TFT driver substrate, subsequent processing is still required. The conductivity of photoresist bumps is mainly dependent on the amount of carbon black in them. It has been shown [40] that the conductivity of an individual photoresist bump is closely related to the percentage of carbon black within the bump: the higher the percentage of carbon black, the better the conductivity, and conversely, the poorer the conductivity. However, most of the organic substances inside the photoresist bumps have a low boiling point, usually not exceeding 150 °C. The organic substances

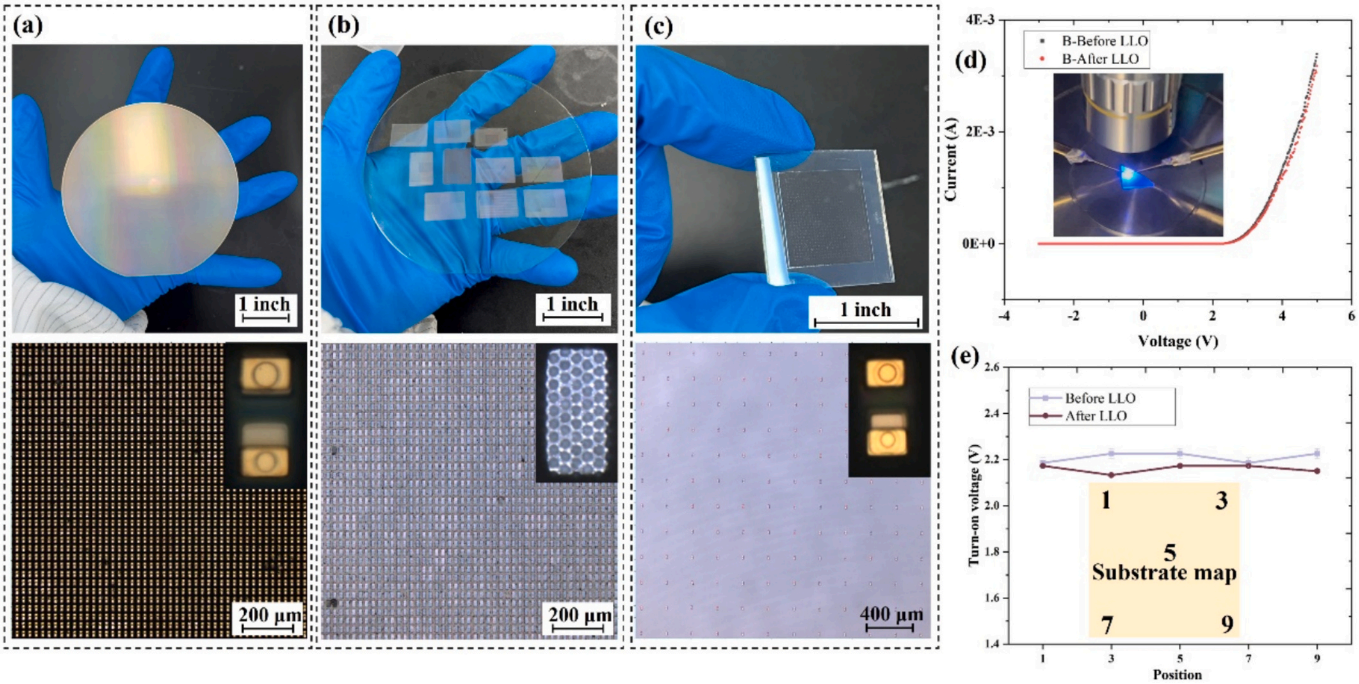

Fig. 8. Chip transfer process. The top image in (a) shows a micro-LED array fabricated on a 4-in. sapphire substrate. Below is a magnified portion of the Micro-LED array. (b) The top image shows the Micro-LED array left on carrier 1 after the LLO process, and the bottom image shows a portion of the array at a higher magnification. The upper panel of (c) shows the Micro-LED arrays further transferred to carrier 2 and arranged at a specific pitch. The following shows a higher magnification image of the same array. (d) Shows the I-V characteristics of the Micro-LEDs before and after the transfer, and (e) measures the uniformity of the transfer.

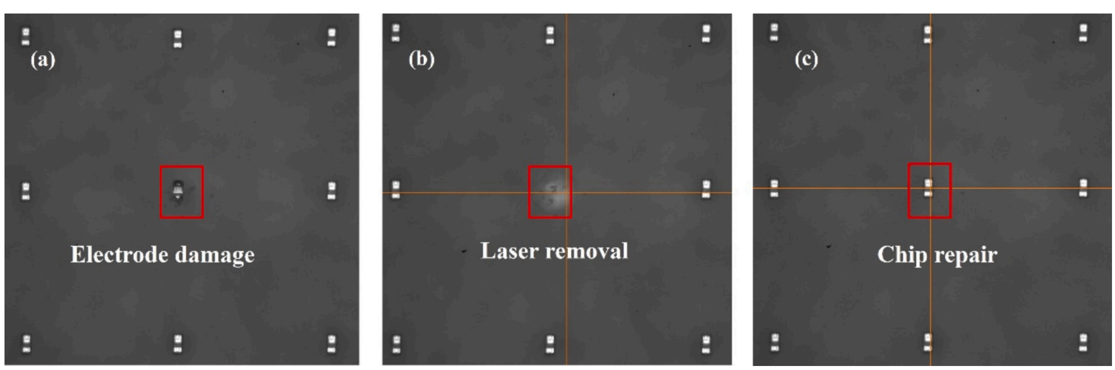

Fig. 9. COC2 repair schematic. (a) a chip with electrode damage, (b) a chip that has been removed with a laser at a wavelength of 532 nm, and (c) re-transferred a new chip from carrier 1 to be repaired.

inside the photoresist bumps can be removed by a baking process. Therefore, these organic substances can be removed through a baking process to enhance the relative proportion of carbon black, thereby enhancing the conductivity. Specifically, we placed the bonded substrate into an oven at 200 °C for 20 min to volatilize the organic substances inside the photoresist bumps, which in turn improves the percentage of carbon black and enhances the electrical conductivity. This baking step is critical for improving the conductivity. Fig. 12 demonstrates the changes in the photoresist bumps before and after baking. Fig. 12a shows the schematic and SEM image of the photoresist bump before baking; Fig. 12b shows the schematic and SEM image of the photoresist bump after baking. It is obvious that after baking at 200 °C for 20 min, the internal organic matter is significantly reduced resulting in a significant decrease in the height of the photoresist bump and an increase in the relative proportion of carbon black. Fig. 12c shows a schematic and SEM image of the chip bonded to the photoresist bump and after completion of baking, further demonstrating that this method can significantly improve the conductivity and overall stability after bonding. In addition, since the conductive material used is carbon black, which is less conductive than metal bumps (indium, gold, tin, etc.), the interconnecting portion between the Micro-LED chip and the driver substrate will be subjected to more voltages when the device is in operation, further generating more heat. To explore this issue, we conducted infrared thermography experiments to evaluate the thermal impact of photoresist bumps under operating conditions. The results are shown in Fig. 13, which shows the thermal distributions of devices using conventional metal bumps and conductive photoresist bumps in Fig. 13 (a) and (b), respectively. Our observations show that the temperature increase in the conductive photoresist-based interconnect stays within acceptable limits, with the maximum temperature difference observed being about 1.4 °C compared to the metal bump configuration, suggesting that although the conductivity of the photoresist bumps is lower than that of the metal, the actual thermal impact is minimal under our test conditions. Therefore, we believe that the proposed method is still

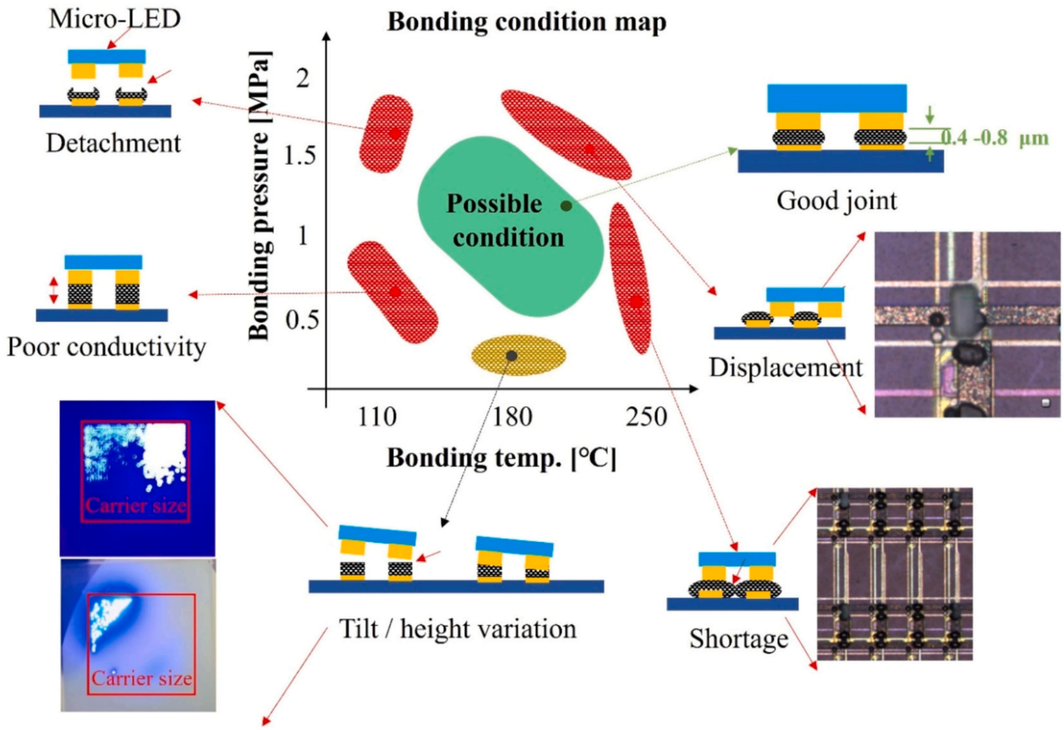

Fig. 10. A schematic illustration of the bonding conditions of photoresist bumps and COC2 at different pressures and temperatures.

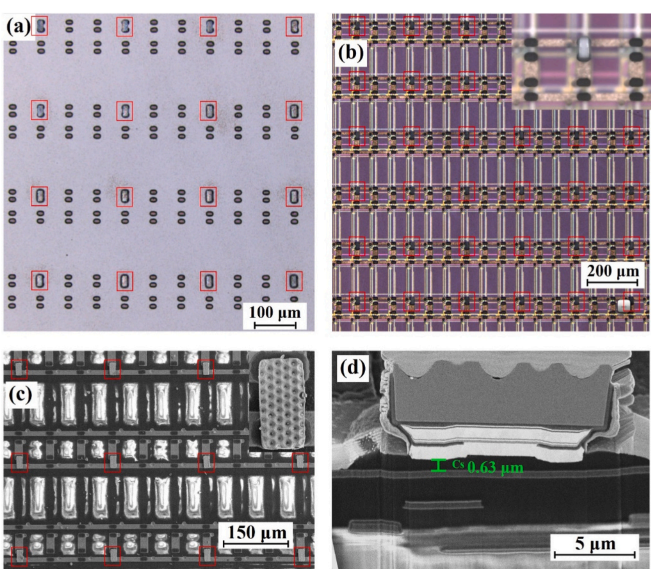

Fig. 11. Chip bonding results. Bonding experiments were first performed on a glass substrate, and then the bonding process was transferred to an LTPS-TFT driver substrate for testing. (a) and (b) show the bonding on glass substrate and LTPS-TFT substrate, respectively. (c) shows the SEM characterization results after successful bonding, while (d) shows the chip cross-section after successful bonding, observed by FIB technique.

viable for Micro-LED applications, especially in low-power display scenarios. Nevertheless, we acknowledge that for high-power applications, further optimization of the conductive photoresist formulation (e.g., somehow indicates the incorporating high-conductivity fillers such as silver nanowires or graphene) may be required.

Fig. 14 shows our results in the final bonding process of COC 2 to LTPS-TFT, where Fig. 14a and Fig. 14b show the comparison diagrams before and after baking, respectively. It is obvious from the graphs that the yield was significantly improved after the baking process, and we also tried to increase the temperature and extend the baking time, and the final lighting was not improved. Some areas in the figure show obvious unlit and darkened phenomena, which is not due to the unsuccessful bonding of the chip, but due to the damage of the LTPS-TFT internal lines. In the end, we achieved a yield of about 99 % on a 1.98-in. LTPS-TFT substrate, as shown in Fig. 14c. A total of 25,600 chips were bonded, of which about 245 chip dots were not lighted, indicating that the majority of the chips were successfully bonded and functioned properly.

The optical performance of the LTPS-TFT after successful device activation was thoroughly evaluated. As shown in Fig. 15, the measurement system used for the characterization is illustrated in Fig. 15(a), where a high-precision optical setup was employed to ensure accurate detection of electroluminescence. The EL spectrum of the device, shown in Fig. 15(b), exhibits a strong emission peak at 465.6 nm, with a full width at half maximum (FWHM) of approximately 19.3 nm, indicating high spectral purity and a narrow emission profile. The corresponding chromaticity coordinates were measured to be (0.1314, 0.0616), as shown in Fig. 15(c), confirming that the emitted light lies in the deep blue region of the CIE 1931 color space. These results demonstrate the excellent optical performance and color purity of the fabricated LTPS-TFT device. In addition, to demonstrate the potential of the proposed conductive photoresist bumps, we compared the optical and electrical performance of LTPS-TFT devices fabricated using our conductive photoresist bumps with those using conventional metal bumps. The measurement results are shown in Fig. 16. As illustrated in Fig. 16a, the bar chart presents the brightness of Micro-LED devices interconnected with different bump materials. The devices with conductive photoresist bumps exhibited a brightness of 2050 cd/m^2, compared to 2315 cd/m^2 for copper bumps and 2260 cd/m^2 for indium bumps. Although the brightness of the photoresist-based bumps was slightly lower, it remains within an acceptable range for practical applications. As shown in Fig. 16b, the I-V characteristics indicate that the conductive photoresist bumps have slightly higher resistance compared to their copper and indium counterparts. Nevertheless, the turn-on voltage of the Micro-

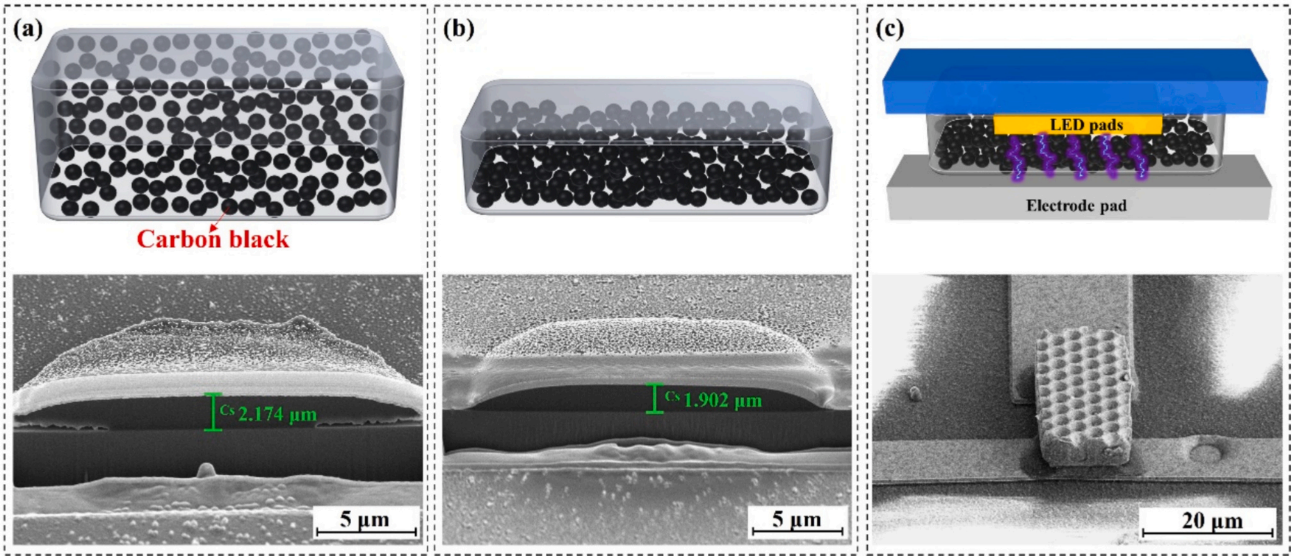

Fig. 12. Result of photoresist bumps baked at 200 °C for 20 min are shown. (a) The upper figure shows a schematic diagram of the photoresist bump before baking, and the lower figure shows a cross-section of the photoresist bump before baking. (b) The upper figure shows the schematic diagram of the photoresist after baking, and the lower figure shows the cross-section of the photoresist bump after baking. (c) The upper figure shows a schematic diagram of the chip conductivity through carbon black after the chip is bonded to the photoresist bump and baked, and the lower figure shows an SEM image of the chip bonded to the photoresist bump and baked.

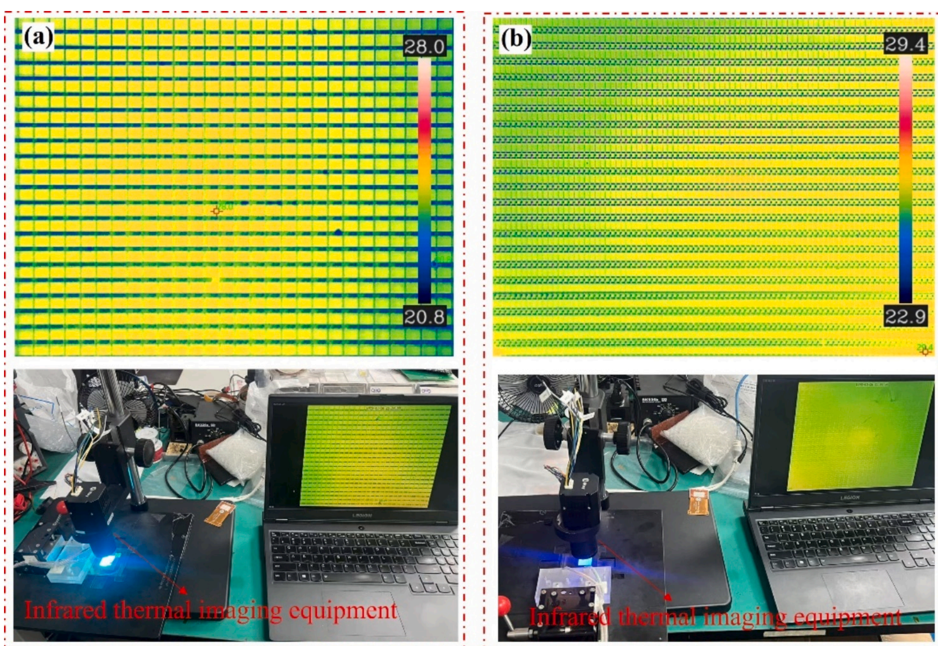

Fig. 13. Diagrams showing the results of infrared thermography of the metal bump and photoresist bump during operation. (a) Indium metal bump. (b) Photoresist bump.

LEDs remains relatively stable, and current conduction is still efficient, confirming the feasibility of using conductive photoresist bumps in display applications. However, to evaluate the long-term environmental reliability of the conductive photoresist bumps, we conducted a high-temperature and high-humidity (HTHH) stress test (see more details in Section S4 and Fig. S3, Supporting Information).

To evaluate the bonding strength, we performed mechanical testing on Micro-LED samples bonded onto LTPS-TFT substrates using a shear force measurement system (MFM1200, BS25G sensor, SH-062-001 shear blade). The test was conducted under ambient conditions at a speed of 300 μm/s. The detailed testing procedure is shown in Fig. 17a, with the probe moving in the direction indicated by the red arrow. The maximum shear force measured was 7 g. These results confirm that the photoresist bump bonding provides effective mechanical adhesion, especially considering the small size of the Micro-LED chips (30 × 15 μm^2). In addition, we performed additional shear tests on chips bonded to indium bumps and copper bumps under the same experimental conditions as described above, where the maximum shear force was measured to be 7.5 g for indium bumps and 9 g for copper bumps, and the results are shown in Fig. 17b. Although the bond strength is lower than that of conventional solder joints, it is sufficient for Micro-LED display applications where mechanical stress is usually limited.

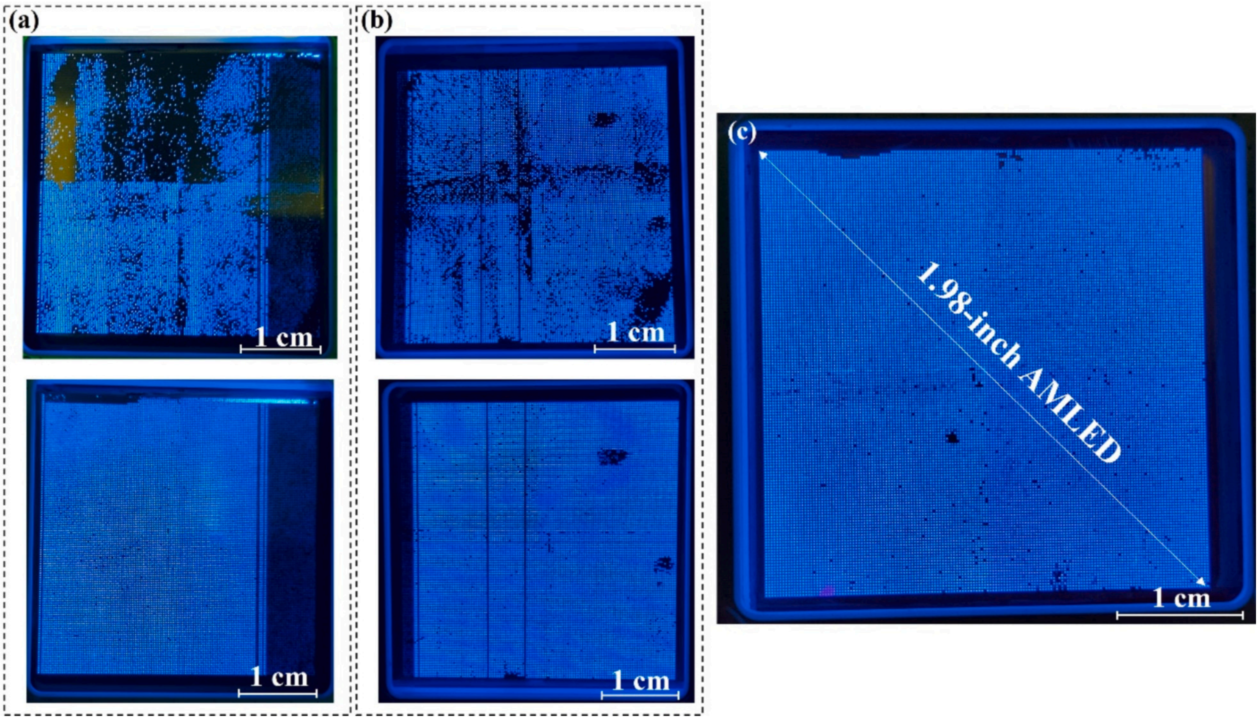

Fig. 14. Final result image of 1.98-in. LTPS-TFT driver substrate after bonding. (a) and (b) are both top images before baking at 200 °C after bonding, and the bottom images are after baking at 200 °C for 20 min after bonding. (c) shows our final active-matrix light-emitting diode (AMLED) display with 99 % bonding yield.

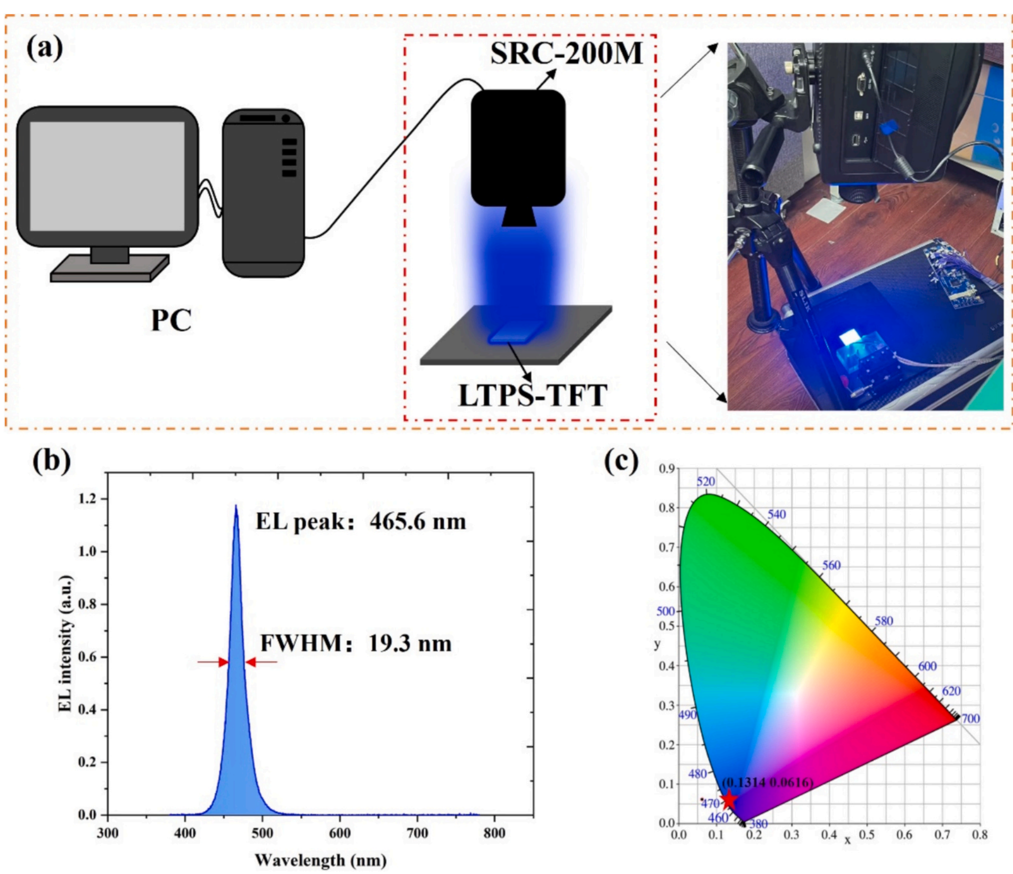

Fig. 15. Optical performance characterization of the LTPS-TFT driver substrate after bonding: (a) measurement setup, (b) emission spectrum, and (c) CIE 1931 chromaticity coordinates of the Micro-LED.

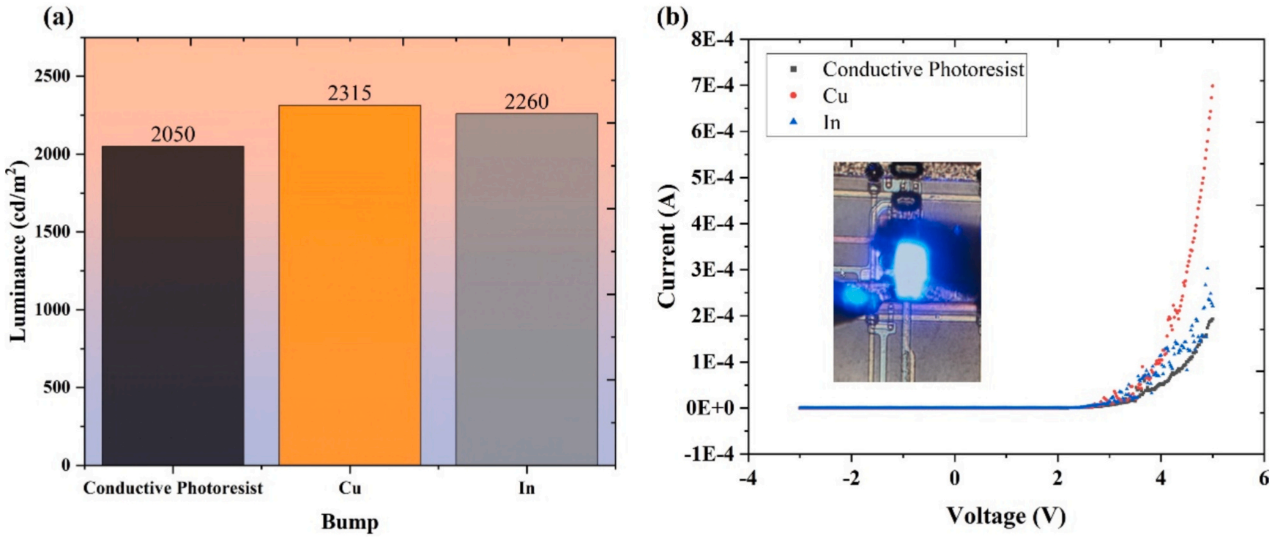

Fig. 16. Comparison of optical and electrical performance of LTPS-TFT devices using different bump materials: (a) brightness of Micro-LED devices with conductive photoresist, copper, and indium bumps; (b) I—V characteristics showing the electrical behavior of each device type.

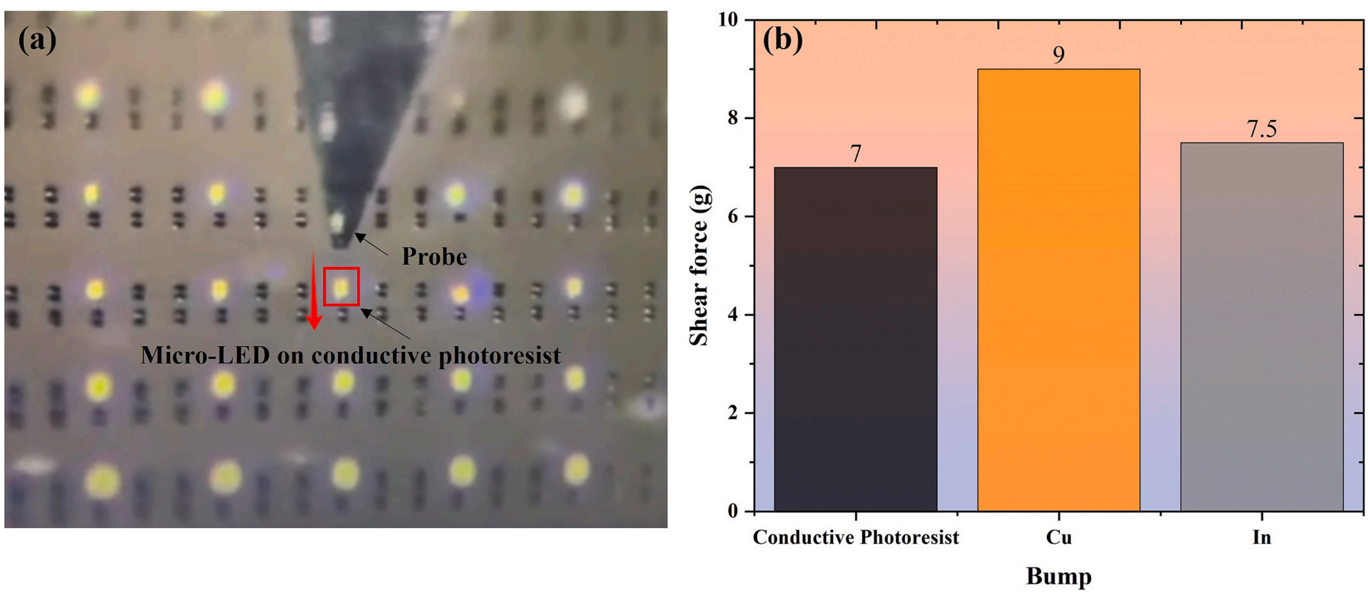

Fig. 17. Shear test. (a) shear force test procedure.; (b) Comparison of shear force for Micro-LEDs bonded to conductive photoresist, copper and indium bumps, respectively.

4. Conclusion

By using photoresist bumping technology, we have successfully avoided the complex lift-off process required for conventional metal bumping and achieved precise bumping by relying only on a mature photolithography process, which significantly improves the preparation efficiency and effectively reduces the risks involved in the process. Combined with laser transfer technology, we have successfully transferred densely distributed micro-LED chips with a size of 30 × 15 μm^2 from sapphire substrates to LTPS-TFT driver substrates with precisely controlled chip pitch (222 μm). During the process, the Micro-LED chip was successfully electrically connected and displayed properly with a final yield of 99 %. This achievement marks a significant advancement in our Micro-LED display technology, especially in terms of innovations in high-precision transfer and high-stability electrical connection. In addition, the advantage of photoresist bumping technology is not only the simplification of the process, but also its high adaptability and scalability. Due to the maturity of the photolithography process, this technology is ideally suited for large-scale production applications and is able to meet the needs of large-size displays. Combined with laser transfer technology, the entire process can significantly improve production efficiency while ensuring high precision and stability. Therefore, photoresist bumping technology not only has important application prospects in the field of Micro-LEDs, but can also be extended to the precision fabrication of other micro and nano devices, with extensive industrialization potential.

CRediT authorship contribution statement

Taifu Lang: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Resources, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Data curation, Conceptualization. **Xueqi Zhu:** Methodology, Formal analysis, Data curation, Conceptualization. **Xin Lin:**

Funding acquisition, Formal analysis, Data curation, Conceptualization. **Xiaowei Huang:** Methodology, Investigation. **Yujie Xie:** Investigation, Funding acquisition. **Shuaishuai Wang:** Software. **Shuangjia Bai:** Validation. **Xuehuang Tang:** Methodology. **Jin Li:** Formal analysis. **Jiawei Yuan:** Software. **Xinrui Huang:** Conceptualization. **Zhonghang Huang:** Investigation, Formal analysis. **Chang Lin:** Methodology, Investigation. **Jie Sun:** Writing – review & editing, Visualization, Validation, Project administration, Methodology. **Qun Yan:** Methodology, Funding acquisition, Formal analysis, Data curation, Conceptualization.

Declaration of competing interest

The authors declare no conflict of interest.

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Appendix A. Supplementary data

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