High-yield fabrication of bubble-free magic-angle twisted bilayer graphene devices with high twist-angle homogeneity

Citation for the original published paper (version of record):

Díez-Mérida, J., Das, I., Di Battista, G. et al (2025). High-yield fabrication of bubble-free magic-angle twisted bilayer graphene devices with high twist-angle homogeneity. Newton, 1(1). http://dx.doi.org/10.1016/j.newton.2024.100007

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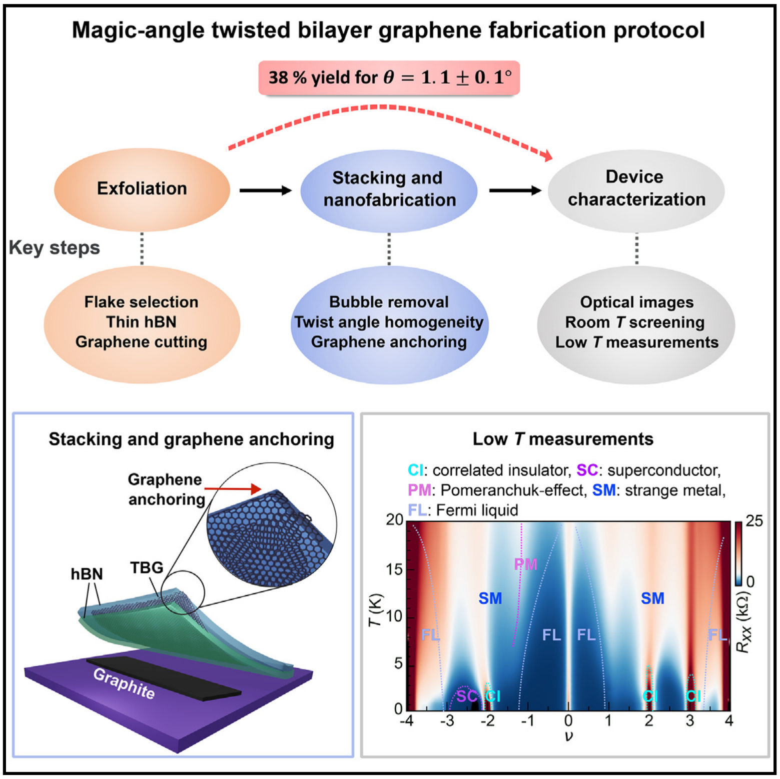
Graphical abstract



Highlights

- Curated protocol to fabricate magic-angle graphene devices with a 38% yield
- Locking the twist angle of MATBG by anchoring to the hBN edges
- Large-area bubble-free devices with high twist-angle homogeneity

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In brief

Improvements in the fabrication protocols of twisted moiré materials are key enablers to unlock the understanding of their rich physics. Díez-Mérida et al. report a protocol to successfully fabricate MATBG samples with high yield and twist-angle homogeneity. This is achieved by optimizing key parameters of the fabrication process, which include a careful flake selection, a controlled bubble-free lamination at a high temperature, and the development of a clamping technique to stabilize the twist angle.

Díez-Mérida et al., 2025, Newton *1*, 100007
March 3, 2025 © 2025 The Authors. Published by Elsevier Inc.
https://doi.org/10.1016/j.newton.2024.100007

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High-yield fabrication of bubble-free magic-angle twisted bilayer graphene devices with high twist-angle homogeneity

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https://doi.org/10.1016/j.newton.2024.100007

ACCESSIBLE OVERVIEW Two graphene layers that are stacked on top of each other with a specific value of the twist angle between the layers can display a plethora of exotic properties, ranging from strong electron correlation to topological effects and superconductivity. Such angles are ~1° and are called magic angles. The first of these MATBG devices were reported 6 years ago; however, to this day it remains challenging to fabricate devices with high reliability, as the fabrication procedure involves delicate manual processes. This work reports an optimized protocol for the fabrication of devices made from twisted bilayer graphene with a small twist angle (the so-called magic angle), demonstrating a high device yield of ~38% and small twist-angle variations, which result in homogeneous properties over areas as large as 36 μm^2. This is achieved thanks to a stabilization technique involving the anchoring of the graphene layer and a careful bubble-removal technique. The discussed protocols may be directly transferred to other 2D moiré materials and will be useful to researchers in this field to catalyze the study of these materials under reproducible conditions.

SUMMARY

Magic-angle twisted bilayer graphene (MATBG) is a very versatile material, hosting a wide variety of exotic phases while allowing easy tunability of material parameters. However, the fabrication of MATBG devices remains a challenging and inefficient manual process, with device properties being highly dependent on the specific fabrication methods, often resulting in inconsistency and variability. Here we present an optimized protocol for the fabrication of MATBG samples, using deterministic graphene anchoring to stabilize the twist angle and a careful bubble-removal technique to ensure high twist-angle homogeneity. We use low-temperature transport experiments to extract the average twist angle between pairs of leads. We find that up to ~38% of the devices show μm^2-sized regions with twist angles in the range of $\theta = 1.1 \pm 0.1^\circ$ and twist-angle variations of $\Delta\theta \leq 0.02^\circ$. In some instances, such regions were up to 36 μm^2 large. The discussed protocols may be directly transferred to non-graphene materials and will be useful for the growing field of moiré materials.

INTRODUCTION

The electronic flat bands in magic-angle twisted bilayer graphene (MATBG) have shown a rich abundance of emergent quantum phases, such as correlated insulators (CIs),[1–3] superconductors,[2–4] magnets,[5–7] non-trivial topological phases,[8–11] and strange metal phases.[12–14] Similar phases have been unraveled in other moiré materials, such as in twisted bilayers of transition metal dichalcogenides (TMDs)[15,16] and twisted mirror symmetric graphene multi-layers.[17–19] While extensive efforts have been dedicated to understanding the intricate ground states of these systems and what drives them, the community is still struggling to grasp the full details of its colorful phase diagrams. One big challenge endures—namely, device fabrication and sample quality. Fabrication of moiré materials remains notoriously tedious and low yield, and devices are quite sensitive to

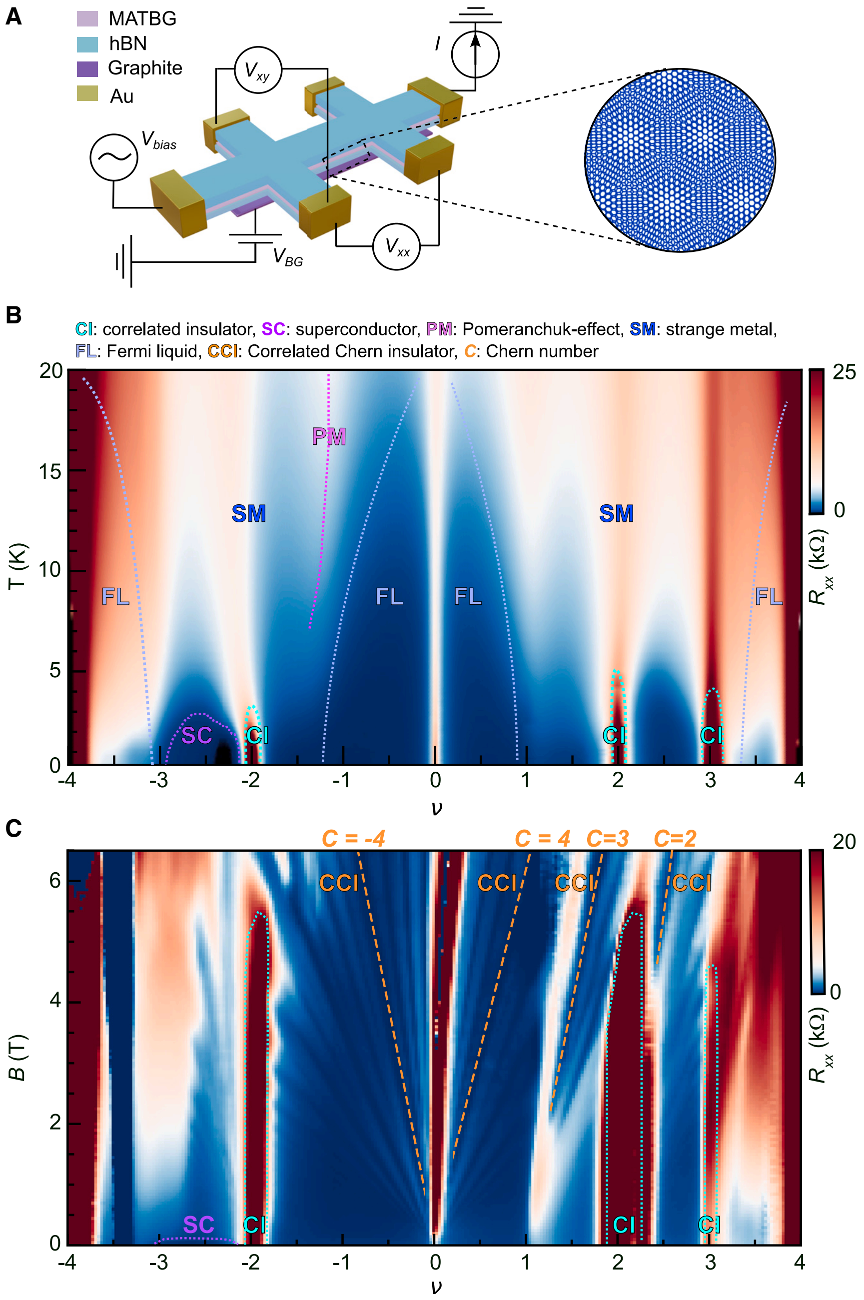

Figure 1. Typical low-temperature phase diagrams of high-quality MATBG devices

(A) Schematic of an hBN-encapsulated MATBG Hall bar with the typical measuring circuit. The zoom-in shows the moiré pattern formed by twisting the two graphene layers.

(B) R_{xx} vs. filling factor υ vs. temperature T of a $\theta = 1.16^\circ$ MATBG device displaying CI states at $\nu = \pm 2$ and superconductor at $\nu = -2 - \delta$. The dashed lines schematically mark the different correlated states, described above the figure.

(C) Landau-fan map (R_{xx} vs. υ magnetic field B) of a $\theta = 1.12^\circ$ MATBG device. The device displays Landau fans emerging from the CI states at $\nu = +1$, ± 2, and $+3$ and a superconductor (SC) dome at $\nu = -2 - \delta$. The dashed orange lines mark the correlated Chern insulators emerging at each integer filling.

the details of the fabrication protocols, showing strong inhomogeneity and irreproducibility.

The complexity of these rich and diverse phase spaces is influenced by numerous external factors. These factors include the twist angle,[20] the twist-angle disorder,[21] the dielectric environment,[22,23] the relative alignment to the encapsulating layer used, in particular hexagonal boron nitride (hBN),[6] and strain.[21,24,25] Some of these parameters, such as the selection of specific dielectric thickness ranges or controlling the alignment of graphene with the hBN, are integrated into the fabrication process. Others, like strain or angle disorder, are currently difficult to control and are highly dependent on the stacking process. Therefore, optimizing and standardizing the fabrication process of moiré materials can greatly impact the reproducibility and overall understanding of the intrinsic properties of these materials.

Here, we report a detailed fabrication protocol that was optimized for the high-yield and high-quality assembly of MATBG devices. It is based on a modified dry-transfer technique[26–28] that allows production of almost bubble-free MATBG devices and results in high twist-angle precision and high twist-angle homogeneity, showing most of the previously reported phases, such as CIs,[1–3] superconductors,[2–4] strange metals,[12,14] Chern insulators,[8–11] and the Pomeranchuk effect.[29,30]

RESULTS

Figure 1A shows the device cross-section of a typical so-fabricated MATBG Hall bar device, and Figures 1B and 1C show typical high-quality phase diagrams of the low-temperature transport measurements of the longitudinal resistance R_{xx} vs. the electron filling factor per moiré unit cell ν, as a function of temperature T for a $\theta = 1.16^\circ$ device (Figure 1B), and R_{xx} vs. ν and perpendicular magnetic field B for a $\theta = 1.12^\circ$ device (Figure 1C).

Preparation of the 2D crystals

One of the often overlooked but key steps is the careful preparation and selection of appropriate 2D crystals, from which the MATBG is eventually assembled. This determines, to a large part, the successful outcome. We find that only with properly selected and prepared 2D crystals can one achieve a high yield

Figure 2. Graphene and hBN flake selection

(A) A suitable graphene flake has a large size and is not surrounded by thicker flakes.

(B) A suitable hBN flake has a homogeneous thickness of 10–20 nm, is not surrounded by thicker flakes, and has a sharp edge for clamping.

(C) A suitable graphite gate is straight, 10 μm long, 3–4 μm wide, and around 2 nm thick.

and high homogeneity of the final stack. Further, we discuss in great detail our preparation and selection criteria.

Exfoliation

The 2D crystals, in particular the graphene and graphite flakes, are exfoliated via the scotch tape technique on Si/SiO_2 (285 nm) substrates, following the standard recipe that was developed by Huang et al.[31]: pre-cleaning the chips in O_2 plasma and heating up the substrate to ∼100°C for ∼2 min to increase the exfoliation yield. For the hBN crystals, however, we use a slightly altered recipe, where first, we prepare a second or daughter scotch tape with thinner hBN crystals, by directly peeling the original tape. Second, we do not apply heat before the peeling process, as the hBN tape is very sparsely covered with crystals, as compared to the graphene tape, and will leave too much tape glue residues on the chips (see supplemental information for more details).

For double-graphite-gated devices, the top graphite gate is exfoliated without performing O_2 plasma cleaning. This reduces the density of viable flakes, which are left on the SiO_2, but significantly improves the pick-up probability of the flake of interest, as well as the smoothness of the process, as has been previously reported.[26,32] The bottom graphite gates are produced as a by-product of graphene exfoliation and can be selected from the plasma cleaned chips.

Flake selection

After the exfoliation process, the 2D flakes are screened under an optical microscope, and all highly suitable flakes are identified and cataloged. There are several considerations for choosing the individual flakes as well as the relations between the different flakes of the stack (Figure 2). In general, the first-order criterion in identifying viable flakes is how pristine and homogeneous they are. Selected flakes should have no tape residues or step terraces and should be well isolated from nearby bulky flakes, which typically cause problems during the stacking process. Then there are certain constraints to consider for the different materials.

Graphene flakes. Graphene flakes should be at least twice as large as the desired device size. Flakes that are ∼10–15 μm × 15–30 μm are typically desired, such that the final Hall bar devices are ∼10 μm long.

hBN flakes. hBN flakes should fully encapsulate the graphene and are chosen to be 10–20 nm thick, which is considerably thinner than the typically used 30- to 70-nm-thick hBN flakes typically used in the community.[3–5] We find that the thinner hBN flake has several advantages. Thinner hBN flakes are considerably more elastic than thicker flakes, which makes the stacking process much smoother and may generally help in the strain relaxation within the hetero-structure. It also reduces the likelihood of unexpected rapid movements or jumps in the stamp during the stacking, which can give rise to sudden stress release and so enhance bubble formation[33] (an example is shown in Video 1), which we try to minimize as much as possible since these significantly contribute to angle inhomogeneity.[21] However, if the flakes are too thin (i.e., <5 nm) they are structurally weak and may tear during the stacking process. Also, unwanted tunneling or capacitive coupling to the gate electrode may affect the final device.[34] It is also easier to spot dirt, defects, folds, or wrinkles in thin hBN flakes under the optical microscope, and flakes less than 20 nm thickness are transparent enough to see through them during the stacking process, which is particularly helpful when making multilayered stacks.

The hBN flakes are generally chosen such that they are larger than the graphite gates to prevent the graphite and graphene layers from shorting in the stack. Also, the hBN that will be picked up first should have at least one sharply defined edge. As we will explain later, this edge can be used as an anchoring line for the graphene sheets in the pick-up process, which helps to stabilize and lock the crystallographic orientation of the graphene sheets in the hetero-structure.

Graphite flakes. The graphite flakes for the gate electrodes are chosen to be ∼2–4 nm thick, 3–6 μm wide, and 10–15 μm long. The width is chosen such that in the final transport devices the arms of the Hall bars, which extend beyond the width of the device, can be gated away from the charge neutrality point (CNP) using the highly doped Si substrate, which helps to minimize the contact resistance. Flakes of less than five layers are avoided due to their potentially complex properties, including magnetism in rhombohedral trilayer and pentalayer graphene[35,36] and their insufficient screening of the charge puddles in the SiO_2 substrate.[37] Thicker flakes are also avoided since they are less elastic and may induce more strain to the final stack. Since they are narrower than the twisted graphene regions, they also produce an unwanted height step and curvature in the TBG device, which is directly proportional to the graphite thickness.[38]

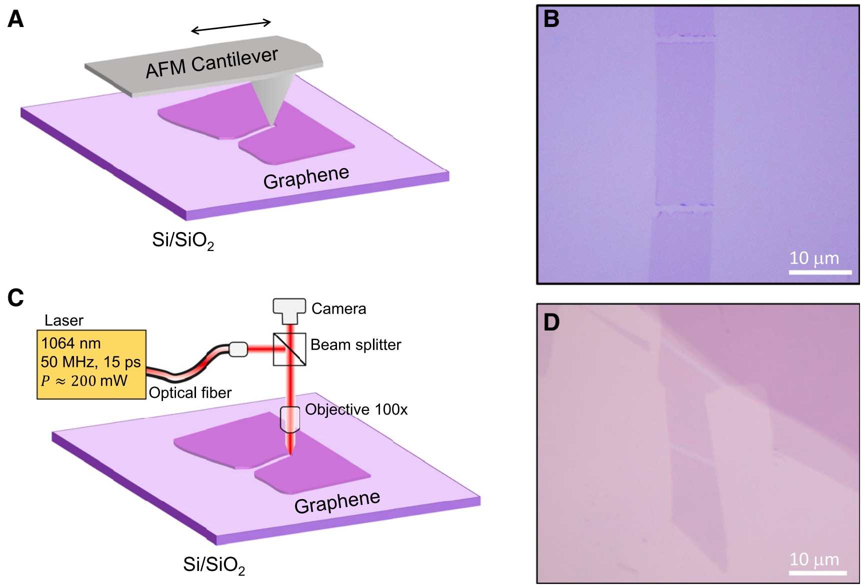

Figure 3. AFM cantilever and laser cutting

(A) Schematic of the AFM cantilever on PDMS used to cut the graphene flake.

(B) The AFM cantilever is used to cut the graphene *in situ* in the transfer stage.

(C) Schematic of the laser setup used to cut the graphene flake.

(D) Graphene flake cut with the laser.

The bottom gate needs to be longer than graphene, such that it can be easily contacted during the lithography process.

For double-gated devices, the relative sizes of the graphite gates need to be considered. To contact the back gate in the lithography process, the bottom gate should also be longer than the top gate. In contrast, the top gate should be wider than the back gate. This way, the region that is gated only by the top gate can be also gated with the Si gate. This is very important in MATBG due to the existence of highly resistive states that can completely dominate the measured signatures otherwise. These considerations are displayed in Figure S3.

Creating two graphene sheets with identical crystallographic orientations

MATBG devices are always assembled starting from a single crystal graphene sheet that is cut into two pieces. That ensures that both sheets have exactly the same initial crystallographic orientation before the rotation of the layers. The devices are fabricated using a cut-and-stack technique,[22] where the original graphene flake is cut into two pieces. This approach has a great advantage over the original tear-and-stack method,[28,39] as it does not induce a pulling and tearing motion in the graphene sheet during the pick-up process and so reduces the chance of altering the relative twist angle between the layers. We use two different techniques to cut the graphene, one with an atomic force microscopy (AFM) cantilever that is mounted on a glass slide, and the other with an ultra-strong pulsed laser beam.

The first technique is built on the typical stamping cantilevers for the stacking process: a small polydimethylsiloxane (PDMS) square is placed on a glass slide and an AFM cantilever is placed on the edge of the PDMS and secured with scotch tape (Figure 3A). To cut the graphene, the glass slide with the AFM cantilever is placed on the micromanipulator of the transfer stage and lowered toward the chip with the desired graphene flake until contact is made. The point of contact can be seen as the cantilever deflects, changing its reflectance. Once the cantilever is in contact with the SiO_2/Si chip close to the desired graphene flake, the sample stage is moved passing the cantilever over the flake, which results in a clean cut $\sim$1 μm wide (Figures 3A and 3B). Graphene is cut at room temperature to avoid sudden relaxation of the graphene flake, as at higher T it tends to fold onto itself.

In the second technique, the graphene flake is cut by using a laser.[40] We use an infrared pulsed laser (1,064 nm) with an average power of 200 mW. The laser passes through a beam splitter, which allows the user to focus it on the sample while imaging through the camera. The laser path that goes to the sample is focused using a 100× objective, which creates a beam size of $\sim$1 μm in width. By passing the laser through the desired flake, we can acquire clean cuts of also $\sim$1 μm in width (Figures 3C and 3D). While both techniques give similar results, in principle, the laser induces less mechanical stress than the AFM cantilever, reducing the chance of breaking a flake while cutting it, making the graphene-cutting process more controlled.

Cleaning of the area that surrounds the flake

The AFM cantilever can also be used to move flakes.[41,42] This is especially useful when a flake is very close to the desired flake, such that it might negatively affect the pick-up process. By precisely controlling the AFM cantilever with the micromanipulators, one can fully push out a flake from the area, as shown in Figure S4. Having a cleaner surface around the desired flakes helps to ensure a slow and controlled lamination of PC over the flakes (see Video S1), which prevents the appearance of bubbles, helps to squeeze any present bubbles out, and lowers the chance of distorting the aimed twist angle. Using the laser as described above, large graphene areas can be burned, which can be useful to isolate a flake for pickup (shown in Figure S5). However, the laser cannot be used so far to structure or remove hBN flakes due to their chemical and temperature stability.

High-yield assembly of MATBG devices using twist-angle locking

From the prior prepared catalog of available 2D crystals, we carefully select the best-fitting flakes and prepare a tentative assembly plan of the ultimate stack. This allows the user to properly choose the size, shape, and compatibility of different flakes and minimizes the possible errors arising during the stacking process.

Preparation of the stacking process

After cutting the graphene, pre-selecting all the flakes, and making a stacking plan, the stacking process may begin. For the dry-transfer process, we use a so-called stamp that is mounted on a glass slide. The stamp is a polymer heterostructure consisting of a small square of ~2 × 2 mm^2 of 1-mm-thick commercially available PDMS that is covered with a polycarbonate (PC) film. The stamp is made following the work of Zomer et al.[27] The full details of the stamp-making process are explained in the supplemental information.

The PDMS acts as a soft viscoelastic cushion in the pick-up process, and the small size (2 × 2 mm^2) is chosen such that the contact point of the PC with the SiO_2 surface, which we generally refer to as the wavefront, can be controlled easily. The decision to use PC films as the adhesive layer is motivated mainly by their high level of adhesion to the materials being used and because PC films allow the stacking process to be performed at higher T than e.g., polypropylene carbonate thin films.[43] As explained in detail later, the higher temperatures during the lamination process enhance the quality of the resulting device.

Pick-up technique

The first step in the assembly process of the 2D crystals is to locate a clean region on the PC film, which is larger than the largest 2D crystal that will be used in the entire stack. Once this is chosen, the top graphite gate is picked up. The direction from which the PC approaches the crystal in every step is important, since it marks the relative orientation between the flakes. Hence, for the pick-up of the different crystals, we always rotate the sample stage to obtain the ideal position.

The approach to pick up all the flakes is as follows: The chip with the desired flake is placed on the heated sample stage and kept in place by applying a vacuum on its back side. The stamp is lowered until contact is made with the heated SiO_2 surface. The point of contact is evident from the change in the deeper apparent color of the contact area, which is surrounded by Newton's rings (see Figures 4A–4D and 4G). In general, we set the tilt angle of the glass slide such that the PDMS/PC stamp makes its first contact with the SiO_2 in one of its corners, which allows for a better control of the wavefront. A sudden jump or fast movement of the PC film can tear, move, or induce bubbles in the heterostructure. Once the PC film has fully laminated over the flake, the stamp is pushed slightly further and then retracted slowly. When the flake is picked up, the PDMS/PC film will acquire a dark shadow in the shape of the flake, unlike the characteristic color it has on the SiO_2 surface.

Locking the twist angle of MATBG by anchoring to the hBN edges

One issue that is commonly observed in the assembly of MATBG devices is that the individual crystals are moving and rotating with respect to one another during the pick-up process. This has its roots in the lateral and vertical forces that are applied on the 2D crystals during the process, which can lead to a relative motion between the crystals that is enabled by the slippery and low-friction van der Waals (vdW) interfaces between them.[44] Especially between hBN, graphene, and graphite flakes, this motion can lead to a distortion of the target twist angles and positions of the 2D crystals in the stack. Furthermore, two graphene sheets are only energetically stable in the AB stacking configuration of $\theta = 0^\circ$ twist angle, where twisted bilayer graphene devices with $\theta \neq 0$ exist only in an energetically meta-stable state and tend to rotate back to an AB configuration. These properties of vdW interfaces significantly lower the yield of a precise setting to the desired twist angle between two graphene sheets.

To increase the yield of MATBG devices, it is therefore essential to develop a technique that hinders the free relative motion of the 2D crystals during the pick-up process and mechanically stabilizes them. For this purpose, we make use of a vdW edge-clamping technique, which allows the edges of the individual layers to interlock, hence locking the relative twist angle between them. As discussed previously, the first picked-up hBN is generally chosen to have at least one sharp edge, which will be used as an anchor, to which we clamp the edges of the two graphene flakes, which were defined in the graphene cutting process. During the pick-up process, the hBN covers the whole graphene flake except the edge that will be used for clamping (see Figure S12). Consequently, the edges between the 2D crystals fold over each other and interlock over a length of ~1 μm, which is visible as an increased roughness on the edge of the hBN/graphene interface in the optical images (see Figures 4B–4D and S11), and so restrict any further relative motion between them. This significantly increases the probability of retaining a twist angle of the TBG stack close to the magic angle.

Importantly, the clamping has to be done using a non-crystallographic axis of the graphene and/or hBN to avoid unintentional alignment between the layers, which would induce an additional moiré pattern and influence the electronic properties of the stack.[5,45] Therefore, the clamping is not done between perfectly straight edges (which point to possible crystallographic axes), but rather asymmetric edges of similar size. Using the cut edge of the first graphene is an ideal clamping point because the rippled graphene provides more roughness (as is clearly seen in Figure 4B), increasing the chances of having a successful clamping. Hence, one strategy is to cut the graphene not just in two pieces, but rather in three, giving a cut edge also for the second graphene layer, as is seen in Figures 4B–4D.

Stacking process

A complete stacking process is shown in Figure 4, where we follow all the steps of the fabrication of a double-gated MATBG device. The same stacking procedure can be, however, extended to the fabrication of twisted graphene multilayers, and TMD bilayers. The entire pick-up process is done by fixing the stage temperature to $T \sim 100^\circ\text{C}–120^\circ\text{C}$. The lamination on the flakes is done at constant T, and the approaching of the crystals is done entirely by hand using the z-micromanipulator on the transfer stage (see supplemental information for a full description of the transfer stage). We do not approach the crystals by ramping up the temperature of the stage, as is used by other recipes elsewhere.[27] After the graphite top gate and the top hBN layer are picked up with the above recipe, we can now continue and pick up the two graphene layers.

When picking up the graphene, the chip is arranged such that the cut in the graphene is matched with the sharp edge of the top hBN (Figure 4B), and the wavefront is parallel to the cut. This facilitates full lamination over the first graphene flake while avoiding any contact between the PC or the hBN with the second graphene flake. The wavefront is approached very slowly to avoid any unintended movement of the graphene, as any movement of either the top or bottom graphene sheet can cause a distortion in the twist angle. Once the hBN is in contact with the graphene,

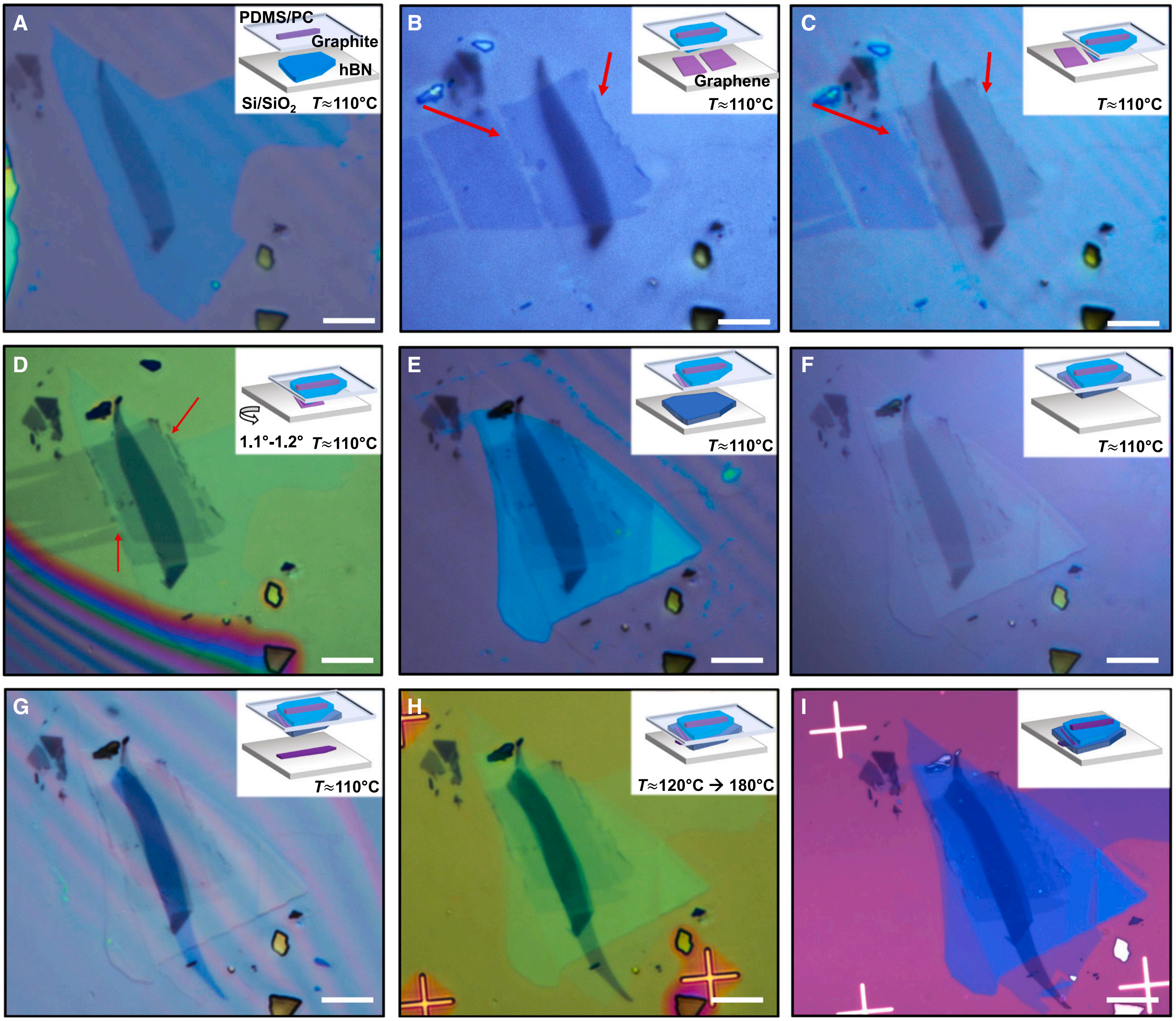

Figure 4. Stacking process

(A) Picking up the top hBN, while the top graphite is already picked up.

(B) Aligning the top hBN with the first graphene flake. The arrows signal the part of the graphene that will clamp over the hBN.

(C) First graphene is picked up. The change of color signals that the pick-up was successful. The red arrow points to the edges having clamped over the hBN.

(D) The stamp is laminated over the second graphene after rotating the stage 1.1°. Red arrows point to the places where the second graphene will clamp over the first graphene.

(E) Both graphene layers are now picked up.

(F) Picking up the bottom hBN.

(G) Aligning the stack over the bottom graphite gate.

(H) The stack is dropped on a pre-patterned chip with markers.

(I) Clean stack after removing the PC. The final stack has an angle of 1.06° ± 0.02°.

Scale bar, 20 μm.

the wavefront is further moved until the entire first graphene sheet is covered with hBN, while ensuring that the PC does not touch the second graphene. As soon as the first graphene sheet is in full contact, the stamp is slowly retrieved and moved a few mm above the Si chip. During this pick-up step, the graphene flake is clamped with the top hBN layer.

Now the second graphene sheet is picked up. While the stamp and the top half of the stack are hovering over the chip, the sample stage is rotated by 1.1°–1.2° to a slightly higher angle than the target twist angle, to account for an often observed slight twist-angle relaxation of ~0.1° during the pick-up process. After rotating, the second layer of graphene is overlapped with the first graphene layer, and the pick-up procedure is repeated in the same fashion as described above for the first layer of graphene. The second graphene layer is also clamped to the hBN edge, in exactly the same way as the first layer. After picking up both graphene layers, the bottom hBN is picked up. The flake is approached in such a way that it fully encapsulates the graphene and that it will fully cover the bottom graphite gate.

Finally, the bottom gate is picked up. The bottom graphite gate should be entirely covered by hBN. If not entirely covered, it may have different adhesive behaviors between the hBN-covered region and the region in direct contact with the polymer, consequently inducing tension or strain during the pick-up process. This tension can be so violent that it can sometimes even displace the position of the graphite gate, destroying the whole stack. We often have observed that this type of tension has affected the twisted bilayer graphene region and has enabled the relaxation of its twist angle. In double-gated devices, this pick-up step is even more crucial since both of the gates need to be perfectly aligned to have a working device.

Dropping the stack

Finally, the complete stack is dropped on an SiO_2/Si chip with preformed alignment markers to facilitate the subsequent nanofabrication process. Before the drop, the chips are cleaned with O_2 plasma to improve the adhesion of the 2D layers. The contact between the PC film and the chip is now made at $T \sim 120^\circ C$–$150^\circ C$ to enhance bubble mobility one more time.[32] The wavefront is moved very slowly over the stack to push away all the remaining bubbles. Once the full stack is in contact with the SiO_2, the wave front is moved ~200 μm further from the stack. Now the stage temperature T is raised slowly up to 180°C. As the T approaches the glass transition temperature, T_g, of the PC of $\sim 147^\circ C$,[43] the PC detaches from the PDMS film, and at a T far beyond the glass transition ~180°C, the PC completely melts. For our PC/PDMS stamps and transfer setup, the detaching happens at a slightly lower T, typically at a setpoint of ~130°C. At this point the z-micromanipulator is moved up slightly to detach the entire PC film from the PDMS. During this process ($130^\circ C < T < 180^\circ C$), we make sure that the PDMS is not in contact with the PC film, and we move it slightly up every time it contacts it. Once T reaches ~180°C, the stamp is fully retracted. At this point, the areas of the PC film that are in contact with the chip are fully molten and detach from the remaining PC areas on the glass slide. A full example of the procedure is shown in Video S2.

The T ranges in this step are very important. Retracting too far at low T can break the stack, while if T is raised without detaching the PC from the PDMS, the thermal expansion of the latter can put pressure on the stack and thus relax the twist angle. During the entire process, the X–Y micromanipulator of the stamp and the sample stage should not be moved, since this will tear the stack. Once the stack is dropped, the T of the stage is lowered to room temperature. The stacking process is now finished. The final step before the lithography is to clean the PC. The chip is dipped in chloroform for 2 min, followed by dipping in acetone for 1 min, isopropanol for 1 min, and blow drying with N_2.

Etching and contacting

After the preparation of the stacks, these are fabricated into a Hall bar geometry (as schematically shown in Figure 1A) via nanolithography techniques, namely, e-beam lithography, reactive ion etching and evaporation. The heterostructures are etched using CHF_3/O_2 plasma and the 1D contacts are made using 5 nm Cr/50 nm Au following the recipe of Wang et al.[26]

Strategies to enhance twist-angle homogeneity by reducing bubble formation

To achieve the cleanest 2D interfaces and greatest twist-angle homogeneity possible, we aim to avoid bubbles from forming during the stacking process as much as possible, as has been explained above. Bubbles significantly contribute to angle inhomogeneity and can even lead to the absence of the magic-angle condition in an area up to ~0.5 μm around the bubble[21] and can induce quite strong strain field in the device. Typically, bubbles form during the stacking process mainly because of the accumulation of dirt on the surfaces of the different 2D materials[32,46] or due to fast wave-front approaches, which can trap air along the interface.[47] The overarching theme is to maintain a stacking process that is as smooth as possible, which involves full control of the stamp's wavefront. Here we summarize the main strategies we use to reduce bubble formation.

Using clean stamps and flakes

We make sure we use an area of the stamp that is clean and larger than the largest flake to be used. If the stacking process is done in an area of the PC film that already has some dust particles, bubbles, and so on, this could hinder the pick-up process and introduce bubbles into the whole stack. In the same manner, we only use flakes that have clean interfaces, as any dirt or defect present on the flakes will induce bubbles.

Using thin hBN flakes

We use thin hBN (10–20 nm), which is considerably more elastic than thicker flakes, and makes the stacking process much smoother and may generally help in the strain relaxation within the hetero-structure. It also helps in avoiding unexpected rapid movements or jumps in the stamp during the stacking, which can give rise to sudden stress release and so enhance bubble formation[33] (an example is shown in Video S1).

Cleaning surrounding areas

We clean the area surrounding the desired flake (see supplemental information). If there are large flakes or dirt close to the flake to be picked up, this modifies the wavefront and can easily lead to jumps in the stacking process.

High-temperature co-lamination process

The entire stacking process is done at high T , ~100°C–120°C, as this serves to improve the self-cleaning properties of the vdW interfaces during the stacking process and to enhance bubble mobility in all the pick-up steps.[32,43] This enables us to use every step to remove bubbles that might have formed in the previous pick-up steps. To highlight the bubble cleaning during different steps, we show the bubble removal in a single graphite gated device in Figure 5. In the image, we observe a stack that has many bubbles before the gate pickup, and during the pickup the bubbles rearrange, leaving the graphite region clean with fewer, larger bubbles being formed on the edge of the graphene.

Characterization of the devices

To understand the device homogeneity of our fabrication protocol, we have analyzed 34 so fabricated and finalized devices. First, we studied their bubble density by optical microscopy,

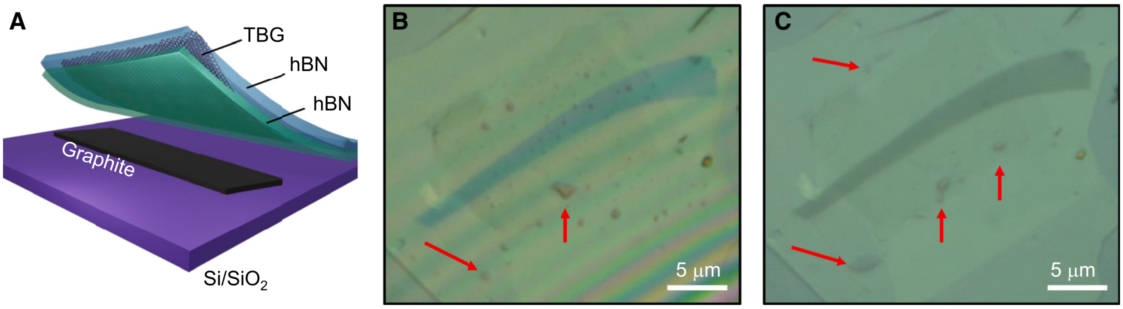

Figure 5. Bubble removal during the pick-up process

(A) Schematic showing the stacking process during the back gate pick-up step.

(B) Before picking up the back gate, there are several bubbles visible inside the graphite gate area, which will be the device region.

(C) After picking up the back gate the bubbles are efficiently moved out of the device area and they accumulate at the edges of the graphene. The final device had a twist angle of 1.1° ± 0.02°. Red arrows indicate the position of the bubbles.

AFM, and in a few devices, by scanning transmission electron microscopy (STEM).

Optical microscopy

By looking at 100× optical images, we can count the amount of bubbles present in the stacks. We have compared some of the images to AFM scans of the same stack and found that with the right microscope settings we observe the same bubbles as in the AFM images (see Figure S13). We characterize the cleanliness of the stacks by extracting three main quantities: largest area with no bubbles, number of bubbles larger than 1 μm^2 (microbubbles), and number of bubbles smaller than 1 μm^2 (nanobubbles). The final area that we select for a device is always centered around the graphite gate, which is the region of interest to create a device. We have found that we obtain on average less than one microbubble and fewer than three nanobubbles per 10 × 5 μm^2, with several devices having no bubbles at all in that region and some devices reaching bubble-free areas larger than 200 μm^2 (see Figure S14). Considering that the final devices are Hall bars with dimensions ranging 8–15 μm × 2–4 μm, this procedure allows us to make the final devices in an entirely bubble-free region of the stack.

STEM

The bubble density found by optical microscopy is further confirmed by STEM. In Figure 6, we show several STEM images taken along the longitudinal cross-section of a device. By combining the STEM images with an electron energy loss spectroscopy (EELS) composition mapping, we can clearly see the different layers conforming the stack, like the hBN, graphite, and MATBG sheets. For one of the devices, we find no bubbles across the length of the entire device of ~12 μm, while for the other device (shown in Figure S15), we observe most of the device to be bubble free over a length of ~15 μm, but in some remote regions still find a few bubbles of ~50 nm in size.

Room temperature transport characterization

To select the most promising devices for further studies, we perform four-terminal resistance (R_{xx}) measurements as a function of back gate voltage V_g at room temperature. Due to the strong dependence of the TBG band structure on the twist angle, the characteristic gate sweeps of R_{xx} vs. V_g allow to distinguish between devices with a twist angle close to the magic angle, from devices with a lower ($\theta \lesssim 0.7°$), higher ($\theta \gtrsim 1.6°$), and completely relaxed twist angle of ($\theta \approx 0°$). At the magic-angle condition, the bands at the Fermi energy are highly non-dispersive (flat bands) and are separated by the dispersive bands by a gap of ~40 meV. As the angle increases, the bands at the Fermi level become more dispersive, while the band gaps move to higher energies.[4,48] In contrast, for low twist angles, several flat bands appear at low energies with small band gaps between them.[49–51]

The room temperature measurements can clearly resolve these signatures, which distinguish between devices, by two main features: the shape of the R_{xx} vs. V_g dependence and the nominal value of the R_{xx} (shown in Figure 7). While devices with $\theta \approx 0°$ have a very sharp CNP, a similar but broadened behavior is observed for TBG with $\theta \lesssim 0.7°$ due to the presence of multiple bands close to the Fermi level. As the angle gets larger ($\theta \gtrsim 1.6°$), the band gap to the dispersive bands move to higher energies, leading to a characteristic double-humped curve (see Figure S16 for an example). Devices with θ close to the magic angle have a much broader, dome-shaped, R_{xx} vs. V_g dependence and a characteristically high $R_{xx} \gtrsim 10\ k\Omega$.

One can attribute this behavior to the simultaneous conduction through a flat band and two temperature activated dispersive bands. However, we also find that devices with an intermediate large/small twist angle ($1.3° \lesssim \theta \lesssim 1.6°$ and $0.7° \lesssim \theta \lesssim 0.9°$) are nearly indistinguishable from magic-angle devices at room temperature.

Low-temperature transport characterization

The devices are then cooled down, where typically below a $T < 100$ K the R_{xx} vs. ν curves start to alter significantly from its high temperature shape, and below a $T < 10$ K the R_{xx} vs. ν curves are dominated by the formation of the insulating and superconducting states, as can be seen in Figure 7B. These states are further characterized at low temperatures, typically at a base temperature of $T = 35$ mK, as has been shown in Figures 1B and 1C.

While it unfortunately is not possible to directly image the moiré pattern in a fully encapsulated and top-gated device, it is, however, possible to infer the twist angle from the magneto-transport R_{xx} vs. B and ν phase diagram as previously described[1,2] (see the methods section for details). By measuring the carrier concentration n in the device, through Hall and

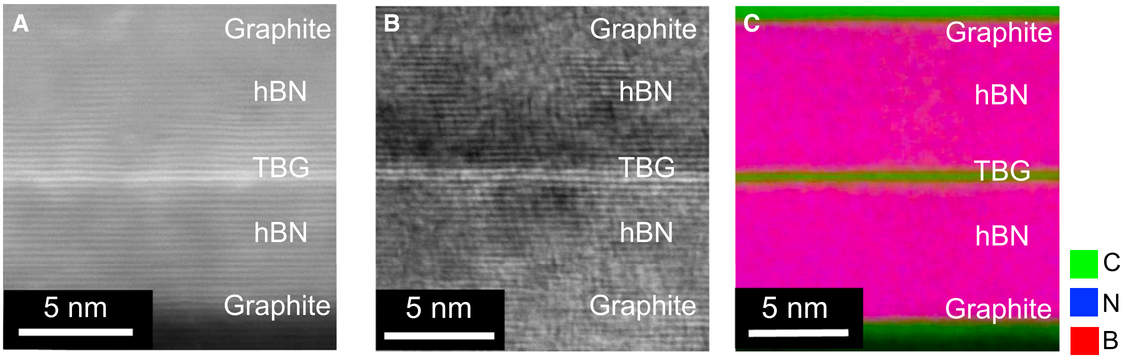

Figure 6. Cross-sectional STEM and EELS imaging of remote device regions

(A and B) STEM cross-sectional images of the device, taken in different regions of the device. The lattice fringes of the double-layer graphene sandwiched between the hBN layers, as well the graphite electrodes, are clearly visible in the STEM images.

(C) STEM-EELS mapping of the device cross section showing the graphite, hBN and double-layer graphene stacking in the device. In most of the device areas, the graphene/graphene and graphene/hBN, as well as hBN/graphite, interfaces are homogeneous and clean at the atomic scale.

Shubnikov-de Haas experiments, it is possible to extract the size of the moiré unit cell, the corresponding filling factor ν, and so assign the average twist angle θ between the used contact pairs in the measurement. We then can perform two terminal conductance measurements between all the different contact pairs and use the carrier concentration at which the CIs at $\nu = 2$ occur to estimate the average twist angle between all the different regions in the device, as is shown in Figure 8.

Device yield and twist-angle homogeneity

Finally, we summarize the main results that we can extract from 34 devices fabricated with the provided protocol, mainly the success rate or yield of the MATBG devices that have a twist angle close to the magic angle of $\theta = 1.1^\circ$, and their twist-angle homogeneity, $\Delta\theta$. For the twist-angle homogeneity, we typically measure the two-probe terminal conductance between all the contact pairs (generally separated by 1.5–2 μm) and extract the twist angle θ using the carrier density n at which the CI state at $\upsilon = 2$ nucleates, which is marked by a sharp dip in the conductance G. We have then estimated the number of contact pairs with a variability of twist angle $\Delta\theta \leq 0.02^\circ$, which is the typical error bar of the angle extraction process as explained in the methods section.

MATBG device yield

To extract the MATBG device yield, we have considered only samples that were made after the establishing of this fabrication protocol, that were fabricated by three fully trained and experienced PhD students (the first three authors in this paper) from 2020 to 2023. This accounted for a total of ~56 attempted stacks, of which 34 were fully fabricated and measured. Out of the 34 finalized devices, 13 (38%) had at least one region between two contact pairs with a twist angle of $\theta = 1.1 \pm 0.1^\circ$, out of which 8 devices (62%) showed superconductivity and 11 devices (85%) showed a CI state at a filling either $\upsilon = +2$ or $\upsilon = -2$. Another five devices showed a twist angle between $\theta = 1.1 \pm 0.2^\circ$, totaling a device yield of 53% for this range of twist angles. Devices that failed at an earlier stage of the fabrication process (~40%) were not counted for the yield calculation.

Twist-angle homogeneity

By extracting the twist angles between all of the different contact pairs in the devices, we typically find regions of ~6 μm^2 that show almost no twist-angle variation, of only $\Delta\theta \leq 0.02^\circ$, with some devices reaching homogeneous areas of up to 36 μm^2, as is highlighted for a best-case device shown in Figure 8. As also seen from the twist-angle distribution in this device, we also observe sudden jumps in the twist angles of neighboring contact pairs, likely introduced by some fault lines between the two graphene sheets.

It is important to note that the twist angle extracted in transport measurements is a global twist angle determined by the average carrier density ($\overline{n_e} \approx C_g V_g / e$) on the micrometer scale. While we observe a homogeneous global twist angle, it is likely that in the nanometer scale (few moiré unit cells), there are areas with different twist angles $\theta(\boldsymbol{r})$, which translate into a local carrier density distribution $n(\boldsymbol{r})$.[21,52] While these local twist-angle/carrier density inhomogeneities do not affect the global twist-angle extraction done by the average carrier density of the correlated and band insulating states (see methods), they can affect the more fragile states such as superconductivity or magnetism.[53]

DISCUSSION

While the field of MATBG specifically and that of moiré materials more generally offers immense new opportunities to uncover exotic quantum phases,[54,55] the device fabrication remains tedious and prone to strong twist-angle disorder. The fabrication of homogeneous and highly reproducible devices remains a big challenge and the main limiting factor of the advancement of the field. Although efforts are being made toward improving the reliability in the fabrication, for example, by the automatization of the stacking process[56,57] or developing assembly processes in high vacuum for improving cleanliness,[58] a deeper understanding of the subtleties of the stacking process is needed to progress further in that direction. The detailed fabrication process for MATBG devices presented here allows further standardization of the assembly of moiré materials by using an almost bubble-free assembly protocol and a twist-angle clamping technique

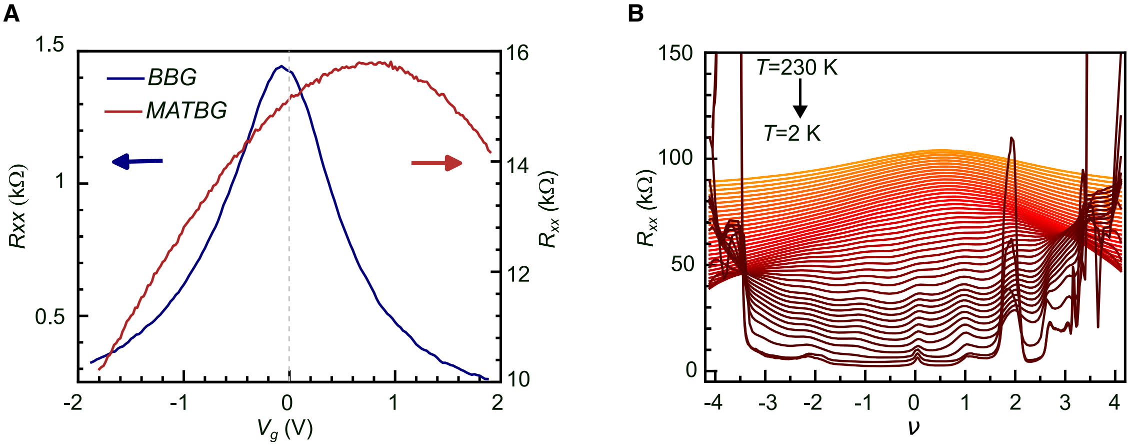

Figure 7. Identifying MATBG devices at room temperature

(A) Room temperature measurement comparing a Bernal bilayer graphene (BBG) and a MATBG device with twist angle $\theta = 1.06 \pm 0.02^\circ$, shown in the blue and red curves, respectively. The asymmetry of the dome, combined with the four-terminal resistance (R_{xx}) value allows to distinguish between the two. hBN of comparable thicknesses ($d \approx 15$ nm) are used in both devices.

(B) Cooldown curves of the MATBG shown in a from 230 K down to 2 K. The curves are shifted by 1 kΩ starting from the lowest T for clarity.

that allows us to obtain large homogeneous device regions with the desired twist angle and with a high probability. The very controlled lamination process, aided by the use of thin hBN, may also contribute to reduction of the accumulated strain within the heterostructure. We are certain that this protocol can be used for all other moiré materials and will increase their device yield and twist-angle homogeneity.

METHODS

Transport measurements

The room temperature transport measurements were carried out in a homemade measurement setup where the sample is placed under a vacuum $\sim 10^{-3}$ bar. Standard low-frequency lock-in techniques (Stanford Research SR860 amplifiers) were used to measure R_{xx} with an excitation current of 10 nA at a frequency of 13.11 Hz. Keithley 2400 source-meters were used to control the gates. The low T measurements were performed in a dilution refrigerator (Bluefors SD250) with a base temperature of 35 mK.

Twist-angle extraction

The twist angle θ is extracted by applying the relation $n_s = 8\theta^2/\sqrt{3}a^2$, where n_s is the superlattice carrier density and a = 0.246 nm is the graphene lattice constant. To accurately extract n_s, magnetotransport measurements, like the Landau-fan map (R_{xx} vs. V_g magnetic field B) shown in Figure 1C, are used. First, the carrier density $n = C_g V_g / e$, is calibrated by extracting the capacitance C_g from fitting the Landau levels arising from the CNP. Alternatively, the capacitance can be extracted using Hall measurements at low field. Near the CNP, the Hall carrier density $n_H = -B/eR_{xy}$ should closely follow the gate-induced carrier density $n_H = n$. Finally, the superlattice carrier density n_s is extracted from the origin of the Landau levels emerging from the band insulators or from the CI at one-half filling ($n_{\nu=2}$), such that $n_s = 2n_{\nu=2}$. Since the twist-angle extraction relies on the accuracy of the position of n_s, the calculated twist angles always have an error of $\sim 0.02^\circ$.

STEM imaging

The STEM imaging and EELS measurements were performed using a JEOL monochromated ARM200F transmission electron microscope operated at 80 kV. The microscope is equipped with a Schottky field emission gun, a double-Wien monochromator, a CEOS ASCOR probe Cs corrector, a CEOS CETCOR image Cs corrector, and a Gatan image filter Continuum for EELS, as well as ADF and bright-field detectors for STEM imaging.

All other details regarding the experimental procedures can be found in the supplemental information.

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Dmitri K. Efetov, dmitri.efetov@lmu.de.

Materials availability

No new materials or reagents were created in this study.

Data and code availability

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

ACKNOWLEDGMENTS

D.K.E. acknowledges funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation program (grant agreement no. 852927), the German Research Foundation (DFG) under the priority program SPP2244 (project no. 535146365), the EU EIC Pathfinder Grant "FLATS" (grant agreement no. 101099139), and the Keele Foundation. J.D.-M. acknowledges support from the INPhINIT 'la Caixa' Foundation (ID 100010434) fellowship program (LCF/BQ/DI19/11730021). I.D. acknowledges funding from the German Research Foundation (DFG) under Germany's

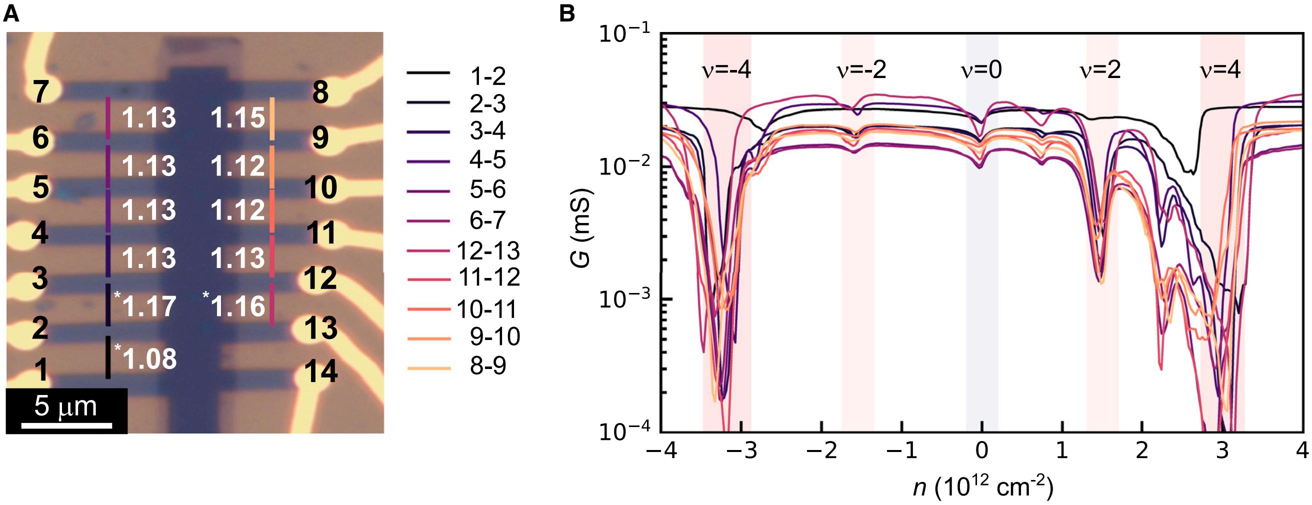

Figure 8. Low-temperature transport extraction of the twist angles

(A) Optical image of a MATBG device with twist-angle homogeneity over a range of 36 μm^2.

(B) Two probe terminal conductance G vs. carrier density n measurement at T = 35 mK for the different contacts in the device shown in a. The shading indicates different filling factors ν.

Excellence Strategy – EXC2111-390814868. K.W. and T.T. acknowledge support from the Elemental Strategy Initiative conducted by the MEXT, Japan (grant number JPMXP0112101001) and JSPS KAKENHI (grant numbers 19H05790, 20H00354 and 21H05233). L.Z. and E.O. acknowledge financial support from the Knut and Alice Wallenberg Foundation (2019.0140). The authors acknowledge financial support from the Swedish Research Council (VR) and Swedish Foundation for Strategic Research (SSF) for access to ARTEMI, the Swedish National Infrastructure in Advanced Electron Microscopy (2021-00171 and RIF21-0026).

AUTHOR CONTRIBUTIONS

J.D.-M., I.D., G.D.B., and A.D.-C. fabricated the devices and performed the measurements. J.D.-M., I.D., G.D.B., A.D.-C., M.L., and D.K.E. analyzed the data and established the fabrication protocol. L.Z. performed the STEM experiments. T.T. and K.W. contributed materials. E.O. and D.K.E. supported the experiments. J.D.-M., I.D., G.D.B., M.L. L.Z., E.O., and D.K.E. wrote the paper.

DECLARATION OF INTERESTS

The authors declare no competing interests.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.newton.2024.100007.

Received: May 18, 2024
Revised: October 4, 2024
Accepted: December 19, 2024
Published: January 14, 2025

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