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ABSTRACT

Minimizing the range of the applied gate bias in field-effect transistors is essential for reducing power consumption in modern electronics. In this study, we successfully realized a low-bias operating graphene p–n junction on a polyethylene terephthalate substrate by combining two distinct high-density electrostatic gating methods—ionic-liquid gating and high-κ solid-state gating—in a dual-gate configuration, requiring gate voltages as low as 2 V in both cases. This dual gating is fully reversible and stable, with no electrochemical reactions associated with the ionic liquids. The highly efficient solid-state gating is achieved using a thin high-κ aluminum oxide layer that naturally forms at the aluminum/graphene interface due to their weak bonding. Our device architecture offers an ideal platform for developing high-performance, energy-efficient 2D material-based transistors that operate at low voltages on flexible and transparent substrates.

The field effect is a powerful technique for investigating the electronic properties of materials in condensed matter physics.[1] In practice, an electric field is established across the material by applying an external voltage between the metallic gate electrode and the material, which is typically separated by a thin dielectric layer in a parallel-plate capacitor configuration. By electrostatically adjusting the gate voltage, the charge density (and thus the Fermi energy) of the gated material can be continuously tuned. Compared to other methods of altering the carrier concentration, such as chemical adsorption, the field effect minimizes potential physical modifications to the material and enables reversible modulation of the doping level, thereby facilitating systematic studies of properties associated with the electronic structures near the Fermi energy. However, the electric field influences only the surface of the material due to electrostatic screening by accumulated surface charges. Consequently, the unperturbed bulk portion of the material may dominate the measured transport results, potentially obscuring field-effect-induced phenomena. From this perspective, two-dimensional (2D) materials are ideal candidates for applying the field-effect method because their atomically thin nature is comparable to the electric screening length, allowing uniform modulation of charge density throughout the entire material.

The performance of the field effect in a transistor device is determined by the rate at which the electrical conductivity of the transistor channel changes in response to variations in gate voltage. In metallic materials, where the geometric capacitance dominates total capacitance—due to a sufficiently large electronic density of states rendering the contribution of quantum capacitance negligible—a thinner dielectric with a higher dielectric constant (κ) is beneficial for attaining high geometric capacitance. Regarding the transistor channel, the gated material must exhibit high mobility to ensure superior gate performance. Graphene, known for its exceptional mobility among 2D materials, serves as an ideal transistor channel, enabling the development of low-voltage operating devices with enhanced gate performance.[2]

In this paper, we successfully demonstrate high-performance graphene p–n junction devices on a plastic substrate, which operate at gate voltages as low as 2 V. To maximize gate performance in a dual-gate configuration, we combine ionic-liquid (IL) gating and high-κ solid-state gating. Specifically, the efficiency of the solid-state gating is enhanced by the naturally formed aluminum oxide at the aluminum/graphene interface, which acts as a thin, high-κ dielectric. Our results show that this device architecture is highly suitable for fabricating stable 2D material-based transistors operating at low voltages on flexible and transparent substrates.

Large-area graphene, synthesized on a copper foil via the CVD method, was transferred onto a 150-μm-thick polyethylene terephthalate (PET) film using the conventional PMMA-mediated wet transfer technique.[3,4] Metal electrodes (10 nm Ti/100 nm Au) were defined on the film through photolithography and thin-film deposition, followed by shaping the graphene channel into a Hall bar structure using oxygen plasma etching. A 50-nm-thick aluminum film serving as a local gate was then defined using the same microfabrication process and left in air to oxidize its surface and its interface with graphene fully. Finally, an 80-nm-thick epoxy-based photoresist (SU-8) was coated as a passivation layer, leaving only the transistor channel and gate electrodes exposed to the IL gating.

The as-fabricated devices were annealed at 65 °C under a nitrogen flow for several hours to eliminate chemical impurities resulting from the copper etchant and lithography process.[5] Subsequently, a commonly used IL, N,N-diethyl-N-(2-methoxyethyl)-N-methylammonium bis(trifluoromethylsulfonyl)imide (DEME-TFSI), was applied to the devices by drop-casting, and the devices were promptly loaded into a vacuum chamber to prevent moisture from compromising the chemical stability of the IL-gated material.[6,7]

Transport measurements were performed under vacuum conditions (~10^{-6} mbar). Electrical properties, including transverse and longitudinal resistances in the Hall bar configuration, were measured using a conventional low-frequency lock-in technique. The thermovoltage was measured using both steady-state DC and low-frequency AC methods to obtain consistent results.[8] All measurements were performed at room temperature under vacuum.

ILs are composed of electronically insulating yet ionically conductive compounds, resulting in most of the applied gate voltage dropping at the gate/IL and IL/graphene interfaces, where extremely thin electric double layers, typically ~1 nm thick or less, form.[7,9] This gating configuration yields exceptionally high geometrical capacitance, enabling the accumulation of charge densities (exceeding 10^{13} cm^{-2}), compared to those induced by conventional SiO_2 (<5 × 10^{12} cm^{-2}). Consequently, recent studies employing IL gating on 2D materials have revealed intiguing physical phenomena such as gate-induced superconductivity,[10–22] quenching of the bandgap,[23,24] and quantitative estimation of semiconducting bandgaps.[25–32] Another advantage of IL gating is its compatibility with non-uniform flexible substrates, which makes it well suited for field-effect devices fabricated on PET films.[33,34]

Figure 1(a) shows the schematic of an IL-gated device on a PET substrate. In the actual device, the area of the gate electrode is intentionally designed to be much larger than that of the transistor channel so that ~70% of the applied voltage drops at the liquid/graphene interface. To eliminate parasitic capacitive coupling effects that occur when the electrodes are in contact with the IL during gating, a passivation layer was used to selectively expose the graphene channel and gate electrodes to the IL.

To verify the overall quality of the IL-gated devices, we fabricated a standard Hall bar structure with relatively large dimensions of 50 × 180 μm^2 [Fig. 1(b)]. Figure 1(c) shows the gate dependence

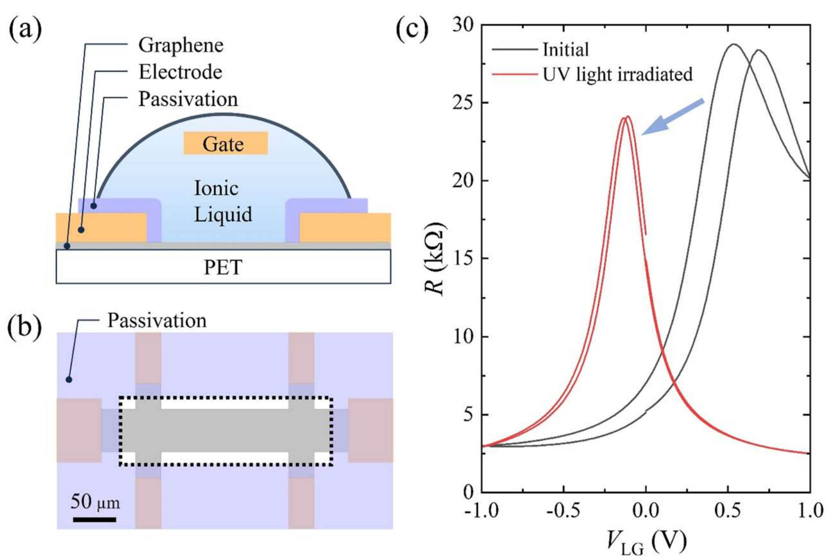

FIG. 1. (a) Cross-sectional schematic of an ionic-liquid-gated device fabricated on a PET substrate (not to scale). In the actual device, the gate electrode is positioned on the PET substrate beside the active area, rather than directly above the graphene channel. A passivation layer is used to selectively expose the graphene channel and gate electrodes to the ionic liquid, thereby eliminating parasitic capacitive coupling effects from other electrodes. (b) In-plane design of the actual device, prepared in standard Hall-bar geometry. The rectangular area enclosed by the dotted line indicates the region in contact with the ionic liquid. (c) Gate voltage (V_{LG}) dependence of longitudinal resistance (R) measured in a four-terminal configuration. After overnight UV irradiation, the charge neutrality point shifts close to zero, and hysteresis is reduced significantly, resulting in a field-effect mobility of 1300 cm^2 V^{-1} s^{-1}.

of the longitudinal resistance measured in a four-terminal configuration with a source–drain current bias of 100 nA (at ~20 Hz). Initially, the graphene was highly p-doped, with a hole doping level greater than 3.8×10^{12} cm^{-2} (black curve). However, upon ultraviolet (UV) light irradiation, the charge neutrality point (CNP), where the resistance peak occurs, shifted toward zero with reduced hysteresis (red curve). This desorption of p-type adsorbates is attributed to UV-induced perturbation of the self-organized TFSI anions (p-dopants) attached to the graphene surface.[35] In addition, degassing of the IL due to heating by UV light may also contribute, as the temperature of the PET substrate increased up to 65 °C during UV illumination. We applied the gate bias (V_G) up to ±1 V, achieving continuous charge density tuning of $\pm 7.5 \times 10^{12}$ cm^{-2}, as confirmed by Hall effect measurements. This corresponds to a capacitance per unit area of 1.2 μFcm^{-2}, which is two orders of magnitude higher than that of a typical 300 nm-thick SiO_2 layer (≈11 nFcm^{-2}). Based on the relationship between gate voltage and charge density, and the slope of the gate dependence curve, the field-effect mobility of the device is estimated to be 1300 cm^2 V^{-1}s^{-1}. It is noteworthy that the gating behavior is fully reversible, and the leakage current remained negligibly small (less than ±1 nA) by slowly sweeping the gate voltage at 5 mV/s. Such reliable behavior is essential for ensuring device stability without electrochemical reactions during the IL gating.

Using IL gating, we extended this approach to create a p–n junction structure. This was accomplished by directly depositing aluminum as a local gate on one side of the graphene channel. Owing to the weak bonding between aluminum and graphene, an aluminum oxide layer forms in air, which can directly serve as a gate dielectric.[34,36–39] The naturally formed aluminum oxide at the interface is very thin (thickness is estimated to be ≈5 nm) and has a high-κ, allowing high geometrical capacitance. In addition, this approach simplifies the fabrication process as it eliminates an additional fabrication step for preparing a separate dielectric layer. The high-κ environments provided by both the IL and aluminum oxide may also reduce scattering from charged impurities on the graphene, thereby enhancing device quality.[40,41]

A schematic cross-section of the p–n junction device is shown in Fig. 2(a). Compared with Fig. 1(a), the aluminum metal used for the local gate was deposited on the right side of the graphene channel, where its surface and interface were oxidized (indicated by the red border) in air to act as a solid-state gate dielectric. Figures 2(b) and 2(c) depict the actual device design and the corresponding optical microscope image, respectively. The graphene channel is divided

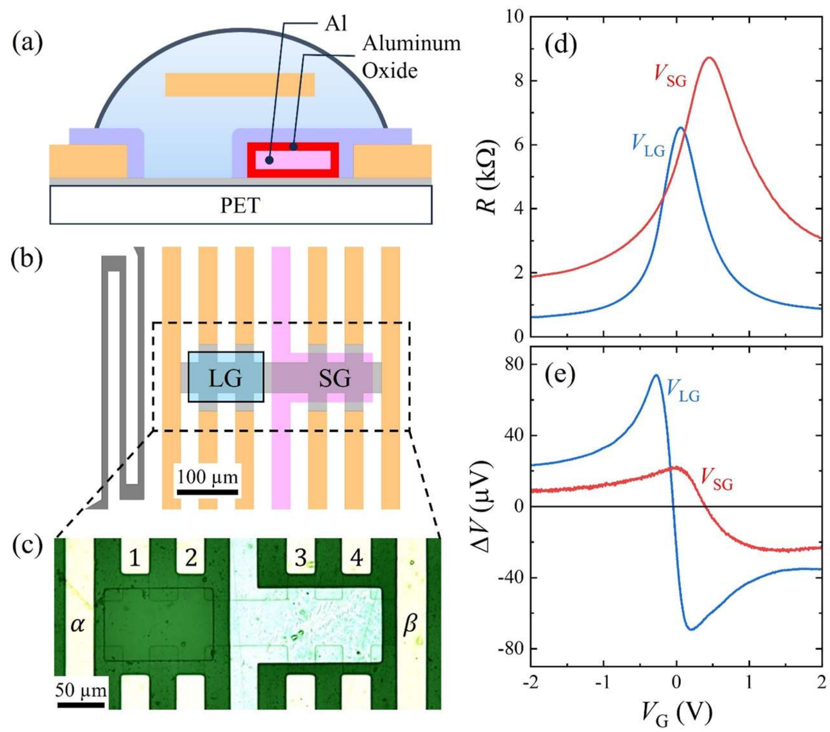

FIG. 2. (a) Cross-sectional schematic of a graphene p–n junction device (not to scale). Aluminum (Al, shown in pink) is deposited on the right side of the graphene channel, with the naturally formed aluminum oxide layer on the surface and at the interface with graphene (indicated by a red border). This thin, high-κ aluminum oxide layer acts as a gate dielectric, allowing for high geometrical capacitance. (b) Actual design of the p–n junction device. Two separate regions in the channel are controlled independently by ionic-liquid (LG) and solid-state aluminum oxide (SG) gates. A metal line (dark gray on the left) serves as a resistive heater for thermovoltage measurements. (c) Optical microscope image of the as-fabricated device corresponding to the area outlined by a dashed line in (b). The gate voltage dependence of (d) resistance (R) and (e) thermovoltage (ΔV) measured in each region using the two distinct high-density gating methods—ionic-liquid (V_{LG}) and high-κ solid-state gating (V_{SG}). In both cases, clear resistance peaks and thermovoltage sign reversals are observed precisely at the charge neutrality points.

into two regions based on the gating method: the IL-gated region on the left and the high-κ solid-state gated region on the right [labeled as LG and SG in Fig. 2(b)]. The resistive heater on the left side (dark gray line) [Fig. 2(b)] was used to generate a temperature gradient along the transistor channel for thermovoltage measurements. In our dual-gate device scheme, the passivation layer plays a crucial role in eliminating any direct electrostatic coupling between the two gates and in preventing possible chemical reactions between the aluminum oxide and IL.

Figure 2(d) shows the gate dependence of resistance (R) measured in each region—the IL-gated (V_{LG}) and solid-gated (V_{SG}) regions—using contacts 1–2 and 3–4, respectively, while a current bias is applied between contacts α and β [Fig. 2(c)]. The capacitance of the aluminum oxide gate dielectric is estimated to be ~0.95 μF cm^{-2}, which is about 80% of the capacitance obtained with IL gating in our experiment, resulting in a charge density of 1.2×10^{13} cm^{-2} at a gate bias of 2 V. For comparison, using a conventional 300-nm-thick SiO_2 dielectric to reach such a charge density typically requires more than 100 V, which exceeds the breakdown voltage of the dielectric. The field-effect mobility of graphene in the IL and solid-gated regions is estimated to be 1000 and 330 cm^2 V^{-1} s^{-1}, respectively. The lower mobility of graphene in the aluminum region indicates that the deposited aluminum and its oxidation may act as scattering centers for graphene, which can be associated with the observed p-doping behaviors. Despite its lower quality, the aluminum oxide layer was robust, maintaining a leakage current of <1 nA during gating.

We also measured the thermovoltage (ΔV) in each region by imposing a temperature gradient along the graphene channel through Joule heating of the heater [Fig. 2(e)]. Thermovoltage measurements complement resistance measurements in studying transport properties of the materials because its magnitude is highly sensitive to the electronic density of states, and its sign directly reflects the type of charge carrier.[42] As expected, thermovoltage signals exhibited positive (negative) values for hole (electron) carriers and reversed sign precisely at the CNP, which is consistent with resistance results for the two regions. The lower magnitude of the thermovoltage in the solid-gated region is attributed to the smaller temperature difference, as this region is farther from the heat source, and to the thermal shunt effect caused by the aluminum covering the channel, which decreases the temperature difference.

To systematically analyze the performance of dual-gate control, we measured both the resistance and thermovoltage across the entire graphene channel using contacts 1 and 4 [Fig. 2(c)], while simultaneously varying the two gate voltages. The fully independent control of the two gates enabled us to investigate these quantities for various combinations of carrier densities and types in each region. Because the two regions are connected in series along the direction of the current path and temperature gradient, the total resistance (R_{tot}) and thermovoltage (ΔV_{tot}) are expected to be a simple sum of the contributions from each region, with a finite constant portion coming from the small ungated region in between. Figure 3(a) presents a 2D color map of total resistance as a function of the two gate voltages, revealing four areas divided by two intersecting ridges with high resistance (lines corresponding to $V_{LG} \approx 0$ V and $V_{SG} \approx 0.5$ V). These high-resistance lines occur when the gate voltages are tuned to the CNP, leading to four characteristic areas, p–n, n–n, n–p, and p–p based on the combination of carrier types in each region.[43] The

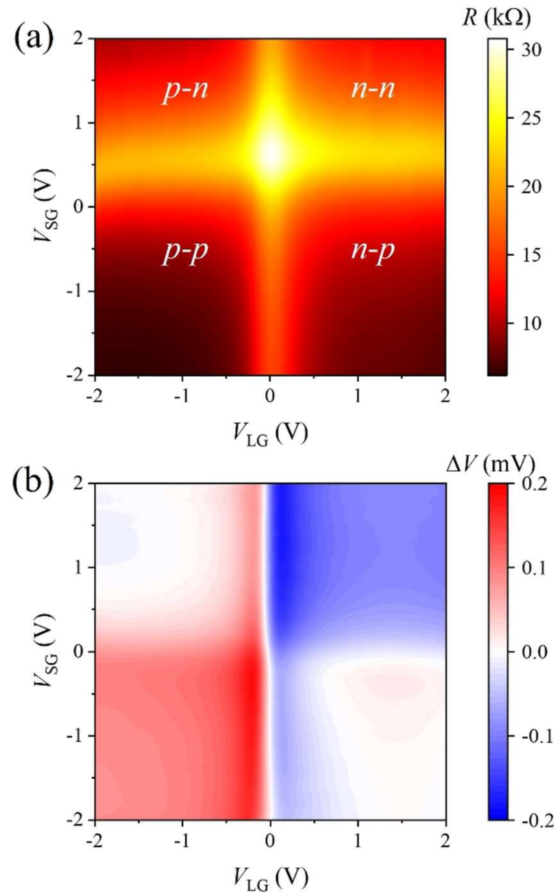

FIG. 3. 2D color maps of total resistance (R_{tot}) and total thermovoltage (ΔV_{tot}) were measured, including both ionic liquid- and solid-gating regions, by simultaneously applying two gate voltages, V_{LG} and V_{SG}. These two gates enable independent control of charge density and polarity in each region. (a) The resistance map showing two high resistance ridges, and the combinations of carrier polarity of the regions labeled as p–n, n–n, n–p, and p–p. (b) Total thermovoltage map showing larger values in the p–p and n–n combinations and relatively smaller values in the p–n and n–p combinations because their magnitudes are determined by the sum of the thermovoltage from each gated region.

total thermovoltage [Fig. 3(b)] exhibits an increased magnitude in the p–p and n–n configurations (as defined in R_{tot}) because each region contributes to the same signal sign with comparable magnitudes. Conversely, the p–n and n–p configurations exhibited small thermovoltages with magnitudes close to zero. The slight coexistence of two opposite signs is associated with the non-monotonicity of the thermovoltage away from the CNP. Consequently, multiple alternating signs are observed in the entire thermovoltage map[44–46] although a mismatch of the boundaries ($V_{LG} \approx 0$ V and $V_{SG} \approx 0.1$ V) with high-resistance lines in R_{tot} is seen owing to the offset voltage coming from the ungated region between IL and SG gated regions. Overall, this clear demonstration of p–n junction formation underscores the reliable operation of the dual-gating performance enabled by the combination of IL and solid gating on the PET substrate.

In summary, we have developed a low-bias operating graphene p–n junction on a flexible PET substrate by integrating the advantages of two distinct high-density electrostatic gating methods—IL gating and high-κ solid-state gating—in a dual-gate configuration, operating at a gate voltage as low as 2 V in both cases. Notably, the solid-state gating is accomplished through a thin high-κ aluminum oxide layer, which forms naturally at the interface between the deposited aluminum and graphene. We demonstrate that the charge densities in two different graphene regions can be independently controlled using these high-density gating methods in a reliable and stable manner. The device architecture presented herein offers an ideal platform for the development of high-performance, energy-efficient 2D material-based electronics that operate at low voltages on flexible and transparent substrates.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Daewon Gu: Investigation (equal); Methodology (equal). **Moonnyeong Choi**: Methodology (equal). **Kyung Ho Kim**: Methodology (equal). **Young Duck Kim**: Methodology (equal). **Munis Khan**: Methodology (equal). **August Yurgens**: Methodology (equal). **Youngwoo Nam**: Investigation (equal); Supervision (lead); Writing – original draft (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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