THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Trapping Effects in Gallium Nitride High Electron Mobility Transistors: Mechanisms, Modeling, and Applications

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Abstract

While GaN-based high electron mobility transistors (HEMTs) have become indispensable for 5G and RADAR systems and shown potential for astronomy and space exploration. Knowledge gaps remain in how epitaxial and processing design impact device performance. Downscaling of GaN HEMTs exacerbates source-drain current dispersion due to trapping and self-heating effects. This thesis focuses on characterizing and optimizing back-barrier/buffer design and processing methods to mitigate trap-induced degradation.

Although back-barrier and buffer doping individually enhance two-dimensional electron gas (2DEG) confinement, carbon-induced trapping creates a trade-off between confinement and dispersion. This work explores variations in carbon doping levels in the GaN buffer and AlGaN back-barrier to improve 2DEG confinement. By employing extensive electrical and spectroscopic methods, trapping mechanisms and their origins are investigated. The results show that dispersion dominates over short-channel effects at the investigated carbon levels, offering guidance for RF performance optimization.

Annealing during gate opening is widely used to counteract damage from fluorine-based plasma treatments. However, the influence of high-temperature pre-gate annealing ($500 - 800\,^{\circ}\mathrm{C}$), particularly in relation to CF_4 and CF_4 chemistries, remains underexplored. This study demonstrates that fluorine implantation and surface oxidation affect device behavior via thermally activated and deactivated traps. It identifies optimal combinations of fluorine plasma and annealing treatments, showing that up to 60 % of CF_4 plasma-induced F^- states can be deactivated by $600\,^{\circ}\mathrm{C}$ annealing.

Buffer trapping is also studied under cryogenic conditions, where Fe-induced traps manifest slow de-trapping dynamics. Field plates are found to mitigate these effects, emphasizing epi-structure and layout design strategies critical for reliable cryogenic GaN HEMT operation.

This thesis further shows that charged states introduced during gate-defining processing can be deliberately harnessed to modulate reverse gate-bias C–V characteristics. By varying fluorine plasma chemistry and pre-gate annealing conditions, the distribution and concentration of charged states in the barrier/channel region can be tuned. This enables the development of GaN-based varactors for MMIC applications, offering low nonlinear distortion in RF systems.

By addressing key challenges in reliability and performance, and exploring emerging applications such as cryogenic operation and varactor integration. This thesis is well placed to advance and diversify GaN HEMT technology.

Keywords: AlGaN/GaN, HEMT, RF, characterization, Trapping effects, downscaling, GaN varactor

List of Publications

Appended Publications

This thesis is based on the content in the following papers:

[A] R. Ferrand-Drake del Castillo, D-Y. Chen, J-T. Chen, M. Thorsell, V. Darakchieva, and N. Rorsman, "Characterization of Trapping Effects Related to Carbon Doping Level in AlGaN Back-Barriers for AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 71, no. 6, pp. 3596-3602, June, 2024.

[B] R. Ferrand-Drake del Castillo, V. Darakchieva, and N. Rorsman, "Effects of Fluorine-Based Plasma Etching and Pre-Gate Annealing on AlGaN/GaN HEMT Characteristics," *IEEE Transactions on Electron Devices*, Submitted: 2025/04/07.

[C] R. Ferrand-Drake del Castillo, B. Hult, M. Thorsell, and N. Rorsman, "Linear C–V Characteristics in GaN HEMT Varactors by Fluorine Plasma-Enhanced Gate Engineering," *IEEE Electron Device Letters*, Submitted: 2025/08/12.

[D] M. A. Mebarki, R. Ferrand-Drake Del Castillo, D. Meledin, E. Sundin, M. Thorsell, A. Papamichail, V. Darakchieva, N. Rorsman, F. Joint, V. Belitsky, and V. Desmaris, "Cryogenic Trapping Effects in GaN-HEMTs: Influences of Fe-doped buffer and Field-Plates," *IEEE Transactions on Electron Devices*, vol. 72, no. 8, pp. 4042-4048, Aug. 2025.

Other Publications

The content of the following papers partially overlaps with the appended papers or is out of the scope of this thesis.

[a] M. A. Mebarki, R. Ferrand-Drake Del Castillo, D. Meledin, E. Sundin, M. Thorsell, N. Rorsman, V. Belitsky, and V. Desmaris, "Noise characterization and modeling of GaN-HEMTs at cryogenic temperatures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 5, pp. 1923-1931, May 2023.

[b] M. A. Mebarki, R. Ferrand-Drake Del Castillo, A. Pavolotsky, D. Meledin, E. Sundin, M. Thorsell, N. Rorsman, V. Belitsky, and V. Desmaris, "GaN High-Electron-Mobility Transistors with Superconducting Nb Gates for Low-Noise Cryogenic Applications," *Phys. Status Solidi A*, vol. 220, no. 8, 2200468, 2023.

[c] R. Ferrand-Drake del Castillo, N. Rorsman, M. Thorsell "GaN Varactor with linear C–V realized through F plasma treatment," *15th ICNS (International Conference on Nitride Semiconductors)*, Malmö, Sweden, July, 2025.

[d] R. Ferrand-Drake del Castillo, D-Y. Chen, J-T. Chen, M. Thorsell, V. Darakchieva, and N. Rorsman, "Impact of Carbon Doping Levels in AlGaN Back-Barriers for GaN HEMTs," *14th ICNS (International Conference on Nitride Semiconductors)*, Fukuoka, Japan, November, 2023.

[e] R. Ferrand-Drake del Castillo, and N. Rorsman, "Considerations in the development of a gate process module for ultra-scaled GaN HEMTs," *CSW (Compound Semiconductor Week)*, Ann Arbor MI, USA, June, 2022.

[f] M. A. Mebarki, R. Ferrand-Drake Del Castillo, D. Meledin, E. Sundin, M. Thorsell, N. Rorsman, V. Belitsky, and V. Desmaris, "Comparison of the low noise performance of GaN HEMTs and MIS-HEMTs at cryogenic temperatures," *18th EuMIC (European Microwave Integrated Circuits Conference)*, Berlin, Germany, September, 2023.

[g] M. Mebarki, R. Ferrand-Drake Del Castillo, and E. Sundin, "A Cryogenic Scalable Small-Signal and Noise Model of GaN HEMTs," *32nd ISSTT (International Symposium on Space Terahertz Technology)*, Baeza, Spain, October, 2022.

[h] M. A. Mebarki, R. Ferrand-Drake Del Castillo, A. Pavolotskiy, D. Meledin, E. Sundin, M. Thorsell, N. Rorsman, V. Belitsky, and V. Desmaris, "GaN HEMT with superconducting Nb gates for low noise cryogenic applications," *CSW (Compound Semiconductor Week)*, Ann Arbor MI, USA, June, 2022.

Abbreviations & Notations

AlGaN	Aluminium gallium nitride
AlN	Aluminium nitride
BV	Breakdown voltage
CC	Current collapse
DUT	Device under test
DCTS	Drain current transient spectroscopy
DIBL	Drain induced barrier lowering
ICP	Inductively coupled plasma
InP	Indium phosphide
FET	Field-effect transistor
GaN	Gallium nitride
GaAs	Gallium arsenide
HEMT	High electron mobility transistor
LNA	Low noise amplifier
LPCVD	Low pressure chemical vapor deposition
MMIC	Monolithic microwave integrated circuit
NF	Noise figure
PA	Power amplifier
PAE	Power added efficiency
PGA	Pre-gate annealing
PIV	Pulsed-IV
PVD	Physical vapor deposition
RF	Radio frequency
RTA	Rapid thermal annealing
SCE	Short channel effect
SEM	Scanning electron microscopy
SiC	Silicon Carbide
TCAD	Technology computer-aided design
TLM	Transfer length method
UID	Un-intentional Doping
2DEG	Two-dimensional electron gas
CF_4	Tetrafluoromethane (Carbon tetrafluoride)
C_{Ga}	Carbon occupying a gallium-vacancy site
C_{I}	Carbon occupying an interstitial site

C_N	Carbon occupying a nitrogen-vacancy site
$DX-like$	Oxygen donor state transitioned to deep acceptor state
E	Electric field
E_a	Apparent activation energy
f_{max}	Maximum frequency of oscillation
f_T	Current gain cut-off frequency
I	Current
I_d	Drain current
I_g	Gate current
I_s	Source current
I_{ds}	Drain-source current
$I_{ds,max}$	Maximum drain-source current
L_{FPD}	Drain field-plate length
L_{FPS}	Source field-plate length
L_g	Gate-length
L_{sd}	Source-drain contact distance
n_s	sheet carrier density
NF_3	Nitrogen trifluoride
P	Power dissipation
R_{on}	On-resistance
R_c	Contact resistance
SiN_x	Silicon nitride (non-stoichiometric)
T_{ck}	Thermal chuck temperature
T_{ch}	Estimated channel temperature
$T_{min-opt}$	Minimum noise temperature
V	Voltage
V_{gs}	Gate-source voltage
V_{dg}	Drain-gate voltage
V_{ds}	Drain-source voltage
$V_{ds,max}$	Maximum drain-source voltage
V_d	Drain voltage
V_{knee}	Knee voltage
V_{po}	Pinch-off voltage
v_s	electron saturation velocity
V_T	Threshold-voltage
W	Device width
μ	Electron mobility
σ	Apparent cross-section
τ	De-trapping time constant

Contents

Chapter 1

Introduction

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) have established themselves as key components in advanced radio frequency (RF) systems, enabling a wide range of applications including fifth-generation (5G) communication infrastructure [1], and defense industry such as RADAR systems [2], while showing potential for future applications within spaceborne communication [3], and radio astronomy systems [4] [5]. These diverse applications place highly demanding requirements on the underlying amplifier technologies, driving the need for solutions that can deliver high output power (P_{out}), efficiency, linearity, dynamic range, and stability across a broad range of operating conditions. In particular, spaceborne and defense platforms are strongly driven by size, weight, and power (SWaP) constraints, where a reduction in SWaP is critical for mission viability, cost, and system integration. The rapid evolution of radio frequency (RF) systems is driving unprecedented demands for power amplifiers (PAs) and low-noise amplifiers (LNAs) in a wide array of sectors, including telecommunications, aerospace, and defense. For 5G and beyond massive multiple input multiple output (MIMO) configurations are utilized, requiring amplifiers that can operate efficiently under high peak-to-average power ratio (PAPR) signals, while ensuring linearity, dynamic response, and power efficiency over wide bandwidths and varying load conditions [6]. Simultaneously, backhaul links place emphasis on maximizing peak output power, and long-term stability, particularly at microwave and millimeter-wave frequencies up to 170 GHz [1].

In the defense and aerospace sectors, active electronically scanned array (AESA) radar systems are evolving toward multifunction and high-duty-cycle operation, placing new demands on efficiency, wideband capability, and dynamic range, while increasingly exploring architectures that benefit from dynamic impedance tuning and load modulation to improve platform agility and reduce power consumption [7]. In satellite communications (Satcom), increasing demand for high data rates, wide bandwidths, and compact ground terminals places emphasis on RF components that offer high efficiency, linearity, and thermal robustness.

For ground and spaceborne applications, heterodyne THz front-ends typically use a cryogenically cooled mixer, such as a NbN-based hot electron bolometer (HEB), to downconvert signals to an intermediate frequency (IF), which is then amplified by a low-noise amplifier (LNA). While InP and SiGe LNAs are common, they face limitations in radiation tolerance, thermal robustness, and power handling. GaN integration, as shown in [8], offers advantages in thermal and power performance.

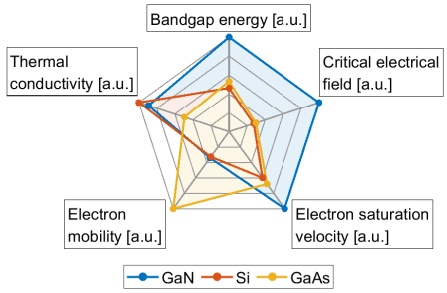


Figure 1.1: Material property comparison between GaN and two legacy semiconductors (Si, GaAs), for parameters relevant to high-power, high-frequency operation. All values are normalized to the material with the highest value for each property, resulting in dimensionless units [a.u.]

On a further note, with the perspective of SWaP constraints, these applications where GaN HEMTs are already indispensable, incentives for a full GaN Monolithic Microwave Integrated Circuits (MMIC) technology have become strong. In these contexts, emerging dynamic load modulation architectures and multifunction array systems demand components with high linearity and predictable behavior [9]. Varactor-based tuning networks, central to these architectures, have traditionally been hindered by nonlinear capacitance-voltage C(V) characteristics and distortion, which limit power handling and integration potential [10].

RF GaN HEMTs

Within this landscape, GaN HEMTs have emerged as a key enabling technology capable of addressing many of the above challenges. The wide bandgap of GaN (Eg = 3.4 eV), combined with a high critical breakdown field ($E_c \approx 3.3$ MV/cm), supports robust device operation under high voltages and powers, with good thermal stability. The polarization-induced two-dimensional electron gas (2DEG) at the AlGaN/GaN interface provides high carrier mobility ($\mu > 2000\ cm^2$/Vs), high electron velocity saturation ($v_s \sim 2 \cdot 10^7$ cm/s), and high sheet carrier density ($n_s \sim 1 \cdot 10^1 3 cm^2$) Fig. 1.1. Together these properties support high current density, (which is critical for large output power and efficiency), fast carrier transport (enabling operation at microwave and millimeter-wave frequencies), and low on-resistance (improving gain and reducing power loss). These properties allow for aggressive downscaling of a GaN HEMT while still maintaining a high output power and breakdown voltage, since a smaller device structure entails lower parasitic capacitances that impede high frequency performance. With these qualities, GaN HEMTs are able to achieve transition frequency and maximum oscillation frequency, (f_T and f_{max}) reaching (454 and 444 GHz) [11]. Thereby enabling 3W/mm output power density at 96 GHz [12]. In this thesis the GaN heterostructure is grown on semi-insulating 4H SiC substrates, thus leveraged by the high thermal conductivity of $3.8\,\mathrm{W\,cm^{-1}\,K^{-1}}$ enabling high output power density and efficiency. Nonetheless, as demonstrated recently by IMEC even a less ideal substrate as Si, can be used for achieving 6G compatible performance combined with using a regrown n^+(In)GaN layer to obtain record-low contact resistance of $0.024\ \Omega \cdot$mm [13]. Up to today, there is ample evidence of how GaN HEMTs outperform other technologies with respect to output power and power added efficiency (PAE) at microwave

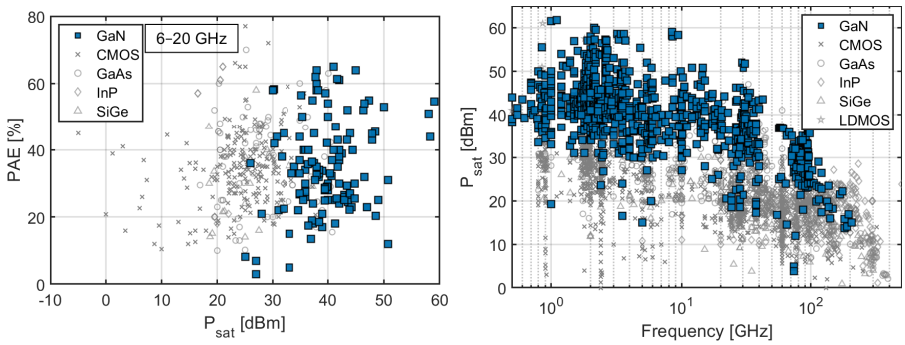


Figure 1.2: **(a)**: PAE and saturated output power (P_{sat}) for different PA technologies within the 6-20 GHz range. **(b)**: the P_{sat} for PA technologies with respect to frequency of operation [14].

frequencies relevant for 5G and RADAR systems, Fig. 1.1a-b.

GaN is a III-V material with stronger atomic bonding compared to InP and GaAs, hence can withstand more ionizing radiation before degrading, making it highly suitable technology for space communication. Furthermore, the potential for monolithic integration between NbN-based HEBs and GaN MMICs makes GaN LNAs with their favorable low noise figure, strong candidates for next-generation low-noise amplification under SWaP-constrained conditions.

Despite these advantages, GaN HEMTs continue to face challenges related to device reliability and stability. Both in terms of thermal and/or trapping induced dispersion, of which the latter is of main concern in this thesis. Charge carriers becoming temporarily trapped at surface states or within the buffer layer, introduce time- and bias-dependent variations (memory effects) in device performance. The resulting increase in dynamic on-resistance and gain compression degrades key amplifier metrics such as linearity, efficiency, and power consistency. In 5G power amplifier systems, especially those operating under high PAPR signals and advanced load modulation schemes, trapping directly limits output power capability and reduces efficiency at power back-off [15]. In AESA radar systems, where PAs must operate over wide bandwidths and duty cycles, low dispersion is essential to maintain linearity and predictable behavior [16]. In spaceborne and high-reliability systems the slow emission rates of trapped charges lead to persistent dispersion and long recovery times, compromising gain stability and noise figure performance under pulsed or varying signal conditions [17]. Hence, minimizing trapping effects remains a critical objective for realizing the full potential of GaN HEMTs in next-generation RF systems.

GaN HEMT Varactors

The same material properties that make GaN an exceptional platform for high-power transistors also make it highly attractive for MMIC-compatible varactors, particularly GaN HEMT and metal–semiconductor–metal (MSM) varactors. These technologies offer a promising route to on-chip tunability in high-power and high-frequency systems. GaN's wide bandgap enables high breakdown voltages and low thermionic leakage currents, allowing for high reverse-bias operation with minimal leakage. This supports improved Q-factor, wider tunability range, and lower distortion under high-

power conditions. Additionally, GaN's inherent thermal stability ensures consistent capacitance behavior in environments with elevated junction temperatures, which is critical in RF power amplifier systems.

Among MMIC-compatible varactors, MSM structures offer distinct advantages due to their inherently low parasitics and high Q-factor, while HEMT-based varactors provide design flexibility by leveraging the transistor structure itself. However, a key limitation in both types remains the nonlinear capacitance-voltage (C–V) behavior, which can degrade overall system performance [18]. In particular, nonlinearity in the C–V response can impact phase and amplitude consistency, which is critical in applications such as beamforming and adaptive RF front ends [19]. Despite recent progress, no study to date has demonstrated a GaN HEMT MMIC-compatible varactor with both high Q-factor and a highly linear C–V response across a broad voltage range. The GaN HEMT varactors investigated in this thesis address this gap by introducing new strategies for engineering linear C–V behavior in both HEMT and MSM device architectures.

Thesis Motivation and Outline

Charge trapping phenomena arising from defects and impurities at the surface, barrier, and buffer represent a key impediment to achieving high efficiency, output power, and dynamic stability in power amplifiers and other MMIC components. This thesis is motivated by the dual need to suppress these unwanted trapping effects in GaN HEMTs while also exploring opportunities to deliberately manipulate charge states introduced during processing.

Chapter 2 discusses the design features of RF AlGaN/GaN HEMTs and their relation to trapping behavior, along with a brief overview of the electrical and spectroscopic techniques used for trap characterization.

Chapter 3 presents a detailed study on minimizing trapping effects across cryogenic temperatures, room temperatures up to 160 °C. Detailing how these effects manifest in DC, pulsed-IV, small- and large-signal operations. The origin and nature of different trap states are analyzed using both electrical and spectroscopic methods. In paper [A] special focus is given to the role of back-barrier C-doping, whereas iron buffer doping in cryogenic LNAs is treated in Paper [D]. Additionally, minimization of process related traps induced by F plasma and how an additional annealing process for removal of the same traps is treated in Paper [B]

Chapter 4 presents a method for realizing GaN varactors with highly linear reverse-bias C(V) characteristics using standard GaN HEMT processing steps [Paper C]. This enables co-integration with power amplifier technologies with minimal additional fabrication. As a result, discrete components can be eliminated, reducing interconnect parasitics, size, and packaging complexity, while improving system-level reliability and performance. Small-signal measurements and TCAD simulations are used to assess device behavior and model charge distribution effects on C(V) linearity.

Collectively, these studies provide a deeper understanding of trapping physics with a dual approach of mitigating harmful traps while leveraging controllable charge states. The findings of this thesis introduce practical pathways for performance enhancement through optimization of epitaxial design, device layout, and processing strategies.

Chapter 2

RF GaN HEMTs Design and Characterization

This chapter lays the groundwork for the thesis, building on previous descriptions of GaN HEMT technology [20]. Efforts to downscale these devices for enhanced high-frequency performance often exacerbate transient effects, i.e. charge trapping and self-heating induced performance drift. Wherein trapping is the primary concern of this thesis. As a wide-bandgap III-V semiconductor, GaN is particularly susceptible to trapping effects, which, if left unaddressed, can reduce the reliability of GaN HEMTs. Consequently, comprehensive methods for trap characterization are needed when optimizing the epitaxial structure and refining device processing. Given that the transient response of GaN HEMTs may arise from both thermal dynamics and charge trapping, careful attention must be paid to measurement chronology, bias levels and experimental setup. Below, a brief introduction to the GaN HEMT technology and the origin of trapping behavior is detailed. Thereafter, various measurement methods for identifying and quantifying trap states are elucidated.

2.1 Epi-structure engineering

The AlGaN/GaN HEMT heterostructure has ever since its conception in the 90's been grown on a foreign substrate [21], although native substrates are emerging, industrial processing is mostly limited to Sapphire, Si and SiC substrates for 100 mm wafer sizes [22]. Out of thermal management reasons and relatively well-matched lattice constants, GaN HEMT power amplifiers are preferably based on a heterostructure using semi-isolating SiC 4H substrate (rather than Si). Since the thesis does not concern N-polar devices, the epitaxial growth detailed below is applicable for a Ga-polar orientation growth.

The aspect of GaN being grown on foreign substrate entails elevated epitaxial dislocation density, which ideally is kept to a minimum in the channel layer where the 2DEG resides. Typically, this is achieved by growing an AlN nucleation layer to bridge the lattice mismatch combined with a thick GaN buffer layer. The most common growth technique metal organic chemical vapor deposition (MOCVD) inevitably leads to residual impurities (Si, O and N-vacancies) in un-intentionally doped (UID) Ga-polar (Al)GaN, resulting in n-type doping [23]. Thus, the thick GaN buffer provides an

alternative un-gated leakage path between source and drain, limiting gate-modulation of the 2DEG. To maintain high 2DEG confinement, Fe and C buffer doping was introduced [24] [25]. Both elements have the net effect of acting as deep-level acceptor states, raising the buffer resistivity, thereby inhibiting un-gated leakage paths. An alternative method to increase 2DEG confinement is to use back-barriers, by such means creating a conduction band discontinuity between the channel layer and the back-barrier, which may include AlGaN, InGaN, and AlN layer [26] [27] [28] [29].

The top barrier exhibits intrinsically a sufficiently large piezoelectric and spontaneous polarization charge in tandem with surface state donors to give rise to a 2DEG predominately located in the underlying GaN channel. Generally, the top barrier consists of an Al_xGa_{1-x}N layer where an increase in x leads to a larger polarization field, forcing the electrons towards the underlying GaN layer. Note that x is limited to ca 0.3 imposed by risk of lattice relaxation [30]. This effect together with the conduction-band discontinuity ensures an electron confinement inside the GaN layer. However, having AlGaN as a surface layer is not preferable out of reliability concerns due to Al being highly prone to oxidation and giving rise to gate-lag and current-collapse. A GaN cap is instead often used as the topmost layer of the top barrier. Although this leads to a slightly lower 2DEG concentration, it improves device reliability [31]. At the Al_xGa_{1-x}N/GaN interface (x = 0.3), part of the 2DEG distribution will extend into the AlGaN layer, hence compromising the electron mobility. Therefore, an ultrathin 1-2nm AlN layer, (below the critical thickness for lattice relaxation) is inserted between the AlGaN and GaN layers, Fig. 2.1a.

The main characteristics to describe the 2DEG are the electron sheet concentration (n_s), mobility (μ) and saturation velocity (v_s). With a higher polarization, the higher the n_s becomes, whereas μ and v_s are mostly dependent on crystal quality and AlN/GaN interface sharpness. Although it should be mentioned that v_s could degrade due to increased electron-electron interactions, which become more prevalent with higher 2DEG concentration [32].

2.2 HEMT Layout design and contact formation

The bare epitaxial structure described above needs to be processed to obtain the functionality of a three terminal device such as a transistor. Source and drain should have pure ohmic contact with minimal contact resistance to the 2DEG, thereby ensuring high I_{ds} and linear correlation towards V_{ds}. The third contact (gate) on the other hand forms a Schottky contact, which through the field effect will modulate the current between source and drain Fig. 2.1a. In this thesis two-finger co-planar devices are used, with a symmetrical plane going vertically through the middle of the gate and drain contact pads Fig. 2.1b. This enables a more compact device design as opposed to single fingered devices, while avoiding the need for complex processing using e.g. air-bridges as is the case of devices with more than two fingers. Additionally, by using co-planar design, control of characteristic impedance is enhanced while parasitics are kept low compared to e.g. microstrip where ground plane and signal plane are vertically separated.

Apart from potential aggravation of memory effects, the downscaling of GaN HEMTs poses challenges in electric field management to maintain a high breakdown voltage, thus influencing layout design. During operation the largest potential differences will be between gate and drain. Therefore, the gate-drain distance (L_{gd}) is kept

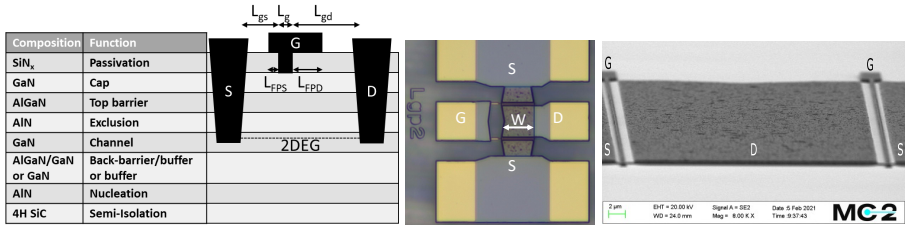


Figure 2.1: HEMT cross-section and layout [C], (a): typical epitaxial layer stack used in this thesis, note the layer below the GaN channel layer varies between studies. **(b)**: optical top-view image with labels showing source,drain, gate contacts and device width. **(c)**: Scanning electron microscope image taken at an angled view before contact pad deposition.

larger than gate-source distance (L_{gs}) Fig. 2.1a, thereby ensuring that the breakdown voltage is maximized for a given source-drain distance (L_{sd}) and gate-length (L_g). The gate exhibits a T-shaped structure with field plates, (deposited on the SiN_x passivation layer) which extend towards source (L_{FPS}) and drain (L_{FPD}) Fig. 2.1a. Although field plates introduce additional parasitic capacitance, it lowers the gate-resistance and the peak electric field, thus ensuring higher breakdown voltage while also reducing the severity of trapping effects most notably in cryogenic environments, Paper [D].

A typical cross-sectional epitaxial structure used in this thesis is shown in Fig. 2.1a, with dimensions indicated along the current flow direction.While [Papers B, C, and D] employ a GaN buffer structure, [Paper A] uses an AlGaN/GaN back-barrier and buffer combination to improve 2DEG confinement.

An optical microscope top-view image taken from a normal angle to the device shows a typical device layout with all three contact terminals denoted including the gate width (W), Fig. 2.1b. A device prior to contact pad deposition is seen in Fig. 2.1c.

2.3 HEMT fabrication

Processing technique and sequence is of high import when understanding the final device performance, as detailed in Paper [B]. Here the typical processing steps for GaN HEMT fabrication is presented. Except for Paper [B], the reader can assume these main steps and chronology to represent how all devices in the thesis were processed.

The wafers processed in this thesis are provided by different foundries, and delivered with the epitaxial structure as shown in Fig. 2.2a. Where the GaN heterostructure is grown upon a semi-isolating 4H-SiC 100mm substrate. The wafer is diced into 20x20mm chips before processing, thereafter the chips individually go through the following process steps:

SiN_x Passivation

The positively charged surface states in the GaN cap act as electron traps under off-state and high drain bias. Silicon nitride (SiN_x) passivation has been shown to be successful in reducing the density of surface states, [33] [34]. For this purpose low-pressure chemical vapor deposition (LPCVD) has proved to be most effective as opposed to plasma enhanced CVD (PECVD) [35]. Generally, passivation with LPCVD requires a passivation-first process due to the high temperature involved (up to 820°C), which is

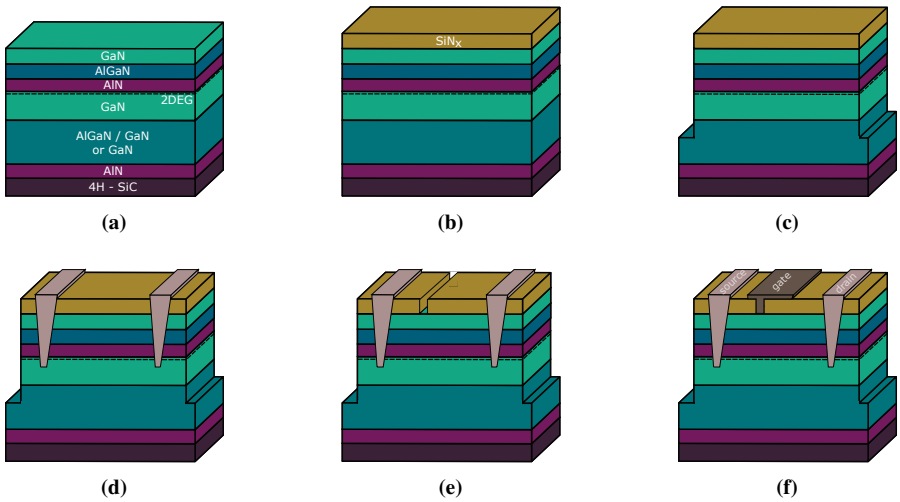


Figure 2.2: step-by-step HEMT processing, (a): The bare wafer pre-processing. **(b)**: SiN_x passivation deposition. **(c)**: MESA isolation etch down into the highly resistive AlGaN back-barrier or GaN buffer. **(d)**: OHMIC metal processing, connecting source and drain to the 2DEG. **(e)**: Gate opening process, recess etch through the SiN_x enabling Schottky gate formation. **(f)**: Gate metal deposition, now all three terminals are established.

not compatible with ohmic or gate mentalization, Fig. 2.2b. Passivation-first ensures no processing related impurities impact the sensitive surface states of the GaN cap.

Mesa Isolation

Electrical isolation is essential to prevent unwanted conduction paths or leakage currents between adjacent GaN HEMT devices. In this thesis, isolation is implemented using MESA etching via Cl-based inductively coupled plasma (ICP), by etching down to the highly resistive AlGaN back-barrier or GaN buffer Fig. 2.2c. An alternative approach is ion implantation, which introduces insulating defects through high-energy ion bombardment [36]. While ion implantation offers smoother surface morphology and avoids issues like sidewall leakage and gate structure fragility, its main advantage lies in preserving breakdown voltage [37]. However, since this work focuses on high-frequency rather than high-power applications, MESA isolation remains a practical choice.

Ohmic Contact Formation

Achieving low contact resistance to a wide-bandgap material such as GaN is challenging but essential, particularly in high-frequency devices where contact resistance constitutes a larger part of the total on-resistance as device dimensions are scaled down. In this work, ohmic contacts were formed by first recess etching through the barrier and partially into the GaN channel, exposing the 2DEG along the GaN channel sidewall, as illustrated in Fig. 2.2d.

An alternative approach, is the use of regrown n^+(In)GaN contact layers, which can achieve contact resistances as low as $0.024\ \Omega \cdot \text{mm}$ [13]. However, such regrown contacts require selective-area epitaxy using MOCVD or molecular beam epitaxy

(MBE), technologies that were not readily available during this thesis work. Instead, a metal stack was directly deposited onto the recessed region followed by rapid thermal annealing (RTA).

The annealing step induces interfacial reactions that reduce the Schottky barrier height (ϕ^B) and enable carrier transport across the metal–semiconductor interface. For ohmic contacts to GaN, tunneling transport is expected to dominate over thermionic emission due to the material's wide bandgap [38].

The metal stack used in this thesis was Ta/Al/Ta (25/280/15 nm) [39]. Tantalum was chosen not only for its relatively low metal work function (ϕ_0 = 4.19 eV [40]), but more importantly for its ability to react with GaN and form TaN. This reaction extracts nitrogen from the GaN surface, generating nitrogen vacancies that enhance tunneling probability [18].

Compared to conventional ohmic schemes, using planar contacts annealed at 800 - 900°C [41] [42], this approach enables low-temperature processing at around 550°C. The reduced thermal budget minimizes the risk of 2DEG degradation due to atomic diffusion and yields improved surface morphology. The resulting contact resistance for this process typically falls in the range of 0.3–0.5 $\Omega \cdot$ mm.

Gate Opening

patterning for gate opening is done through e-beam lithography. Gate opening is performed by selectively etching the SiN_x layer using a fluorine-based ICP process to expose the underlying GaN cap, enabling Schottky gate metal deposition in the subsequent step. Since this step defines the gate length (L_g), precise dimensional control is critical. Furthermore, exposure of the GaN surface to fluorine plasma can impact device performance negatively, making the choice of plasma chemistry, control of etch duration, and post-etch recovery strategies especially important. These considerations are addressed in detail in this thesis through an extensive study presented in Paper [B].

Gate Metal Deposition

The Schottky gate is deposited using a Au/Pt/Ni (450/20/30 nm) metal stack, as illustrated in Fig. 2.2f. This step involves a dedicated e-beam lithography process, separate from the gate opening, which can introduce a $\sim$ 50 nm offset between the gate and the field plate. While alignment to the gate opening is generally critical particularly for minimizing parasitic capacitance and ensuring effective field modulation the gate architecture used in this work is relatively forgiving to small misalignments. This is in contrast to mushroom gates where the reduced overlap makes precise alignment more critical, although it should be mentioned that slight overlap i.e. mini/micro-field-plates are demonstrated to ensure lower current collapse (CC) and better power density scaling [43]. Moreover, since this thesis does not investigate breakdown voltage characteristics, which are strongly influenced by field plate design [37], such minor deviations are not expected to significantly affect the results. In the cryogenic trapping study (Paper [D]), where field plate dimensions were found to influence performance, SEM imaging confirmed no deviations from the nominal design geometry.

Contact Pad Deposition

Contact pads, formed after all terminal metallization steps (not shown in Fig. 2.2f), are fabricated using a Ti/Au/Ti (30/300/20 nm) metal stack. The bottom Ti layer promotes adhesion to the underlying layers, while the thick Au layer ensures low electrical resistance. These pads serve as probing interfaces for electrical characterization of the devices. The processing steps conclude at this stage. In a complete MMIC process, additional steps would be required. However, such steps could potentially degrade HEMT performance. Therefore, this work reports HEMT performance based on a minimal set of necessary processing steps.

2.4 HEMT operation

Intrinsically, the GaN HEMT is usually a normally-on (depletion-mode) device. Hence, turning off the device, i.e. depleting the 2DEG below the gate, necessitates a negative bias on the gate contact, sufficiently large to elevate the two-dimensional quantum well above the fermi level. Whereas a gate-source voltage V_{gs} exceeding the threshold voltage (V_T), enables 2DEG accumulation. By adjusting the forward gate bias, the electron sheet density (n_s) in the 2DEG can be modulated, thereby directly influencing I_{ds}. However, no current can flow unless a non-zero V_{ds} bias is applied, inducing an electric field forcing free electrons from source to drain, where the μ determines how efficiently electrons accelerate under the electric field. At a sufficiently high V_{ds}, the I_{ds} saturates, as the drift velocity approaches the material's v_s. Unto this day, new studies attempt to link the abovementioned physical parameters to an analytical expression for $I_{ds}(V_{gs}, V_{ds})$ [44]. With the resistive and saturation region current described as:

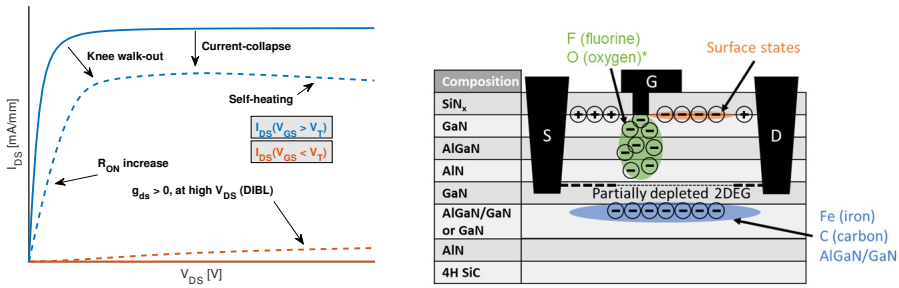
$$I_{\text{ds,resistive}} = \frac{q\mu n_s}{L_g} V_{ds} \tag{2.1}$$

$$I_{\text{ds,saturation}} = \frac{q\mu n_s}{L_g} \cdot \frac{v_{\text{sat}}(V_{gs} - V_T)}{v_{\text{sat}} + \left(\frac{\mu}{2L_g}\right)(V_{gs} - V_T)} \tag{2.2}$$

Where q is the electron charge. A unified expression of Eq. (2.1) and Eq. (2.2) for all drain-source current was formulated as:

$$I_{DS} = \frac{I_{\text{DS,resistive}} \cdot I_{\text{DS,saturation}}}{\sqrt{I^2_{\text{DS,resistive}} + I^2_{\text{DS,saturation}}}} \tag{2.3}$$

From this expression Eq. (2.3), ideal output characteristics, without self-heating, trapping and short channel effect (SCE) is depicted with solid lines in Fig. 2.3a. To contrast the ideal case, striped lines of a physical device measurement are displayed Fig. 2.3a. For $V_{gs} < V_T$, the device is expected to remain off ($I_{ds} = 0$) independent of V_{ds} bias, but for the non-ideal case the output conductance ($g_{ds} > 0$), i.e. gate control is compromised leading to SCE. In the case of $V_{gs} > V_T$ multiple non-ideal effects are depicted, primarily caused by trapping and/or self-heating. Electron trapping can occur at various sites within the epitaxial structure, such as at surface states, interfaces, in the gate vicinity, or within the buffer/back-barrier layers. The location and nature of the trap strongly influence the dynamics of charge capture and emission. Which in turn affects the transient and steady-state performance of the device. In this thesis



(a) **(b)**

Figure 2.3: **(a)**: off- (orange) and on- (blue) state output characteristics of ideal HEMT (filled lines) contrasted to a HEMT suffering from dispersive and SCEs (striped lines). **(b)**: electrons can get trapped in different locations in the epitaxial structure, here three different regions with likely trap states are exemplified. Trapped electrons will cause a reduction in the 2DEG density. *Although O typically acts as a donor state, it can act as a DX-like acceptor state [47].

three main regions for potential trapping are depicted in Fig. 2.3b, which are addressed depending on the study split.

2.5 Trap origin

Any deviation from an ideal crystal structure periodical arrangement can be considered as a defect state. Examples are point-defects, vacancies, interstitials and antisite, extended defects, screw dislocations, edge dislocations, interface states and impurities [45]. Whenever considering an optimal epi-structure used for effective 2DEG confinement, attention towards how the proposed design will influence the density of defect states in vicinity of the 2DEG is crucial. The defect states introduce allowed energy-states within the forbidden energy gap of GaN, with varying trapping/de-trapping time constants, causing a time-dependent partial depletion of the 2DEG Fig. 2.3a, creating I_{ds} time-transient behavior depending on the previous bias-settings the HEMT has been subjected to. Commonly reported de-trapping time constants range from μs to a few seconds [46], hence potentially having adverse impact on the performance of RF GaN HEMTs. Therefore, a central theme throughout this thesis is how trapping can be minimized [Papers A, B and D]. With [Paper C] serving as the exception where surface charge state modulation instead is utilized for enhancing GaN varactor performance.

2.6 Conventional IV and Signal-Based Measurements

This chapter presents the electrical measurement techniques employed throughout the thesis to evaluate device performance. Each subsection first introduces the method in a general context, outlining the key parameters and figures of merit that can be extracted.

To emphasize the central theme of trap characterization, each method is subsequently revisited in a dedicated section, where its specific relevance to trapping effects is discussed. In this way, the reader can clearly distinguish between standard measurement principles and their interpretation in the context of charge trapping.

2.7 DC Measurements

Direct current (DC) measurements are widely used to extract low-frequency or steady-state parameters in field-effect transistors. Among the key figures of merit obtained from DC sweeps and referenced throughout this thesis are the threshold voltage (V_T), saturation current ($I_{ds,sat}$), knee current (I_{knee}), knee voltage (V_{knee}), transconductance (g_m), on-resistance (R_{on}), subthreshold swing (SS), and drain-induced barrier lowering ($DIBL$).

How these parameters are influenced by trapping is hard to discern due to most being influenced by self-heating, (and may have quasi-static behavior). Therefore low-power conditions are typically used when attempting to link DC performance to trapping effects. In this thesis, such an approach is used in [Paper A], where R_{on}, SS, and DIBL are analyzed as indirect indicators of charge trapping.

SS and DIBL are extracted from the transfer characteristics near the threshold or pinch-off region. DIBL is determined by tracking the shift in V_{gs} required to reach a defined pinch-off current (I_{po} = 1 mA/mm) across different V_{ds} values. SS is obtained from the steepest slope of the $\log(I_{ds})$ versus V_{gs} curve in the subthreshold regime, as illustrated in Fig. 2.4.

$$\mathrm{DIBL} = \frac{V_{\mathrm{po,high}} - V_{\mathrm{po,low}}}{V_{\mathrm{ds,high}} - V_{\mathrm{ds,low}}} = \frac{\Delta V_{\mathrm{po}}}{\Delta V_{\mathrm{ds}}} \tag{2.4}$$

$$\mathrm{SS} = \frac{\delta V_{gs}}{\delta \log_{10}(I_{ds})} \tag{2.5}$$

Lower DIBL and SS values typically indicate improved gate control and reduced short-channel effects. R_{on} is extracted from the output characteristics in the linear regime, with the gate in forward bias and drain voltage kept low. In this region, R_{on} primarily reflects access resistance and carrier mobility.

DC Trap Characterization

In [Paper A], an increase in negatively charged traps (e.g., electrons at the channel or back-barrier interface) was shown to cause further depletion of the 2DEG through a back-gating effect. This led to lower apparent SS and $DIBL$ values, even though the actual gate control was not improved. Simultaneously, the reduced channel conductivity also resulted in an increase in R_{on}.

Thus, under low-power DC conditions, a combination of low SS and $DIBL$ with increased R_{on} may indicate the presence of trapped charge. However, because de-trapping in III-nitride materials can occur over timescales of several seconds, DC measurements may capture non-equilibrium charge states and should therefore be interpreted with caution. For example, in [Paper B], slow F^--related traps induce apparent permanent shifts in threshold voltage (V_T), as the measurement timescale is shorter than the de-trapping time of these states at room temperature [48].

2.7.1 Pulsed IV Measurements

As described in the previous section, DC measurements are constrained not only by self-heating, which can mask or distort trapping phenomena, but also by long transient effects that may result in apparent steady-state readings that are, in fact, non-equilibrium. Pulsed IV (PIV) measurements overcome these limitations by applying

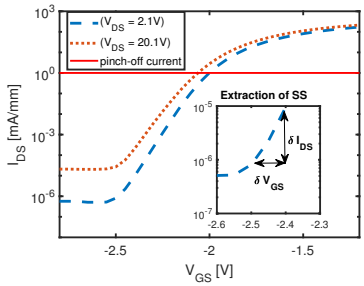


Figure 2.4: Transfer characteristics at low and high V_{ds} showing DIBL extraction from I_{po} intersections. Inset: region used for SS extraction.

short, low duty-cycle voltage pulses to the gate and drain terminals. This approach minimizes thermal effects and allows for time-resolved analysis of charge dynamics.

In this thesis, PIV measurements were implemented with pulse widths of approximately 1 μs and a duty cycle of 1 %. This ensures that most of the self-heating, which occurs on millisecond timescales, is avoided, and any generated heat can dissipate between pulses.

The distinction between gate-lag and drain-lag configurations is illustrated in Fig. 2.5a. In gate-lag mode, the drain-pulse defines the measurement window, and no drain field is present during the quiescent period. In drain-lag mode, the gate-pulse defines the window, ensuring no heating occurs during off periods. The current is typically sampled at the center of the measurement pulse to avoid distortions due to transients.

Fig. 2.5b shows a representative PIV sweep for five different quiescent bias conditions, labeled by their gate and drain quiescent voltages: Q_{ref} (0,0), Q_g (gate-lag), and Q_{d1}–Q_{d3} (increasing drain-lag bias).

Current collapse $Z(Q_x)$ is defined as the relative reduction in saturation current compared to the reference condition:

$$Z(Q_x)\,[\%] = \frac{I_{ds}(Q_x) - I_{ds}(Q_{\text{ref}})}{I_{ds}(Q_{\text{ref}})} \cdot 100 \tag{2.6}$$

PIV Trap Characterization

PIV enables qualitative insight into the spatial origin and dynamics of traps through the use of targeted quiescent bias conditions. Therefore, extensively used method for trap evaluation, as demonstrated in [Paper A, B, and D]. While no single pulse scheme can isolate surface from buffer traps entirely, the relative contributions of each can be inferred. In Fig. 2.5b , gate-lag measurements, which apply a negative quiescent gate bias and zero drain bias, predominantly activate surface traps, hence a slight CC and increase in R_{on} is seen. Drain-lag measurements, which include both gate and drain quiescent biases, activate both surface and deeper buffer traps, hence typically manifesting a larger CC and dynamic-R_{on}. With increasing quiescent drain bias progressively larger trapping is seen Fig. 2.5b , likely located in the buffer/back-barrier region.

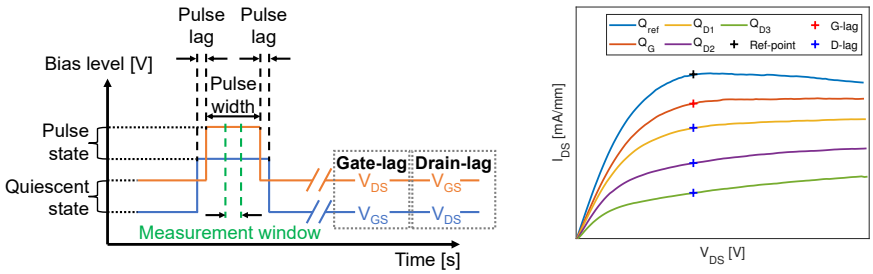


Figure 2.5: (a) Time-domain schematic of PIV operation, illustrating the timing of gate and drain pulses for gate- and drain-lag configurations. **(b)** Output characteristics of a GaN HEMT measured under five different quiescent bias conditions. CC and increased dynamic-R_{on} are observed in both gate- and drain-lag cases relative to Q_{ref}.

2.7.2 Small-signal operation

Initial assessment of high frequency performance is done through small signal measurements. With sufficiently small input and output signals, an inherently non-linear device such as a GaN HEMT can be considered linear, thus simplifying the description of the intrinsic parameters. However, this approximation means that the modelled equivalent circuit is only applicable for the specific bias point for which the parameters are extracted. Through extracted s-parameters the small signal current and unilateral power gains can be obtained, which by extension is used to obtain two figures of merit at which frequency the short-circuit current and the unilateral power gain become 0 dB denoted as transit frequency (f_T) and maximum oscillation frequency f_{max}. f_T can be expressed in terms of transconductance g_m, gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}, typically C_{gd} is neglected since L_{gs}<L_{gd} [49].

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{2.7}$$

f_{max} depends on additional parameters such as R_i,R_s and R_g, which represent gate charging, source and gate resistance, including g_{ds} which is the output conductance [50].

$$f_{\max} = \frac{f_T}{2\sqrt{(R_i+R_s+R_g)g_{ds}+2\pi f_T R_g C_{gd}}} \tag{2.8}$$

Small-signal Trap Characterization

In [Paper A], f_T and f_{max} were found to be relatively insensitive to trapping-induced dispersion effects, only for sufficiently large V_{ds} could some insight into the dispersive behavior of the devices be observed in f_{max}. Although the reader should note that dispersion was better addressed through large-signal measurements.

2.7.3 Large-Signal Operation

Power amplifiers (PAs) often operate under large-signal conditions. Key figures of merit in this regime include output power (P_{out}), PAE, gain, and linearity. The

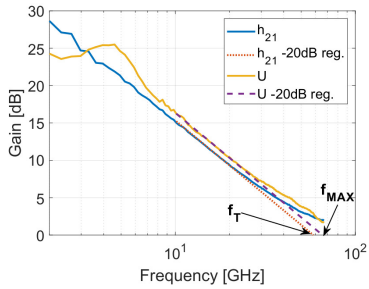


Figure 2.6: the extraction of f_T and f_{max} is extracted by using the small signal unilateral power and current gain (U and h_{21}) and by imposing a -20dB/decade regression line.

maximum output power ($P_{out,\max}$), as expressed for Class A operation in Eq. (2.9), corresponds to RF voltage and current swings that fully span the device's load line from the knee point to the off-state at maximum V_{ds}.

$$P_{\text{out,max}} = \frac{(V_{ds,\max} - V_{ds,\text{knee}})(I_{ds,\text{knee}} - I_{ds,\text{off}})}{8} \tag{2.9}$$

PAE quantifies how efficiently a power amplifier converts DC power (P_{DC}) into additional RF output power, Eq. (2.10):

$$\text{PAE} = \frac{P_{\text{out}}^{\text{RF}} - P_{\text{in}}^{\text{RF}}}{P_{\text{DC}}} \tag{2.10}$$

In Fig. 2.7, two load lines are shown for Class AB operation (an operation mode that is typically chosen as a compromise between $P_{out,\max}$ and $PAE_{\max}$). The ideal case assumes no dispersive or SCE, while the non-ideal case includes them. The latter thus demonstrates a reduction in the usable RF swing and hence limiting both P_{out} and PAE.

Large-Signal Trap Characterization

Under RF operation, trapping-related dispersion manifests as a reduced output current swing, particularly near the knee region. This results in a decrease in $I_{ds,\text{knee}}$ and an increase in $V_{ds,\text{knee}}$ (Fig. 2.7), ultimately leading to a reduction in $P_{out,\max}$ and degradation of PAE. In contrast, short-channel effects (SCE) such as the loss of gate control at high V_{ds}, cause an elevation in $I_{ds,\text{off}}$, Fig. 2.7, which increases DC power consumption and further reduces PAE. Additionally, the increased self-heating can impair P_{out} by degrading carrier mobility.

In aggressively scaled devices, a critical trade-off emerges between mitigating SCE and suppressing trap induced dispersion. This trade-off is central to the back-barrier C-doping study reported in [Paper A].

Whereas DC and PIV measurements can reveal manifestations of SCE or dispersion under specific bias conditions, they fall short of capturing their interaction under realistic RF stress. The large-signal load-pull methodology enables joint analysis of P_{out} and PAE across frequency and power levels, providing a more comprehensive picture. By tracking these metrics simultaneously, the dominant degradation mechanism, whether trap-related or due to SCE can be identified.

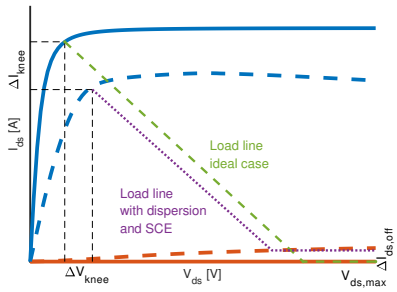


Figure 2.7: the demonstrated dispersive and SCE seen in Fig. 2.3a result in a Compressed load line swing compared to the ideal case.

2.8 Trap Analysis

In the above mentioned measurement techniques, ample ways of describing trapping is provided. However, the manifestation of trapping may be difficult to ascribe to a certain device epitaxial design, layout or processing technique and by extension, to a specific defect. Thus, an additional measurement technique is implemented throughout this thesis, drain current transient spectroscopy (DCTS). which facilitates to go from showing correlation to causation by providing the means to tie specific trap signatures to a specific defect state.

2.8.1 Drain Current Transient Spectroscopy

Drain Current Transient Spectroscopy (DCTS) is a technique based on Shockley-Read-Hall (SRH) theory used to characterize trap states in GaN HEMTs. Similar to Pulsed IV (PIV), a specific bias condition, called the filling state, is applied for a fixed duration to activate trap states. In this thesis, the fill state typically corresponds to an off-state with the gate bias $V_{GF} < V_T$, and a filling time of 10 s is frequently used.

The filling-state drain voltage V_{DF} influences which traps are activated. A low V_{DF} tends to activate surface-related traps, while a high V_{DF} can engage both surface and buffer/back-barrier traps. The device is then pulsed into an on-state, where the gate voltage $V_{G,ON}$ is typically set to 1 V. The drain voltage $V_{D,ON}$ is kept low to avoid self-heating, which could distort transient behavior and obscure trap detection [51]. However, since some traps induce not only dynamic R_{on} degradation but also V_T shifts [52], an accurate characterization often requires biasing the device in the saturation regime. Therefore, in this thesis, most DCTS measurements use $V_{D,ON}$ values above the knee voltage, typically 4–6 V.

Modeling Current Transients and Extraction of Trap Parameters

By analyzing the transient drain current following the gate or drain voltage pulse, DCTS allows for the extraction of key trap parameters, such as activation energy (E_a) and capture cross-section (σ). These parameters are generally evaluated under the assumption that thermionic emission dominates over tunneling as the primary de-trapping mechanism [52]. The transient current can be modeled using stretched exponentials as described in [53]:

$$I_{DS}(t) = I_{DS,\text{final}} - \sum_{i=1}^{N} \alpha_i \exp\left[-\left(\frac{t}{\tau_i}\right)^{\beta_i}\right] \tag{2.11}$$

Here, N is the number of distinguishable transient components; α_i is the amplitude, τ_i is the de-trapping time constant, and β_i is the stretching exponent associated with the i^{th} trap. A value of $\beta_i \approx 1$ suggests a narrow energy distribution, typical of discrete point defects, while $\beta_i \ll 1$ indicates a broader distribution, often linked to extended or interface-related trap states.

Under the thermionic emission assumption, the time constant τ_i varies with channel temperature. Measuring τ_i across a temperature series enables extraction of E_a and σ through an Arrhenius plot [51], using the relation:

$$\ln(\tau T^2) = \ln\left(\frac{\gamma}{\sigma}\right) + \frac{E_a}{kT}, \quad \gamma = \frac{h^3}{2(2\pi)^{3/2}\sqrt{3}\, m_e^* k^2} \tag{2.12}$$

Here, the channel temperature T denotes the estimated channel temperature, which is calculated based on the chuck temperature t_{chuck}, the dissipated power P_D, and a thermal resistance $R_{\text{th}} \approx 5\,\text{K mm/W}$, the value of which reflects devices with a finger pitch of $\sim 100\,\mu\text{m}$ and finger width of $\sim 50\,\mu\text{m}$, [54].

It is important to note that extracting the actual values of E_a and σ presents several challenges. For instance, the extracted time constants τ_i in such fits represent effective values, not single emission rates, especially when $\beta_i \ll 1$. This spectral dispersion can distort Arrhenius plots, leading to inaccurate activation energies E_a, often underestimated or non-physical. Since the capture cross-section σ is derived from the same fit intercept, its accuracy is equally affected. These issues are particularly critical when multiple traps contribute simultaneously to the transient [52]. Furthermore, the extraction of σ can be complicated by the nature of the defect states. For non-interacting point defects, the capture rate remains constant, and the trap occupancy depends exponentially on the fill pulse time, making σ effectively time-independent. However, for interacting point defects (such as those arranged linearly) electrons already captured create a time-dependent Coulombic repulsive potential. This repulsion suppresses subsequent capture events, effectively reducing the capture cross-section σ over time. This effect becomes more pronounced when the fill time is significantly longer than the characteristic emission time constant τ of the trap [55]. While stretched exponentials offer robust empirical fits, care must be taken in interpreting the extracted parameters as uniquely representing physical trap states.

DCTS Implementation

All DCTS measurements in this thesis were performed using an AMCAD AM3200 PIV system, capable of resolving transients from microseconds to tens of seconds. Elevated chuck temperatures were used to accelerate long de-trapping processes and reveal traps not detectable at room temperature. For reliable extraction of trap parameters, the following criteria were enforced:

- Good fitting of all I_{DS} transients across the temperature range.
- Minimal drift in β with temperature.
- Linear Arrhenius plots across at least four temperature points with $\alpha > 0$.

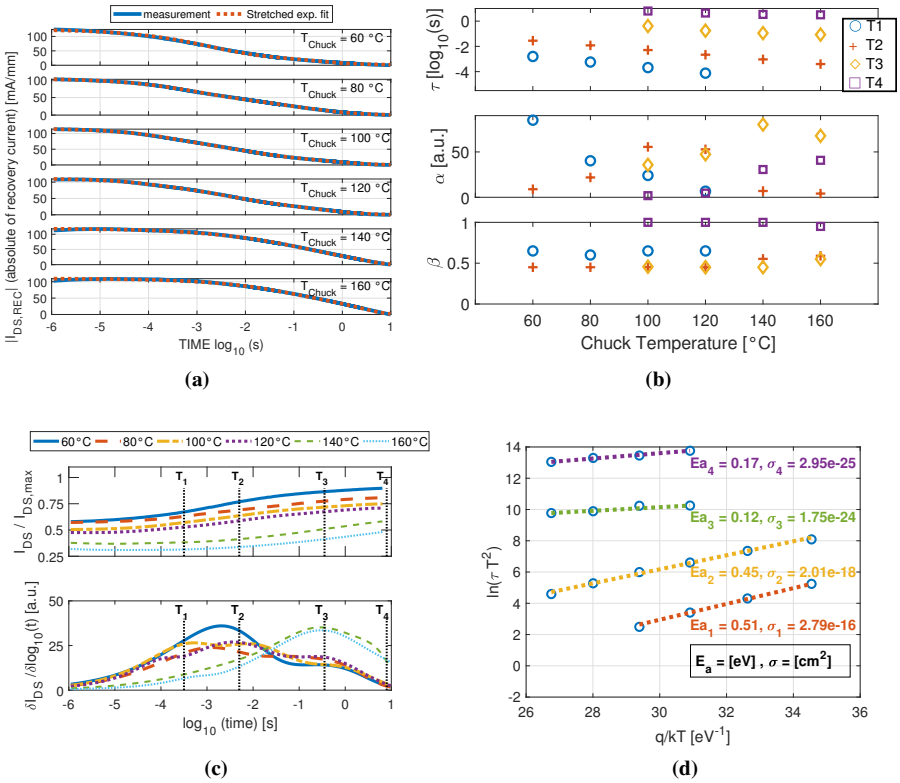


Figure 2.8: Example of trap analysis in a GaN HEMT: **(a)** Fitting of measured I_{DS} transients at multiple temperatures using stretched exponentials. **(b)** Extracted parameters α, β, and τ versus temperature. **(c)** Differential of fitted transients highlights temporal contributions from individual traps, [B]. **(d)** Arrhenius plots used to extract E_a and σ for each trap.

An example of this methodology is illustrated in Fig. 2.8a–2.8d, based on a device analyzed in Paper [B]. Four distinct transients were identified to achieve accurate fitting, satisfying the three main criteria listed above. In Fig. 2.8b, the extracted parameters α, β, and τ are shown for each temperature. The differential plot in Fig. 2.8c highlights the role of each parameter: peak height corresponds to α, peak width to β, and peak position to τ. The dashed lines mark the extracted τ values for four trap states at 100 °C. The resulting linear fits are shown in Fig. 2.8d, from which E_a and σ are extracted.

Throughout this thesis, DCTS has proven to be an effective method for identifying specific trap states and their locations within the epitaxial stack. While other electrical methods provide indirect evidence of trapping, DCTS offers direct insights into trap kinetics and distributions. Nevertheless, DCTS is rarely used in isolation; its findings are complemented by material analysis techniques such as secondary ion mass spectrometry (SIMS) [Paper A] and x-ray photoelectron spectroscopy (XPS) [Papers B and C].

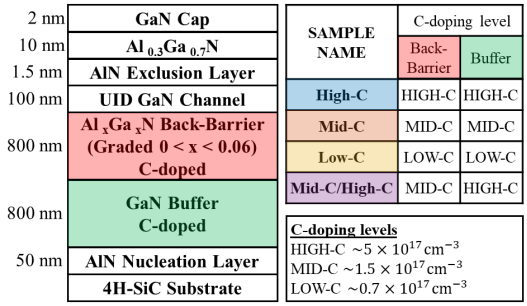
Chapter 3

Characterization of trapping effects limiting the performance of microwave GaN HEMT

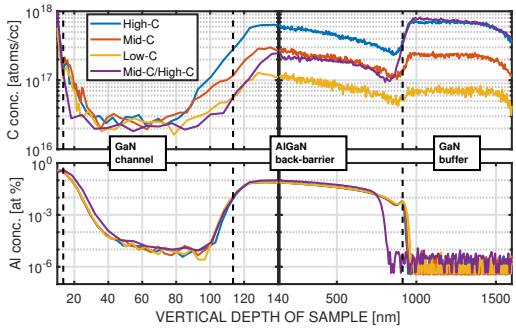
In the studies here described, the common thread is a desire to enhance device performance by curtailing trapping that presents itself in various ways. Trapping as a consequence of buffer/back-barrier and intentional doping is addressed in Paper [A], providing new insights into how epitaxial engineering can be used to control the dispersive and SCE of a GaN HEMT. In Paper [B] focus is put on how a critical processing step for defining Schottky gate contacts (in a passivation-first technology) alters device characteristics such as V_T while also impacting surface related trapping behavior. It covers a wide range of F plasma treatments for SiNx gate opening and to what extent an additional processing step of pre gate annealing may be effective in reversing the adverse impacts the F plasma treatment entails. For a GaN HEMT low-noise-optimized transistor described in Paper [D], trapping is highly aggravated at 4.2 K, especially in devices with Fe-doped buffers. In the pursuit of achieving highly reliable devices without significant current collapse, variations in field plates and designs and buffer doping are evaluated.

3.1 Carbon doping of AlGaN back-barrier

Buffer doping has been demonstrated a reduction in SCE and improved power added efficiency (PAE) but only moderate improvements in f_T and f_{max} [27] [56]. More considerable improvement in high frequency operation was seen when back-barriers were implemented. Today the back-barrier is considered as one of the key design technologies mitigating SCE and improving 2DEG confinement, enabling high frequency performance with f_T and f_{max} of 454 GHz and 444 GHz [11]. Despite its benefits in 2DEG confinement, the implementation of an AlGaN back-barrier introduces certain trade-offs. It adds thermal boundary resistance to the epitaxial stack, which hinders heat dissipation and may compromise power-added efficiency (PAE) compared to structures with C-doped GaN buffers [57]. Another challenge is the potential formation of a parasitic channel at the AlGaN/GaN buffer interface. This risk can be mitigated by grading the Al content in the back-barrier from 0% to 10%—a technique implemented



(a)



(b)

Figure 3.1: Nominal epitaxial structure and measured Al- and C-profiles for the four device splits from [Paper A]. **(a)**: The epitaxial structure is shown on the left, with each layer's thickness indicated. Through color coding, the **AlGaN back-barrier** and **GaN buffer** are clearly identified. The top-right device split table details four different splits: **High-C**, **Mid-C**, **Low-C**, and **Mid-C/High-C**. The sample color coding matches that used in the Al and C SIMS profiles to ensure consistency. **(b)**: PCOR-SIMS data of the epitaxial stack from the surface (left) down into the GaN buffer (right). Note the scale transition from linear to logarithmic at a depth of 140 nm. Overlaying the C concentration on the Al profile reveals variations in C trailing at the back-barrier/channel interface, which provides crucial insight for comparing device performance [A].

in Paper [A] and supported by previous work [58].

C doping can give rise to transients that can be as long as 10s, which has been demonstrated for C-related trapping [46], have considerable ramifications on the high frequency operation of GaN HEMTs. Depending on the occupied position in the crystal structure C can give rise to a wide range of activation energy states. As substitutional occupation in n-type GaN there is a slightly lower formation energy for C_N (deep level acceptor) occupation as opposed to C_{Ga} (shallow donor), resulting in a self-compensating characteristic with slight domination of acceptor states creating a high resistive GaN. Additional occupation sites to consider are interstitials (C_I) that can range from deep-level donors to more shallow donor states. Common reported E_a for C_N are E_V+0.35 eV and E_V +0.9eV, whereas C_I can assume a wide range of E_a from E_C – 1.35 eV, E_C – 1.2 eV, E_C – 0.578 eV. E_C – 0.49 eV down to E_C – 0.14eV [45].

The use of carbon-doped AlGaN back-barriers has been demonstrated in other device types, such as Schottky barrier diodes [59], in InAlGaN/AlN/GaN HEMTs [60] and more recently AlGaN/GaN HEMTs [46]. These studies showed that such structures exhibit similar trapping mechanism, namely C_N defects as C-doped GaN buffers.

To counteract the resulting increase in on-resistance (R_{on}) and knee voltage (V_{knee}), a bi-layered AlGaN barrier where only the lower layer is C-doped was proposed [46]. This trade-off between reducing trapping and maintaining robust 2DEG confinement is directly explored through large singal analysis in Paper [A].

The work in Paper [A] builds upon previous findings regarding the impact of channel thickness (t_{ch}) on large-signal performance [60]. That study concluded that a channel thickness of 100 nm overall yielded the highest output power (P_{out}) across a range of gate lengths (L_g) from 50 to 200 nm. However, an important factor not fully explored in [60] was the role of carbon (C) doping in the buffer, especially in structures incorporating a C-doped AlGaN back-barrier to confine the two-dimensional electron gas (2DEG). Paper [A] addresses this by retaining the 100 nm t_{ch} and introducing three distinct carbon doping concentrations, overlapping the reference value of $3 \cdot 10^{17}$ cm^{-3} used previously.

3.1.1 Back-barrier C doping: trade-offs in dispersive and SCEs

The purpose of the study in Paper [A] was to systematically evaluate how varying levels of carbon doping in an AlGaN back-barrier impact large-signal performance, particularly by addressing the relative contributions of SCE and trap-induced dispersion. This study aims to identify an optimal balance where neither SCE nor trapping effects dominate, thereby maximizing power-added efficiency (PAE) and output power (P_{out}).

Three doping levels were chosen Fig. 3.1a, including a mid-range reference value of $3 \cdot 10^{17}$ cm^{-3}, to span the range of interest for large-signal performance. Devices were characterized using pulsed I–V, S-parameter, and load-pull measurements to extract metrics such as gate lag, current collapse, and large-signal RF performance.

Secondary ion mass spectroscopy

Through ion bombardment in vacuum condition, sputtering of ions stemming from the sample i.e. secondary ions, can be identified and quantified with respect to their mass and charge. By simultaneously linking the composition of secondary ions to how deep the sample is etched, a compositional map can be established with respect to vertical depth.

In paper [A] Point-By-Point corrected (PCOR)-SIMS from EAG Laboratories was used, which is a SIMS technique specifically well adapted for layer-by-layer quantification in complex epitaxial stacks. Depending on element the detection limit ranges from ca $10^{17} cm^{-3}$ for detecting N and C atoms down to ca $10^{14} cm^{-3}$ for Fe, this in combination with a vertical resolution of ca 1-5 nm makes PCOR-SIMS a highly suitable method for analyzing AlGaN/GaN heterostructures [61]. The nominal epitaxial design, Fig. 3.1a, was insufficient in explaining why the characteristics of sample MID-C/High-C deviated from the MID-C/MID-C An important part of the inter device analysis was enabled by linking the Al-profile to the C-profile, Fig. 3.1b

3.1.2 Trap Manifestation

Most trap measurement techniques described in Chapter 2.6 were utilized in Papers [A]. Here the consequences of trapping and SCE on device performance is discussed. Going from DC and PIV measurements where very specific conditions may reveal either

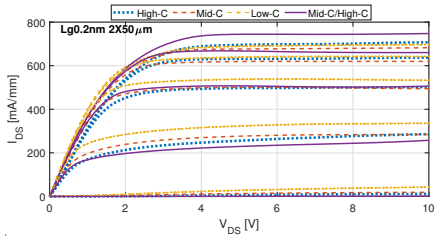


Figure 3.2: Output characteristics for a V_{DS} = 0:0.1:10 V sweep, while stepping V_{GS} = -3:1:1 V [A].

TABLE 3.1: DC CHARACTERIZATION RESULT [A]

WAFER	Ron	L_g = 200 nm (100 nm)		
		SS @2.1 V	SS @20.1 V	DIBL
	[Ω·mm]	[mV/dec.]	[mV/dec.]	[mV/V]
High-C	3.5	66 (72)	78 (87)	2.0 (2.8)
Mid-C	2.9	68 (75)	77 (93)	5.4 (5.3)
Low-C	2.0	69 (76)	92 (102)	8.1 (14)
Mid-C/High-C	2.2	71 (74)	81 (96)	5.9 (11)

effect, large signal analysis, gives the indication of which phenomenon dominates the device performance for each device split.

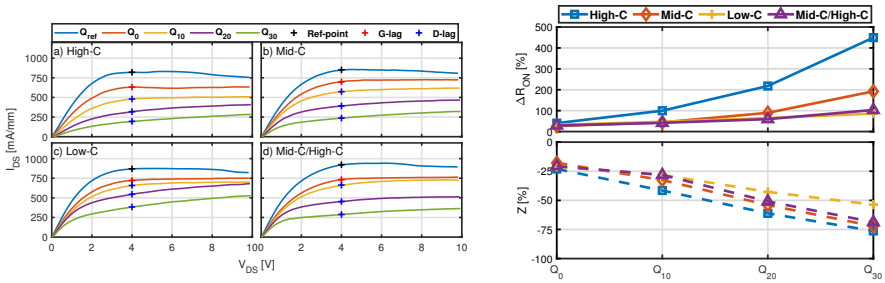
DC

In the case of carbon-doped back-barriers paper [A], the effect of traps is most clearly seen through field-dependent modulation of device electrostatics. Heavier doping enhances 2DEG confinement, leading to improved subthreshold swing (SS) and lower drain-induced barrier lowering (DIBL). However, this improvement comes at the cost of increased back-gating effects reducing the n_s, visible in DC as elevated R_{ON}, TABLE 3.1. Note that this effect is less apparent at high fields, possibly due to the saturation current being more dependent on v_s. Furthermore, the trapped electrons inducing back-gating may at elevated channel temperatures, be released, counteracting the reduced mobility due to self-heating, which is manifested as $g_{ds} > 0$, which is how HIGH-C behaves at high V_{DS} Fig. 3.2. These changes reflect the dynamical filling/de-trapping of deep-level traps in the back-barrier under strong electric fields, which in turn may screen the gate potential and degrade the channel control.

Pulsed-IV

In Paper [A], gate lag was largely unaffected by the level of carbon doping. This suggests that surface-related trapping remained consistent across all device splits, as expected given the identical top-barrier design. However, as the quiescent drain voltage (V_{dsq}) increased, progressive activation of carbon-related traps was observed. At this point, the nominal epitaxial design (Fig. 3.1a), no longer provided a sufficient basis for inter-device comparison. Instead, meaningful interpretation of device behavior subject to electric fields extending down to the back-barrier, required analysis of the actual C concentration profiles, obtained through secondary ion mass spectrometry (SIMS), Fig. 3.1b.

At $V_{\mathrm{dsq}} = 10$ V i.e. Q_{10}, initial signs of current collapse and increased dynamic R_{ON} suggested activation of traps near the channel/back-barrier interface. When V_{dsq} was raised to 20 and 30 V i.e. Q_{20} and Q_{30}, the collapse became more pronounced, consistent with C-trap activation within the back-barrier. Importantly, the Mid-C/High-C split behaved similarly to the Low-C device at Q_{10}, but more like the Mid-C device at Q_{20} and Q_{30}, in line with the SIMS profile shown in Fig. 3.1b. Furthermore, at Q_{30}, the Mid-C/High-C devices exhibited no additional collapse relative to the Mid-C devices, indicating that buffer-related traps remained inactive under these field conditions.



(a) **(b)**

Figure 3.3: The measured PIV characteristics of devices with varying back-barrier and buffer C doping, Paper[A]. a) the output characteristics at V_{gs} = 2 V, for quiescent biases ranging from reference $(V_{gs,q}, V_{ds,q}) = (0,0)V$, to gate-lag Q_0 and drain-lag measurements Q_{10}, Q_{20} and Q_{30}, with crosses marking where the current collapse (Z) was extracted (V_{ds} = 4 V. b) the ΔR_{ON} and Z is visualized, the differences seen between the four devices directly reflects activation of C traps in the channel/back-barrier region [A].

This confirms that the back-barrier effectively shields the device from buffer-related trapping up to at least 30 V.

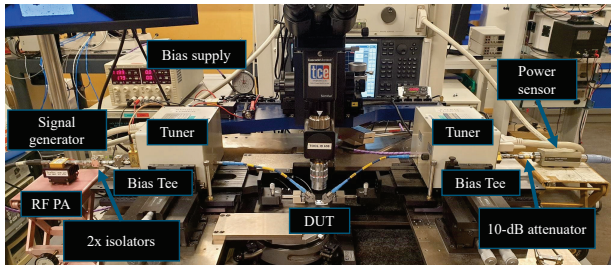
Small-Signal Measurements

Small-signal S-parameters were measured up to 145 GHz on six 2 × 50 µm, L_g = 100 nm devices per wafer. The gate bias V_{GS} was swept from –3.5 V to +1 V in 0.5 V steps, and the drain bias V_{DS} from 0 V to 20 V in 0.5 V steps. All devices exhibited similar peak extrinsic f_T of 56–58 GHz at (V_{GS}, V_{DS}) = (–1.5 V, 4.5 V) and peak $f_{\max}$ of 66–68 GHz at (–1.5 V, 10 V). This uniformity at low fields ($V_{DS} \leq 10$ V) indicates that C-related trapping does not significantly impact the small-signal response under these bias conditions.

At higher fields ($V_{DS} = 20$ V), a stronger reduction in $f_{\max}$ was observed for the High-C devices (–21%) compared to Low-C (–13%), consistent with increased trap activation in the back-barrier and channel regions. While higher C-doping improved 2DEG confinement and reduced g_{ds}, this did not translate into higher $f_{\max}$, since dispersion effects, rather than short-channel effects, dominated performance degradation at high drain bias [60]. These results align with the PIV observations, where C-related trapping became significant for $V_{DS} > 10$ V, and reinforce the conclusion that dispersion is the primary high-field limitation in the studied L_g = 100 nm devices.

Large-Signal Measurements

Load-pull measurements in [Paper A] were conducted to evaluate the manifestation of SCE and dispersion under realistic power amplifier (PA) operating conditions. This necessitated a dedicated measurement setup, Fig. 3.4a, which is schematically described in Fig. 3.4b. On the input side, a signal generator provides the input signal frequency. This signal is amplified by the driver amplifier (RF PA), increasing the input power level. The subsequent two isolators protect the RF PA from any undesired reflections from the tuner. Symmetrically around the DUT tuners are used to present controlled source and load impedances, additionally Bias tees are used to superimpose DC bias onto the RF signal path going to the DUT while preventing RF leakage into



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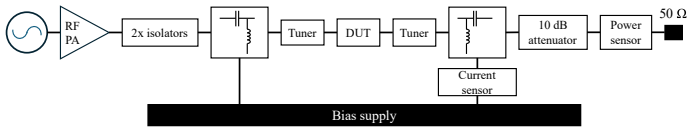


(b)

Figure 3.4: HEMT cross-section and layout, (a): typical epitaxial layer stack used in this thesis, note the layer below the GaN channel layer varies between studies. **(b)**: optical top-view image with labels showing source,drain, gate contacts and device width.

the DC supplies. On the RF output side, a 10 dB attenuator is placed before the next-in-line power sensor to prevent overload and ensure linear response. A current sensor on the drain supply line is used to monitor the DC operating point and verify class of operation. In pure class A operation P_{out} and linearity is maximized, whereas class B achieves higher efficiency. By biasing in between these optima, class AB allows for favorable large-signal trade-offs. In [Paper A] the aimed amplifier operation mode was class AB (with output current of roughly 15 – 20 % of the I_{DSS}) providing a compromise between linearity and efficiency. The load reflection co-efficient Γ_L was optimized for maximum output power P_{out}, at each bias condition, with subsequent power sweeps conducted until reaching 5 dB gain compression, i.e. sufficiently deep to capture peak power-added efficiency (PAE), typically located near 3 dB compression for GaN HEMTs [62] [63].

Three systematic limitations in the measurement setup likely contributed to an underestimation of both PAE and P_{out}. However, since these limitations were consistent across all device splits, they did not compromise the validity of the comparative analysis. Nevertheless, they do constrain comparisons with results from other studies.

The first limitation was the use of a single power sensor, placed at the output. This meant that reflected input power could not be measured, and PAE had to be calculated assuming perfect source matching, that is, $P_{\text{in}} = P_{\text{avs}}$. Under large-signal conditions, where impedance mismatches can arise due to dynamic loading, this assumption leads to a systematic underestimation of the actual PAE.

The second limitation, was the load-pull system employed passive tuners with a maximum achievable load reflection coefficient of approximately 0.73. This restriction, particularly significant at 30 GHz, limited the ability to present the ideal load impedance (Γ_{opt}), thereby reducing the measured peak large-signal performance of the DUT. To mitigate this limitation, measurements focused on wider gate-width HEMTs (2 × 100 µm), which can deliver higher output current and thus present a lower output impedance. This brings Γ_{opt} closer to 50 Ω, making load matching more straightforward. Concerning the L_g devices with 200 nm were chosen (to further

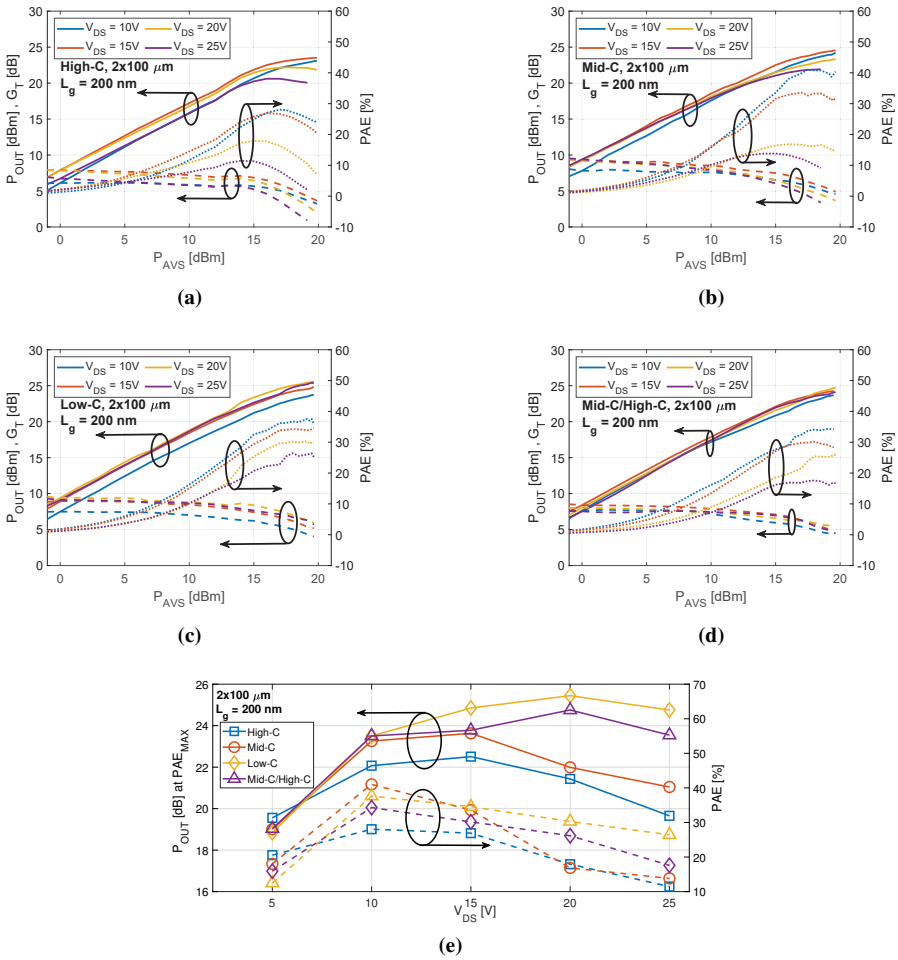


Figure 3.5: Transducer gain, output power and power added efficiency (G_T, P_{out} and PAE) for V_{DS} bias ranges 10-25 V for all C-doped back-barrier device splits (a): High-C. **(b)**: Mid-C. **(c)**: Low-C. **(d)**: Mid-C/High-C. **(e)**: All splits summarized, showing PAE_{max} and P_{out} at PAE_{max}, (P_{PAE}) [A].

simplify load impedance matching), also led to less SCE, (as opposed to measuring on L_g of 100 nm devices). Therefore, the likelihood of dispersion effects having a more prevalent performance-limiting effect at high drain bias increased.

A third limitation was the early compression of the driver amplifier, which in some cases restricted the available input power before the DUT reached its maximum output power or the by measurement protocol set 5 dB gain compression. This input-side constraint is distinct from the limited Γ_L range of the passive tuner but for certain load conditions, full DUT compression may require higher drive levels than the driver could deliver, making it a secondary bottleneck. This was especially noticeable for the devices with lower C content i.e. less susceptible to soft compression [6], see Low-C showing compression < 4dB Fig.3.5c, whereas Fig.3.5a reached close to 5dB compression for the same available input power level.

The detrimental impact of both dispersion and short-channel effects (SCE) on RF

performance is discussed in [60], providing the background to comprehend the results here presented. In [Paper A], the chosen figure of merit was the output power at peak PAE, P_{PAE}, rather than the absolute maximum output power, $P_{\mathrm{out,max}}$. This approach was chosen partly because it better reflects performance under realistic conditions, where high efficiency is as important as high output power, but also as a consequence of the above listed limitations making $P_{out,max}$ unattainable since it for many devices occurred at input power levels beyond the 20 dBm limit of the available signal source.

Just as in the case of PIV Fig. 3.3b, the lower V_{ds} biases of 5 and 10 V showed little trap-activation, with all but High-C behaving similarly. However for higher V_{ds} bias, PAE starts to decrease and the P_{PAE} starts to scale poorly. Notably, Mid-C/High-C, diverges from Mid-C and scales similarly as Low-C up to V_{ds} = 20 V, a further indication of how impactful the C-profile at the channel/back-barrier interface is on device performance Fig. 3.1b. Since dispersion was dominating over SCE for the L_g = 200 nm devices throughout the whole study split the highest P_{PAE} was obtained for the Low-C devices at V_{ds} = 20 V. Maintaining a consistently higher PAE for V_{ds} of 15 V and above.

3.1.3 Trap Analysis

Having established a correlation between C-doping profiles in the back-barrier and variations in trapping behavior, the next step is to demonstrate causality. This was achieved through Drain Current Transient Spectroscopy (DCTS).

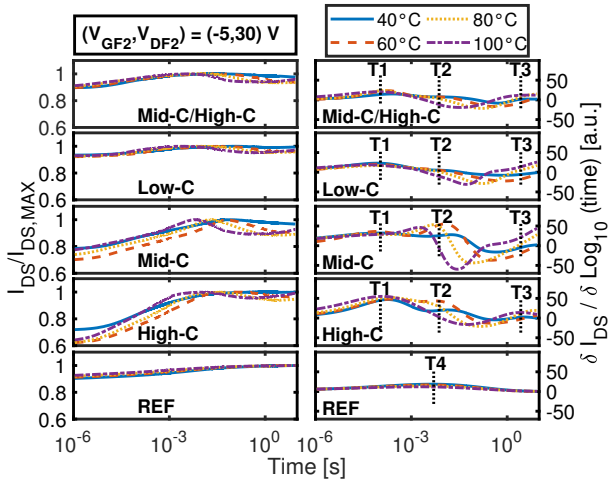
Drain Current Transient Spectroscopy

To support the DCTS measurements, a reference sample was introduced, featuring the same top barrier epitaxial structure but without a back-barrier and without intentional buffer doping. While all C-doped back-barrier samples revealed three distinct trap states, T_1, T_2, and T_3, the reference device exhibited only a single trap state, T_4. This trap showed minimal shift in time constant (τ) for a variation in (T_{chuck}), yielding an activation energy E_a of 0.12 eV and a highly stretched transient ($\beta \approx 0.2$). These characteristics suggest a de-trapping mechanism that is weakly thermally activated and likely governed by tunneling or hopping processes. The origin of T_4 is likely surface-related, associated with nitrogen vacancies or residual impurities such as carbon or hydrogen [64–66].

Given the similar epitaxial design, it is likely that T_4 is also present in the C-doped samples. However, its low α and low β results in a weak signature, which also overlaps with T_2. This makes its distinct identification challenging in those devices.

Importantly, the absence of T_1, T_2, and T_3 in the reference sample indicates that these trap states originate either directly or indirectly from carbon doping and/or the presence of the back-barrier. PIV and large-signal measurements further confirmed that all devices exhibit similar performance at low drain bias ($V_{ds} \leq 10$ V), but substantial trapping effects emerge at higher V_{ds} (> 20 V). Therefore, DCTS was performed at $V_{DF} = 10$ V and V_{DF} = 30 V, to capture the differences in trap activation at low and high electric fields.

At V_{DF} = 30 V, all three trap states, T_1, T_2, and T_3, were detected Fig. 3.6a. At V_{DF} = 10 V, only T_3 was observed. Moreover, the α parameters for T_1 and T_2 increased with carbon content, indicating stronger de-trapping behavior, and pointing to a direct link between these traps and C-related defects.



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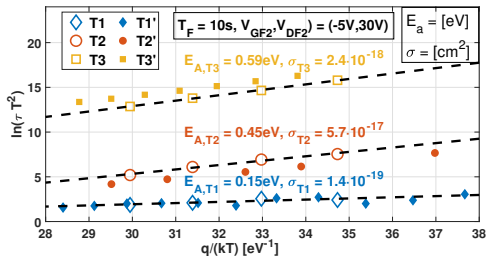
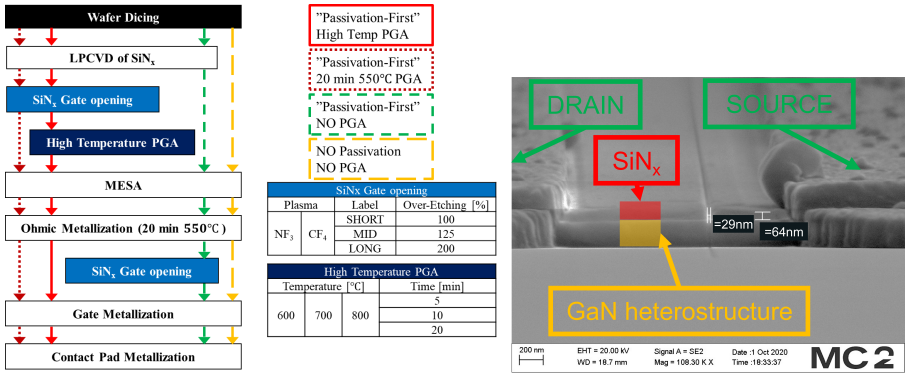


(b)

Figure 3.6: DCTS results for the C-doped back-barrier samples [A]. (a): To the left, normalized I_{ds} transients for filling bias (V_{GF}, V_{DF}) = (-5, 30) V and on-state bias $(V_{G,ON}, V_{D,ON})$ = (1, 6) V, shown for a T_{chuck} between 40°C and 100°C. To the right, the corresponding differential plots are depicted, with all four detected trap states τ value $\sim$ 80°C marked with striped lines. **(b)**: Arrhenius plot for trap states T_1, T_2, and T_3 showing extracted E_a and capture cross-section σ. Literature values for corresponding trap states T_1' [67], T_2' [68], and T_3' [59] are also shown, revealing good agreement.

T_1 and T_2 thus appear to originate from carbon-induced trap states located within the back-barrier. In contrast, while T_3 is also related to C-doping and/or the back-barrier, its activation is relatively independent of carbon concentration. Its spatial origin is likely the surface or channel region. Similar to Fe-induced indirect trapping effects reported in literature [69], T_3 may result from dislocations propagated during the growth of C-doped AlGaN layers. The rather low β is in line with the trap state being associated with structural defects. These dislocations could act as trap centers in the channel region, with a density insensitive to the carbon doping levels investigated in [Paper A] [59].

The activation energies and capture cross-sections extracted from Arrhenius plots align well with literature-reported values for similar traps, providing strong support for the proposed trap origins Fig. 3.6b.



(a) **(b)**

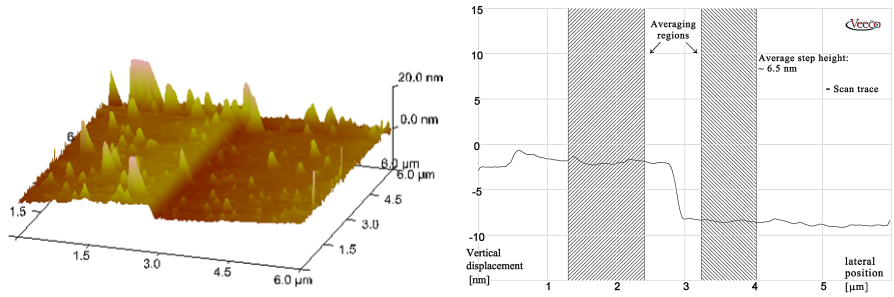
Figure 3.7: (a): the HEMT processing chronology and processing variations for all devices used in Paper [B] and [D]. F plasma was split in chemistry (CF_4 or NF_3) and degree of SiN_x over-etching. The high temp pre-gate annealing was either (600, 700 or 800°C) time ranging from 5, 10, or 20 min. The devices without passivation serve as reference devices [B]. **(b)**: a SEM side-view showing an example of the gate opening of a SiN_x passivation, enabling a L_g of 30 nm.

3.2 Fluorine plasma gate opening and device recovery

The effects of fluorine-based plasma treatments on GaN HEMTs are well-documented, particularly their use in shifting the threshold voltage (V_T) by incorporating fluorine ions (F^-) into the AlGaN barrier, which compensates polarization charges and suppresses 2DEG formation [70, 71]. While this approach facilitates the realization of enhancement-mode (E-mode) transistors, it often comes at the cost of degraded drain current, output power, and efficiency. For high-performance RF applications such as RADAR, Satcom, and 5G systems, depletion-mode (D-mode) GaN HEMTs remain the preferred choice due to their intrinsic ability to form a high-density 2DEG without gate bias, supporting high power density, excellent high-frequency performance, and robustness under thermal and electrical stress [72].

For all GaN HEMTs with Schottky gate contacts, fluorine plasma based on CF_4, NF_3, or SF_6 are used to over-etch SiN_x for gate opening [52, 70, 73]. As a result, the GaN cap surface is subjected to F^- implantation, potential etching, and structural degradation. The implanted F^- ions form acceptor states in GaN and AlGaN that contribute to positive V_T shifts. Although studies indicate that these F states are thermally instable and can be partially inactivated through annealing, effective F^- out-diffusion typically requires annealing at ~800°C [74], whereas conventional processes are limited to 550°C due to the risk of Schottky contact degradation [75]. Thus, a study into the optimal annealing strategy (encompassing high temperature annealing up to ~800°C) for preserving D-mode HEMT performance needed exploration.

Furthermore, the literature contains conflicting reports regarding the etching of the barrier layer by CF_4 plasma [76] [70] [77], making the potential for full V_T recovery uncertain. For NF_3 plasma, no etching of GaN has to the authors' knowledge been reported. Therefore, a comparative study of NF_3 and CF_4 plasma effects, combined with high-temperature annealing, is warranted. In this work, pre-gate annealing up to 800°C was enabled through a passivation-first process.



(a) **(b)**

Figure 3.8: AFM measurements of a sample exposed to CF_4 plasma **(a)**: a 3D plot portraying a $6 \cdot 6\ \mu m^2$ scan area, the left region was mask protected, while the right was exposed to the CF_4 plasma. **(b)**: line profile taken perpendicular to the step edge, showing an average height difference of approximately 6.5 nm between the masked and exposed regions.

3.2.1 High temperature pre-gate annealing for device recovery

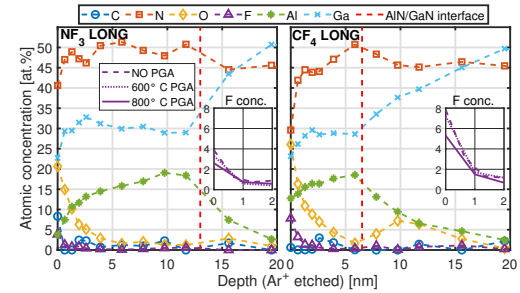
To address the concerns and knowledge gaps addressed above, Paper [B] contained a unprecedented wide variety of splits on F plasma and annealing treatments Fig.3.7a. This study utilizes the potential for high pre-gate annealing enabled by passivation first technology through low pressure chemical vapor deposition (LPCVD). By chronologically placing the gate opening process directly after the passivation step, the annealing treatment can be designed without any concern for metal contact deterioration.

Since reversibility was the central theme of the study, any irreversible impacts from the F plasma needed to be investigated. In that category the potential etching of the top barrier was of high interest, therefore, all F plasma exposed samples were analyzed in atomic force microscopy (AFM), Fig. 3.8a. The electrical evaluation of how well annealing promoted device recovery after F plasma exposure, was primarily done using DC measurements of V_T. This metric was explicitly chosen due to a desire of maintaining D-mode operation.

By combining DC and PIV measurements, the study was designed to provide guidance in how the optimal pre-gate annealing treatment leads to improved DC performance while curtailing drain- and gate-lag effects. Additionally, the study strives to fully categorize the present trap states for all F plasma and annealing treatments, thereby incorporating a DCTS and XPS analysis. Revealing thermal activation of O-related and deactivation of F-related acceptor states, providing means to correlate these two trap states to DC and pulsed-IV characteristics.

Atomic Force Microscopy

To establish certainty on whether F plasma etches GaN and/or AlGaN and if so, how dependent the etching is of F plasma chemistry and etch time, AFM was used. Test chips were exposed to both F plasma chemistries with varying exposure times corresponding to the over-etching recipes described in Fig. 3.7a, In case the exposed material was etched, a step height towards an unexposed region could be detected. As demonstrated in Fig. 3.8a, CF_4 plasma does indeed etch both GaN and AlGaN. The CF_4 LONG (200 % over-etching) led to 6.5 nm barrier etchingrecipe led to 6.5 nm, Fig. 3.8b. This was not seen for NF_3 plasma. Even when taking into account the



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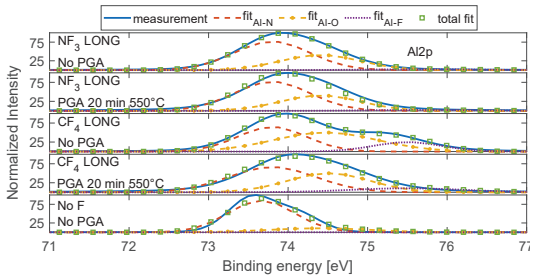


(b)

Figure 3.9: For both F plasma chemistries and a range of annealing temperatures, XPS analysis was performed [B]. (a) Ar^+ milling between measurements enabled compositional analysis. The left figure shows NF_3-treated devices, and the right figure shows CF_4-treated devices (without pre-gate annealing). The inset plots the F concentration as a function of pre-gate annealing temperature. **(b)** Al 2p binding energies at the sample surface for five different samples. The bottom spectrum corresponds to a GaN cap unexposed to F plasma, whereas the four spectra above reflect varying plasma chemistries and annealing treatments.

impact of the RF power level and the related DC self-bias, the difference in propensity to etch GaN remained. The CF_4 plasma etch rate was found to be 0.03 nm/s for the standard recipe.

Since top barrier etching irreversibly causes a reduced n_s and thereby shifts V_T positively, any degree of CF_4 plasma over-etching is sure to compromise the D-mode operation. Hence, an early indication that NF_3 plasma has less adverse impacts on D-mode device performance compared to CF_4 plasma.

X-ray Photoelectron Spectroscopy

Beyond potential barrier etching, fluorine-based plasma treatments strongly influence the surface chemistry of AlGaN/GaN structures. To investigate the incorporation of fluorine and potential surface chemistry changes stemming from plasma exposure and subsequent pre-gate annealing, X-ray Photoelectron Spectroscopy (XPS) was employed. XPS is particularly well-suited for this purpose due to its surface sensitivity of 5–10 nm and its ability to distinguish chemical bonding states. Measurements were carried out using a PHI5000 VersaProbe III – Scanning XPS Microprobe, equipped with a monochromatic AlK α X-ray source (photon energy of 1486.6 eV), offering a spectral resolution of approximately 0.6 eV [78]. This resolution is sufficient to resolve chemical state shifts in the Al2p core level, such as Al–N (73.5 eV), Al–O (74.7 eV),

and Al–F (75.6 eV) [79] [80], allowing for identification of oxidation and fluorination phenomena induced by plasma processing. To complement surface analysis, Ar^+ ion sputtering was used between scans to obtain depth-resolved compositional profiles. These are shown in Fig. 3.9a for the case of LONG over-etch exposure. Notably, the barrier thickness is only ∼6 nm thick due to the barrier thinning following the CF_4 plasma exposure.

In terms of surface composition, XPS revealed that both CF_4 and NF_3 plasma treatments led to elevated levels of fluorine and oxygen at the surface. However, the changes were substantially more pronounced for CF_4 exposure. Specifically, CF_4-treated samples exhibited surface fluorine concentrations of approximately 8 at.%, compared to around 4 at.% for NF_3-treated samples. Similarly, oxygen concentrations reached 24–26 at.% for CF_4, whereas NF_3 exposure resulted in a lower range of 16–21 at.%. These results indicate a stronger tendency for CF_4 to both fluorinate and oxidize the surface. After annealing at 800 °C, the fluorine concentration in CF_4-treated samples decreased to roughly 5 at.%, while the oxygen content remained largely unchanged, highlighting the thermal instability of surface-bound fluorine species and the persistence of oxidation effects.

Importantly, chemical state analysis via the Al2p spectrum showed that plasma treatments induced significant Al–O bond formation, which was largely absent in reference (untreated) samples Fig. 3.9b. This indicates that plasma exposure renders the GaN/AlGaN surface more prone to oxidation. Moreover, Al–F bonding associated with the formation of AlF_3 was observed exclusively in CF_4 treated samples. The AlF_3 signal diminished after annealing ≥550°C, confirming its thermal instability. In contrast, NF_3 treated samples exhibited no detectable Al–F bonding and less nitrogen depletion, suggesting a more chemically benign interaction with the surface. These spectroscopic insights confirm a plasma chemistry dependent incorporation of F and O species, and demonstrate how annealing can partially reverse the fluorine incorporation effects while failing to reduce oxygen-related species.

It is worth noting that while XPS provides valuable bonding and depth-resolved information, its detection limit (10^{19}–10^{20} cm^{-3}) is higher than that of Secondary Ion Mass Spectroscopy (SIMS), which can resolve concentrations as low as $\sim 10^{16}$ cm^{-3}. Nonetheless, the observed shallow fluorine profiles are consistent with previously published SIMS results for similar treatments [81].

3.2.2 Trap manifestation

In [Paper B] traps showed thermal activation/de-activation, with a wide range of temperatures investigated, all from no pre-gate annealing, up to 800 °C annealing, the thermal instabilities of the trap states involved as a consequence of F plasma treatment could be investigated.

DC – Characterization

Among the various DC parameters, the threshold voltage (V_T) served as the most direct and sensitive metric for quantifying the impact of fluorine plasma exposure and subsequent pre-gate annealing. Primarily, V_T was tracked to monitor how well depletion-mode (D-mode) operation was preserved. In AlGaN/GaN HEMTs, fluorine readily forms negatively charged acceptor states, particularly within the gated region, resulting in a positive shift in V_T. These fluorine-related traps act as fixed negative

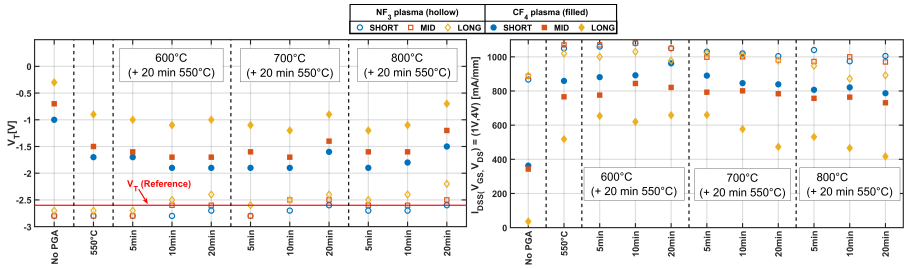


Figure 3.10: Summary of DC characteristics with NF_3 plasma exposed devices in hollow markers, CF_4 plasma in filled markers: To the left, (V_T) extracted at maximum $R_{DS}(V_{GS})$ with $V_{DS} = 50\,mV$. The red line indicates the V_T of the reference device without fluorine plasma exposure. To the right, $I_{DSS}(1,4)V$. The x-axis categorizes devices by pre-gate annealing treatments. Black-striped vertical dividers separate annealing temperature groups [B].

charges with long de-trapping times (>∼10 s at room temperature), making V_T a reliable indicator of their electrical influence.

The V_T was extracted using a *maximum resistance method*:

$$V_T = V_{gs}\big|_{\max\left(R_{ds}(V_{gs})\right)} \tag{3.1}$$

where R_{ds} is calculated as V_{ds}/I_{ds} at a low drain-source voltage of $V_{ds} = 50\,mV$. This method captures the gate voltage at which the device transitions between off and on states.

Pre-gate annealing demonstrated partial recovery of V_T, affirming the thermal instability of the F-related acceptor states [82]. However, in CF_4 plasma-exposed devices, complete recovery to the reference V_T of $-2.7\,V$ was not achievable. This limitation is attributed to irreversible barrier thinning caused by plasma etching. The contribution of this thinning to the V_T shift (denoted ΔV_T,etch) correlates quantitatively with measured etch depths and follows the relation ΔV_T,etch $= qn_s t_e/\varepsilon_{AlGaN}$, where t_e is the barrier thickness removed. Furthermore, while both NF_3 and CF_4 plasma introduce F implantation, the magnitude of V_T shift and the extent of recovery upon annealing are plasma chemistry dependent. NF_3-treated devices exhibit no significant V_T shifting and superior recovery, mostly due to crystal structure regeneration which was achieved through annealing at 550°C , whereas CF_4-treated devices show more severe V_T shift towards E-mode and only partial reversibility. Moderate annealing (550–600°C) led to a partial recovery of V_T, consistent with the thermal deactivation of fluorine-related acceptor states [82]. However, at higher annealing temperatures ($\geq$ 700°C), a reversal of this trend was observed: V_T increased again despite continued reduction in fluorine content, as confirmed by XPS Fig. 3.9a. This positive V_T shift suggests the emergence of a new electrically active trap, likely induced by high-temperature annealing. The nature and origin of this trap will be explored in detail in the DCTS section.

In addition to V_T, other DC parameters such as the saturation current (I_{DSS}) Fig. 3.10, maximum transconductance ($g_{m,max}$), and on-resistance (R_{on}) were also evaluated to assess the impact of fluorine plasma exposure and pre-gate annealing. The trends in $g_{m,max}$, R_{on} and I_{DSS} were found to be primarily governed by the recovery of the crystal structure in the gated region. Once pre-gate annealing at 550°C was performed, the damage caused by plasma exposure was largely mitigated, leading to a significant improvement in these parameters. Beyond this annealing temperature,

no significant improvement in either $g_{m,\max}$ or R_{on} could be observed, regardless of plasma chemistry or degree of over-etching.

In contrast, I_{DSS} continued to evolve in close correspondence with the V_T shift. As the depletion-mode (D-mode) operation was partially restored through annealing, I_{DSS} increased, reflecting the progressive recovery of channel charge. NF_3-treated devices followed the V_T trend closely and reached higher $I_{\text{DSS}}(1,4)V$ values compared to CF_4-treated devices Fig. 3.10, which could not sustain the same gate-overdrive due to barrier thinning and the resulting increase in forward gate current.

Pulsed-IV

Pulsed-IV (PIV) measurements complement the DC analysis by revealing transient effects such as dynamic on-resistance (R_{ON}), drain-lag, and gate-lag. These measurements highlight how pre-gate annealing influences short-timescale carrier dynamics and charge trapping behavior.

Devices subjected to moderate annealing temperatures—550 °C for NF_3 and 600 °C for CF_4—exhibited marked improvements in all transient metrics. Specifically, a reduction in dynamic R_{ON} of at least 12%, along with lower drain- and gate-lag, was consistently observed (Fig. 3.11a). This improvement is attributed to the thermal deactivation of fluorine-induced traps in the gated region, reducing the overall trap density and mitigating current collapse under switching conditions.

However, annealing at temperatures above 600 °C introduced a clear degradation in transient performance across all devices. Dynamic R_{ON}, drain-lag, and gate-lag all increased, indicating the presence of additional trap states that negatively affect carrier transport. This degradation was particularly pronounced in devices subjected to LONG plasma over-etching, suggesting that the plasma-induced damage played a role in enabling or amplifying the observed effects (Fig. 3.11b).

The onset of lag behavior at higher annealing temperatures, and its stronger expression in devices with more extensive fluorine plasma exposure, points to the formation of a new, thermally activated trap state. Moreover, the progressive degradation of dynamic R_{ON}, suggests that this trap diffuses into the access regions beyond the gated area during high-temperature annealing [52].

Therefore, optimal annealing conditions, 550 °C for NF_3 and 600 °C for CF_4, strike the best balance between reducing fluorine-related traps and avoiding the emergence and diffusion of additional trap states. The nature and behavior of these newly formed states will be explored in the subsequent DCTS analysis.

3.2.3 Trap Analysis

A central question at this stage is the origin of the positive V_T shifts and the degraded gate- and drain-lag performance observed after pre-gate annealing above 600 °C. These effects appear consistently in all devices irrespective of the F plasma chemistry, suggesting a thermally activated mechanism. As previously indicated, the most plausible explanation is the emergence of a trap state that becomes electrically active only at elevated temperatures. Supported by data from XPS, DCTS was utilized to pin-point the origin of this trap-state.

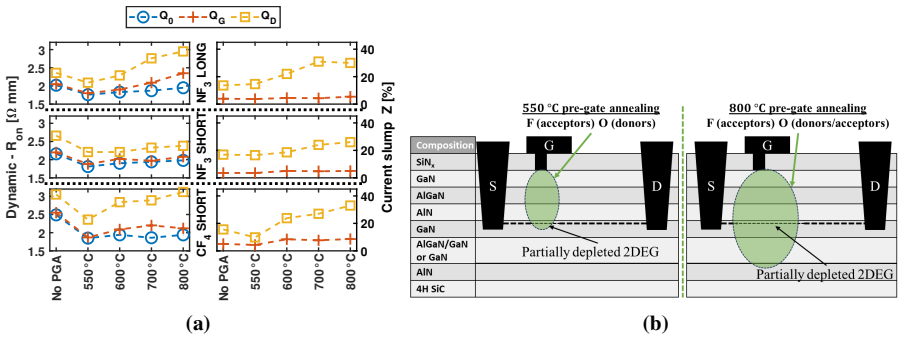


Figure 3.11: Summary of PIV characteristics: (a): dynamic R_{ON}, gate-lag and drain-lag as a function of pre-gate annealing temperature [B]. **(b)**: Illustration of the impact of oxygen-related trap diffusion at 800 °C annealing, where the increased trapping volume beyond the gated region degrades transient performance .

Drain Current Transient Spectroscopy

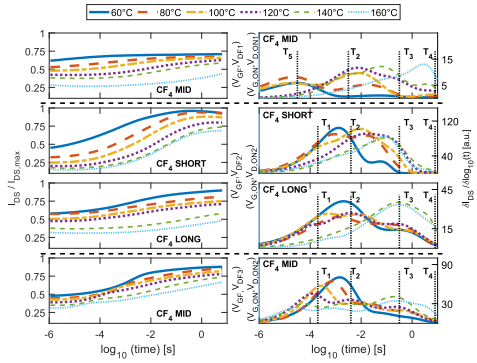
Drain Current Transient Spectroscopy (DCTS) provides insight into electrically active trap states already present in the epitaxial structure, including the ones introduced by fluorine-based plasma etching and modified by subsequent pre-gate annealing. By capturing the transient drain current response following various trap-filling biases, DCTS enables the extraction of activation energies (E_a) and capture cross-sections (σ) of individual trap states via Arrhenius analysis. A total of six trap states (T_1–T_6) were identified, each contributing differently to the dynamic characteristics of the HEMTs.

Trap Overview:

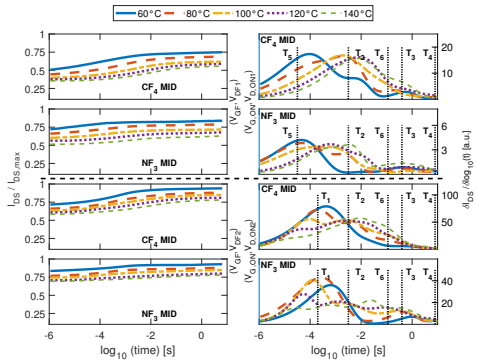
- T_1: Fe-induced acceptor, in the buffer ($E_a \approx 0.51$–0.54 eV, $\sigma \sim 10^{-15}$ cm^2).
- T_2: Oxygen-related donor (O_N) ($E_a \approx 0.43$–0.45 eV, $\sigma \sim 10^{-18}$ cm^2).
- T_3: Nitrogen vacancy (V_N) donor ($E_a \approx 0.09$–0.12 eV, $\sigma \sim 10^{-23}$ cm^2).
- T_4: Shallow fluorine-related acceptor ($E_a \approx 0.17$–0.20 eV, $\sigma \sim 10^{-24}$ cm^2).
- T_5: Dislocation-related acceptor ($E_a \approx 0.23$–0.25 eV, $\sigma \sim 10^{-17}$ cm^2).
- T_6: Oxygen-related DX-like acceptor trap ($E_a \approx 0.59$–0.62 eV, $\sigma \sim 10^{-17}$ cm^2).

These trap states were identified by combining measurements from three complementary filling/on-state bias configurations, each targeting traps in different spatial regions of the device while minimizing self-heating and unwanted re-trapping during the readout:

- **Low V_{DS} filling:** $(V_{GF}, V_{DF1}) = (V_T - 4, 0.5)$ V with $(V_{G,ON}, V_{D,ON1}) = (1, 0.5)$ V. Fills primarily shallow traps near the gate edge or in the upper barrier. The low on-state V_{DS} minimizes channel heating, enabling accurate extraction of slow near-surface de-trapping processes.
- **Intermediate V_{DS} filling:** $(V_{GF}, V_{DF2}) = (V_T - 4, 8)$ V with $(V_{G,ON}, V_{D,ON2}) = (1, 4)$ V. Extends the depletion region deeper into the barrier and partially into the buffer, activating mid-depth traps such as interface or dislocation-related states. The moderate on-state V_{DS} ensures biasing of the device to saturation region, thus both V_T shifts and dynamic-R_{ON} effects are captured.



(a)



(b)

Figure 3.12: Normalized I_{DS} transients recorded at different T_{chuck}, referenced to $I_{DS}(Q_0)$, from pulsed measurements at the corresponding on-state, obtained at a chuck temperature of 60°C (left), together with the respective differentials, where the de-trapping time constants (at 100 °C) are marked with striped lines (right) [B]: (a): For the three different filling and on-states, these four devices without pre-gate annealing provided complementary information for trap analysis, the Arrhenius plot of CF_4 LONG subject to $(V_{GF}, V_{DF2}) = (V_T - 4, 8)$ V with $(V_{G,ON}, V_{D,ON2}) = (1, 4)$ V is demonstrated in Fig. 3.13a.**(b)**: These devices, having been subject to 800 °C pre-gate annealing, reveal the thermal sensitivity of T_4 and T_6, the Arrhenius plot of CF_4 MID subject to $(V_{GF}, V_{DF2}) = (V_T - 4, 8)$ V with $(V_{G,ON}, V_{D,ON2}) = (1, 4)$ V is demonstrated in Fig. 3.13b.

- **High V_{DS} filling:** $(V_{GF}, V_{DF3}) = (V_T - 4, 25)$ V with $(V_{G,ON}, V_{D,ON2}) = (1, 4)$ V. Drives the depletion region far into the buffer, efficiently filling deep-level traps such as Fe-related acceptors. Using the same on-state as in the intermediate case allows direct comparison of transients while isolating trap depth effects.

Aggregating results from these three bias regimes enables spatial separation of traps and reveals their thermal activation/deactivation behavior across the full device depth.

Temperature-Dependent Suppression and Activation of Trap States

The two traps most critical to understanding the annealing-dependent I_{ds} transient behavior are T_4 and T_6.

T_4 is a shallow fluorine-related acceptor state, introduced by CF_4 over-etching. It

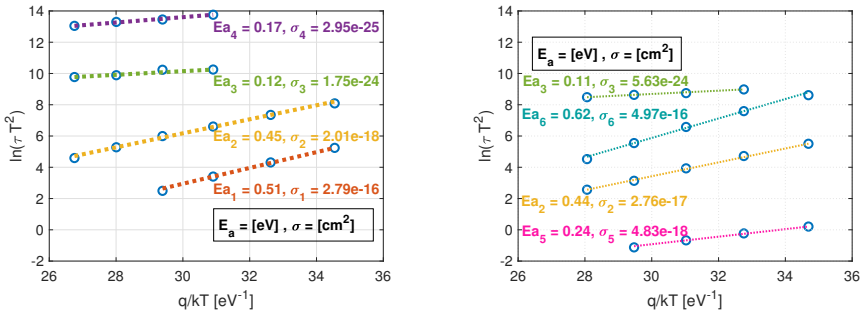


Figure 3.13: Arrhenius curve fittings for two specific devices shown in Fig.3.12: **(a)**: example of Arrhenius extraction from CF_4 LONG without pre-gate annealing, shown in Fig. 3.12a. **(b)**: example of Arrhenius extraction from CF_4 MID with 800°C pre-gate annealing, shown in Fig. 3.12b.

exhibits a very small σ, which results in slow trapping and de-trapping dynamics. The α of T_4 increases with plasma exposure duration (Fig. 3.12a), indicating a correlation with fluorine implantation and associated damage in the gate region. These slow dynamics contribute to threshold voltage (V_T) shifts and dynamic-R_{ON} degradation under switching conditions. Importantly, moderate annealing between 550–600°C effectively suppresses T_4, leading to improvements in both V_T and R_{ON}, as shown in Fig. 3.10.

The characteristics of T_6, and thermally activated nature, explain the consistent degradation observed in both DC and PIV measurements after annealing at or above 700°C. The re-emergence of positive V_T shifts (Fig. 3.10) despite fluorine trap de-activation, as well as the aggravated current collapse and increased dynamic R_{ON} (Fig. 3.11a), are consistent with the rapid trapping and long-term charge retention behavior of T_6. Furthermore, the XPS data confirms an increased presence of oxygen for all F plasma treatments. This finding together with the discovery that high temperature annealing at 800°C of $Al_xGa_{(1-x)}N$ with $x > 0.3$ has a tendency to form oxygen-related DX-like acceptor states [83], provide a solid basis for explaining the origin of the T_6 trap state. The diffusion of these traps into the access regions at elevated annealing temperatures aligns with the spatial broadening of transient degradation observed in PIV (Fig. 3.11b). Together, these results establish T_6 as the primary driver of the irreversible degradation observed at high-temperature annealing conditions.

Thermally Stable Traps

The remaining traps (T_1, T_2, T_3, T_5) are relatively thermally stable and consistently detected in all F-treated devices.

Trap T_1, attributed to Fe-induced background traps in the buffer, only appears at high filling biases $V_{DF} \geq 8$ V, which suggests its deep location. Conversely, trap T_5 is prominent at low V_{DF} of 0.5 V, indicating a location near the surface or in the top barrier. T_5 matches the signature of dislocation-related defects and remains stable even after 850°C annealing [84].

Trap T_2 is omnipresent across all measurements and aligns well with an oxygen atom occupying a nitrogen vacancy site (O_N), supported by XPS data showing high

oxygen content and nitrogen depletion post plasma exposure (Fig. 3.9a). Trap T_3, with similar E_a but significantly smaller σ, is likely a pure V_N state, more prevalent after aggressive CF_4 plasma etching.

The spatial origin of traps is reflected in their filling bias dependencies:

- T_1 grows with increasing V_{DF}, consistent with deep-level buffer traps.
- T_5 dominates at low V_{DF}, implying near-surface activity.
- T_2 and T_3 show intermediate filling behavior, matching the barrier/interface region.

Overall, DCTS measurements confirm that moderate annealing (550–600°C) deactivates the shallow fluorine-related trap T_4, improving DC and dynamic performance. However, excessive thermal budgets (≥ 700°C) activate the deep oxygen-related trap T_6, resulting in irreversible degradation, including positive V_T shifts and increased dynamic-R_{ON}. These observations are consistent with XPS findings and pulsed-IV trends. The combined spectroscopic and electrical data strongly support a trap-driven mechanism for the annealing dependence of GaN HEMT performance.

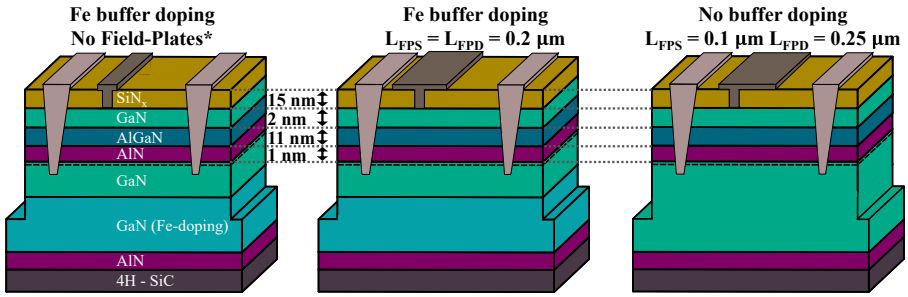


Figure 3.14: the layout split for the Fe-doped buffer devices in [Paper D]. To the left, **Fe-doped buffer, No FPs***. In the middle, **Fe-doped buffer, with FPs**. To the right, **No buffer doping, with FPs**. Note that the dimensions are not to scale. * Due to process conditions described in Chapter 2.3 mini-FPs of ca 50 nm are present, as exemplified by Fig. 3.15a and Fig. 3.15b.

3.3 Trapping dynamics at cryogenic temperatures

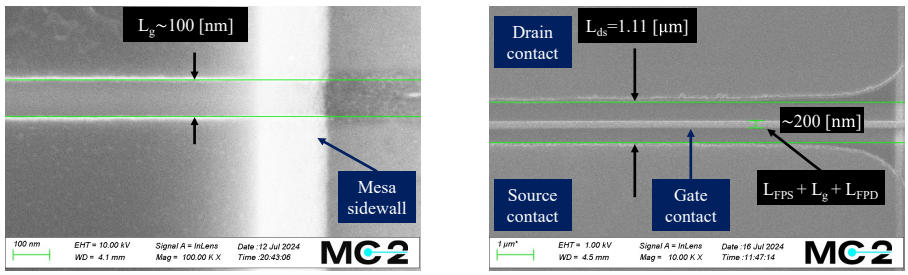
AlGaN/GaN HEMTs have shown promise for cryogenic applications such as radio astronomy and quantum computing due to their relatively low-noise and high power-handling characteristics even at deep cryogenic temperatures (4–10 K) [85, 86]. These advantages stem from high electron velocity combined with reduced parasitic resistances and increased mobility at cryogenic environments [87]. However, at so low temperatures, electron trapping becomes more pronounced, leading to current collapse and degraded device performance. This degradation has been attributed to trap states activated at low temperatures and is especially exacerbated in structures containing Fe-doped GaN buffers. While Fe-doping enhances breakdown and suppresses short-channel effects, it introduces deep acceptor traps with long de-trapping time constants that impair cryogenic operation.

Although trapping effects in GaN HEMTs have been widely studied at or above 77 K, there remains a lack of systematic evaluation at deep cryogenic temperatures [88, 89], particularly regarding the distinct roles of Fe-doping and field plates (FPs). Prior work has not fully disentangled the impact of buffer-induced and surface-related traps under these conditions, limiting our understanding of how to optimize device structures for reliable cryo-electronics. The subject of trapping in GaN HEMTs at cryogenic temperatures builds upon several previous studies on GaN HEMTs at cryogenic temperatures:

- In Paper [a], **a process and device layout optimized for cryogenic low-noise operation were developed.** The study introduced a bias- and frequency-dependent noise model for AlGaN/GaN HEMTs operating at $\sim$ 10 K, demonstrating state- of-the-art performance and identifying key contributions from intrinsic device properties and parasitic effects, providing clear targets for further optimization.

- In Paper [b], **a process and device layout with superconducting NBN gates for low noise applications were developed.** Resulting in reduced gate resistance and verified superconductivity at cryogenic temperatures, though the Nb-gated device showed a 5 K higher $T_{\text{min-opt}}$, due to suppression of superconductivity at the optimum-noise bias.

- In Paper [f], **Devices with a split on MIS/Schottky gate were developed.**



(a) **(b)**

Figure 3.15: SEM images showing the same device after two process steps defining the L_g and gate metal dimensions for the Fe-doped buffer, No FP devices: (a): By over-etching the SiN_x the GaN cap is exposed, the opening in the SiN_x serves as the L_g. **(b)**: Gate metal deposition, employing a margin of ∼50 nm with respect to the gate recess opening, thus resulting in FPs of ∼50 nm.

Enabling a comparative study for cryogenic low-noise applications was conducted. Measurements at ~ 4 K demonstrated comparable state-of-the-art noise performance, with the MIS-HEMT benefiting from reduced gate capacitance at low bias and the HEMT showing advantages at higher bias conditions.

- In Paper [g], **Devices with a split on gate-widths were fabricated.** The varying gate peripheries facilitated the employment of a scalable small-signal and noise model for AlGaN/GaN HEMTs operating at $\sim$ 10 K. The established model provides a framework for device and LNA optimization.

Within this research effort, one study directly addresses trapping, i.e. **Paper D**. The findings of this study are included in this thesis and are discussed in this chapter.

3.3.1 Buffer doping and field plate modulation of trap activation

Paper [D] investigates $Al_{0.3}Ga_{0.7}N$/GaN HEMTs with variations in both buffer doping and gate FP design, using DC, PIV, and DCTS. This enables a clear separation of buffer-induced and surface-induced trapping mechanisms, and allows examination of how FP geometry influences trap activation and de-trapping dynamics. Three device types were evaluated, Fig. 3.14:

- **Fe-doped buffer, No FP** — Serves as both a worst-case trapping prone device but at the same time a realistic low-noise design variant, illustrating the cryogenic trade-off between reduced parasitics for better noise performance [90], while simultaneously being more susceptible to trapping.
- **Fe-doped buffer, with FP** — Same Fe-doped epistructure as above, but with gate field plates of $L_{\mathrm{FPS}} = L_{\mathrm{FPD}} = 0.2\,\mu$m, designed to reduce peak electric fields and thereby mitigate trapping.
- **Undoped buffer, with FP** — Incorporates asymmetric field plates of $L_{\mathrm{FPS}} = 0.1\,\mu$m and $L_{\mathrm{FPD}} = 0.25\,\mu$m, serving as a baseline to study predominantly surface and access-region trapping.

The “No FP” label refers to the smallest field-plate (FP) dimension that can realistically be fabricated, as described in Fig. 2.3, a complete absence of FP is not

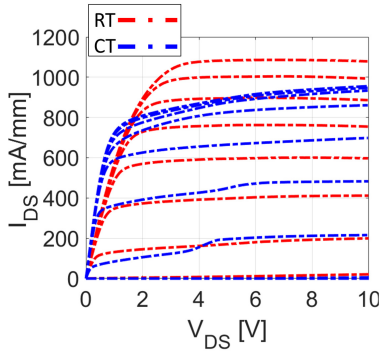


Figure 3.16: DC output characteristics of the Fe-doped buffer, No FP device: The same bias sweep V_{GS} -3 to 1 V in steps of 0.5 V was done at cryogenic (blue) and room (red) temperature [D].

feasible. For example, Fig. 3.15a and Fig. 3.15b show SEM images of the same device, where the gate still has FPs of about 50 nm.

In contrast, devices with a **Fe-doped buffer and FP** have much larger FPs, which significantly affect the electric field profile and, in turn, device performance. While **Fe-doped buffer, with FP** and **Undoped buffer, with FP** use slightly different FP geometries, the main performance difference between them arises from the buffer design. In summary, Paper [D] performs two key comparisons, both focusing on trapping:

1. **Fe-doped buffer, No FP** vs. **Fe-doped buffer, with FP** — isolates the effect of FP geometry.
2. **Fe-doped buffer, with FP** vs. **Undoped buffer, with FP** — isolates the effect of buffer design.

By extending the temperature range and combining epitaxial with layout variations, the study reveals how buffer doping and FP geometry shape cryogenic trapping behavior, knowledge that is critical for achieving fast recovery and low dynamic resistance in GaN HEMTs for cryogenic applications.

3.3.2 Trap manifestation

In Paper [D], DC and PIV are used over a large temperature range to provide a wider trap-characterization of GaN HEMTs than what is typically studied. These measurements were done in both dark and light conditions facilitating investigation of the trap response.

DC Measurements

At cryogenic temperatures, pronounced deep-level Fe-related trap impacts are observed, inducing a kink-effect for the **Fe-doped buffer, No FP** devices, Fig. 3.16. Additionally, the persistent occupation of acceptor-like states likely explains the positive shift in threshold voltage (V_T) as a consequence of a reduced two-dimensional electron gas (2DEG) density beneath the gate. By extension causing a degradation in $I_{DS,\max}$, despite improvements in on-resistance (R_{ON}). Although it should be mentioned that the positive shift in V_T at cryogenic temperatures could be as in InP

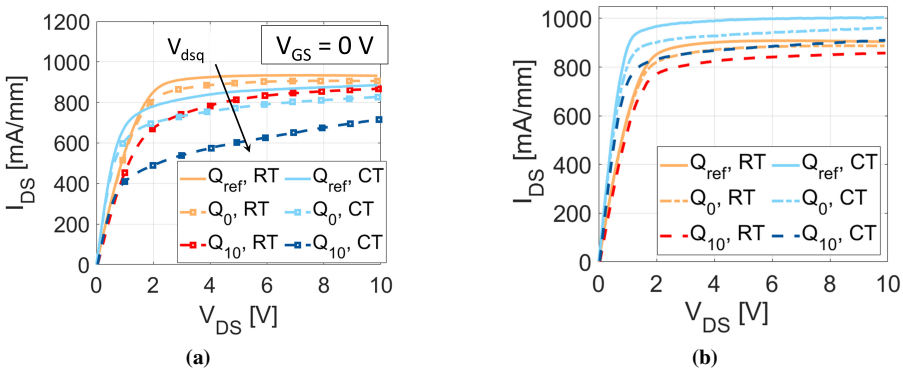


Figure 3.17: PIV output characteristics at cryogenic (blue) and room (red) temperature on device splits [D]: (a): Fe-doped buffer, No FP, **(b)**: Fe-doped buffer, with FP.

HEMTs stem from increased 2DEG confinement, reducing phonon interactions and thus carriers occupy lower-energy subbands more strongly [91]. However, if that effect wore to dominate, the $I_{DS,\max}$ reduction would be more universal rather than just tied to the **Fe-doped buffer, No FP** devices.

As previously demonstrated [92], wavelength-dependent light illumination can accelerate recovery from trap-induced current collapse in AlGaN/GaN HEMTs, enabling estimation of trap energy levels and identification of their origin. Here a GaN LED was used, which is guaranteed to supply the necessary energy for exciting any trap state in a GaN material. For **Fe-doped buffer, No FP** devices, light exposure at 4.2 K led to a significant recovery of $I_{DS,\max}$ (up to +17%), indicating that optical excitation facilitates the de-trapping of electrons from deep-level states. In contrast, no notable light-induced changes were observed at room temperature or in devices without Fe doping, reinforcing the link between Fe-related traps and cryogenic performance degradation. Moreover, FP devices demonstrated reduced sensitivity to light at cryogenic temperatures, only 1–2% variation in $I_{DS,\max}$, highlighting the role of modulating (or reshaping) the electric field profile within the device to suppress trap activation and improve recovery characteristics.

Taken together, these findings demonstrate that cryogenic trapping effects in GaN HEMTs are alleviated by epitaxial design, and device geometry. The use of undoped buffers and field plates emerges as a promising strategy to improve DC stability and mitigate trap-related degradation under cryogenic operation.

PIV

Pulsed sweeps were performed in a cryogenic probe station at RT (∼295 K) and CT (∼4.2 K) using short pulses (1 μs width, 1% duty cycle). Dynamic R_{ON} was extracted from pulsed $I_{\mathrm{DS}}(V_{\mathrm{DS}})$ with 0.1 V steps. Unless otherwise stated, stressed measurements were taken in the dark, whereas reference sweeps included optical illumination to promote de-trapping.

Under baseline measurement conditions (no prior intentional trap charging and with optical illumination during the reference sweep), the **Fe-doped buffer, No FP** device, Fig. 3.17a exhibited notably more trapping phenomenon compared to **Fe-doped buffer, with FP**, Fig. 3.17b, as can be seen in the dynamic R_{ON} comparison

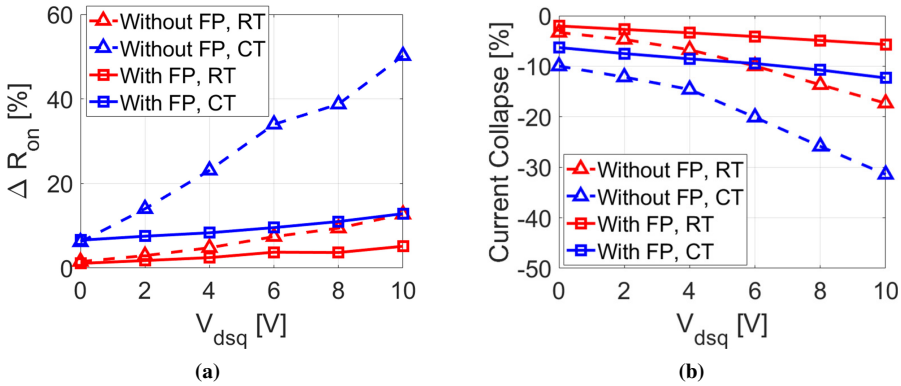


Figure 3.18: PIV comparisons at cryogenic (blue) and room (red) temperatures on the device splits: Fe-doped buffer, No FP and Fe-doped buffer, with FP [D]: (a): Dynamic-R_{ON}, **(b)**: Current collapse.

Fig. 3.18a and further supported by the current-collapse comparison in Fig. 3.18b. Findings that align with the DC observation of a CT kink and reduced $I_{DS,\max}$ in the same split, where light exposure at CT partially reverses the collapse through photo-assisted de-trapping.

Introducing a gate field-plate substantially mitigates these effects in the **Fe-doped buffer, with FP** device (Fig. 3.17b). At CT, the FP reduces drain-lag driven collapse by up to a factor of $\sim$2.6 and suppresses the dynamic R_{ON} increase by roughly 4 fold at high V_{DSQ}, while also making the characteristics largely insensitive to illumination.

For the **undoped buffer, with FP** device (Fig. 3.19a), the CT to RT difference in PIV is modest, ΔR_{ON} Fig. 3.19b, and current collapse Fig. 3.19c, remain low and show little dependence on V_{DSQ}, consistent with the lack of buffer-related trapping when Fe is not introduced. Any residual dynamics are attributable to surface/interface states and access regions rather than buffer traps.

In comparing the **Fe-doped buffer, with FP** device, Fig. 3.17b to the **undoped buffer, with FP** device, Fig. 3.19a, an interesting observation can be made: at $V_{\mathrm{DS}} =$ 4 V under short-pulse conditions, the **Fe-doped buffer, with FP** can exhibit lower apparent current collapse and ΔR_{ON} than the undoped device, despite the absence of buffer traps in the latter. This counterintuitive result is likely not due to intrinsic trapping in the buffer, but rather to differences in epitaxial growth and processing between the two splits, including possible variations in surface state density, passivation quality, and access-region resistance. Such factors can influence the measured dynamic behavior, particularly at low V_{DSQ}, where the **undoped buffer, with FP** device may appear more affected despite lacking Fe-induced deep traps. Consequently, these PIV results highlight that dynamic ΔR_{ON} and current collapse are sensitive to both buffer and surface/interface properties, and that care must be taken when attributing differences solely to buffer-related trapping.

Pulsed $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ and $g_m(V_{\mathrm{GS}})$ (at $V_{\mathrm{DS}} = 4$ V) further clarify the presence of trapping. At CT, the **Fe-doped, no FP** split shows a small positive shift of the apparent threshold/pinch-off and a pronounced g_m roll-off at high V_{GS} that is aggravated with V_{DSQ}, both consistent with drain-side trapping [93]. Illumination at CT partially restores the transfer and g_m curves (photo-assisted de-trapping). In contrast, the **Fe-doped, with FP** device exhibits negligible g_m degradation and only minor V_T

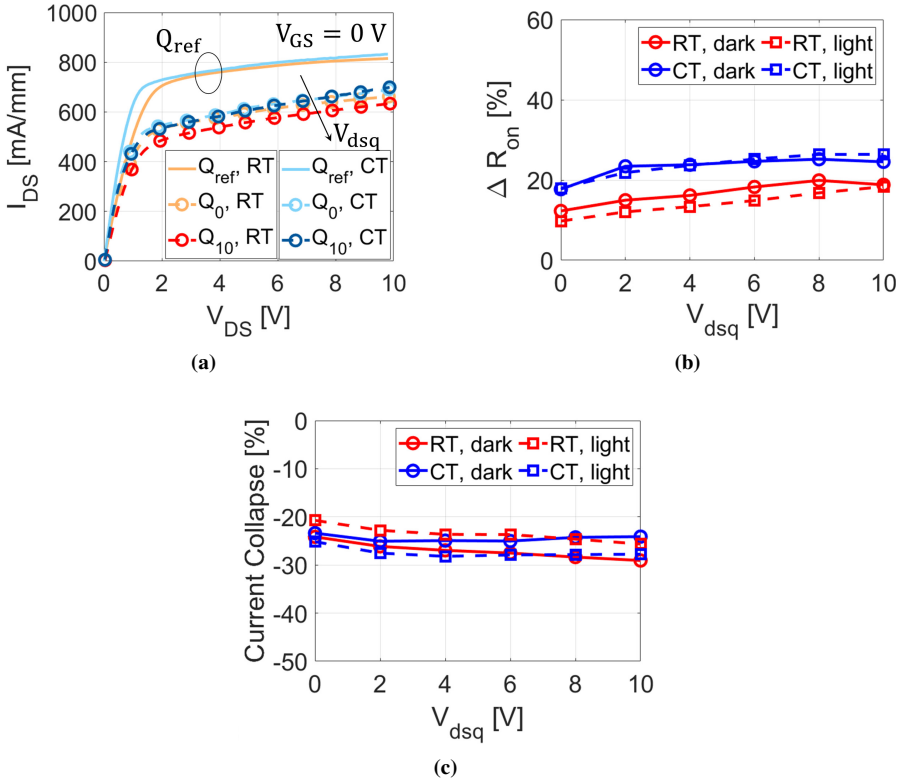


Figure 3.19: PIV at cryogenic (blue) and room (red) temperature on: Undoped buffer, with FP [D]: (a): output characteristics , **(b)**: Dynamic-R_{ON}, **(c)**: Current collapse.

movement with V_{DSQ}, indicating effective field moderation by the FP. The **undoped, with FP** device shows the smallest CT to RT change, a slight increase of peak g_m upon cooling, and no clear drain-lag signature in the transfer characteristics.

3.3.3 Trap Analysis

While DC and pulsed I–V measurements in Paper [D] revealed clear evidence of cryogenic trapping effects, particularly in Fe-doped devices, they did not offer direct insight into the physical mechanisms underlying those effects. To better understand the nature, depth, and dynamics of the responsible trap states, drain current transient spectroscopy (DCTS) was employed.

However, applying DCTS at cryogenic temperatures presents several important challenges. One key limitation is related to the time resolution of the measurement setup, which ranges from microseconds to tens of seconds. At cryogenic temperatures, trap emission times can exceed the measurement window, rendering many de-trapping events effectively undetectable in practical experiments. We can re-write Eq. 2.12 to study the emission rate from a trap level:

$$\frac{1}{\tau} = \sigma_n \cdot \langle v_{\mathrm{th}} \rangle \cdot N_C \cdot \exp\left(-\frac{E_a}{kT}\right) \tag{3.2}$$

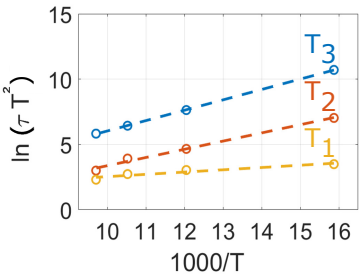


Figure 3.20: Arrhenius plot for E_a and σ extraction of trap states [D].

TABLE 3.2: SUMMARY OF TRAP STATES EXTRACTED FROM DCTS MEASUREMENTS, THE CHANNEL TEMPERATURE T WAS ESTIMATED TO RANGE FROM T_{chuck} + 5K-25K, CAUSING A WIDE RANGE OF E_a AND σ VALUES [D].

Trap	E_a [eV]	σ [cm^2]	β
T_1	0.17 (0.10 – 0.22)	$6.3 \cdot 10^{-22}$ ($5 \cdot 10^{-22} - 7.8 \cdot 10^{-22}$)	0.5
T_2	0.63 (0.41 – 0.76)	$2.6 \cdot 10^{-20}$ ($7 \cdot 10^{-20} - 5.2 \cdot 10^{-19}$)	0.58
T_3	0.79 (0.53 – 0.96)	$9.5 \cdot 10^{-21}$ ($1.8 \cdot 10^{-21} - 2.3 \cdot 10^{-20}$)	0.9

Here, both the thermal velocity $\langle v_{\text{th}} \rangle$ and the effective density of states N_C are temperature-dependent, scaling as $\sqrt{T}$ and $T^{3/2}$, respectively. Combining these with the exponential factor leads to the following temperature dependence for the de-trapping time constant:

$$\tau(T) \propto \frac{1}{T^2} \cdot \exp\left(\frac{E_a}{kT}\right) \tag{3.3}$$

This expression highlights that as temperature decreases, the exponential term dominates, causing τ to increase rapidly. At cryogenic temperatures, even shallow traps can become effectively "frozen" with emission times stretching far beyond typical measurement scales.

Temperature stability is another concern. At cryogenic conditions, the chuck temperature (T_{chuck}) is more difficult to control precisely than at room temperature, introducing uncertainty into the estimated channel temperature. This directly affects the reliability of Arrhenius-based extraction of trap parameters. In addition, the material properties of GaN change with temperature. Specifically, the bandgap widens by approximately 0.07–0.08 eV at 4–8 K compared to room temperature [94]. This shift can increase the apparent activation energy (E_a) of traps and reduce their emission rates, further complicating the interpretation of transient data.

Taken together, these factors introduce greater uncertainty in the extracted values of activation energy and capture cross-section (σ) at cryogenic temperatures. The reported trap properties in this study should therefore be interpreted within the context of these limitations.

DCTS

To investigate the cryogenic trapping effects observed in DC and pulsed I–V measurements, Paper [D] employs drain current transient spectroscopy (DCTS) over the T_{chuck} 45–85 K range, This temperature range was selected to ensure that the trapping dynamics were under cryogenic conditions, while at the same time giving the traps sufficient kinetic energy for de-trapping in a µs to 10's second time window. The measurements were performed on **Fe-doped buffer, No FP** devices, using a quiescent OFF-state filling bias of $V_{\text{GF}} = -5$ V and $V_{\text{DF}} = 10$ V to promote buffer-related trap activation.

Three trap states were extracted. T_1 ($\sim$0.17 eV) is attributed to either carbon, nitrogen vacancy or surface states [68] [95] [52], consistent with gate-lag behavior seen in undoped-buffer devices. T_2 ($\sim$0.63 eV) is likely Fe-related [69], while T_3 ($\sim$0.79 eV) may stem from Fe-complexes or intrinsic defects such as nitrogen interstitials or gallium vacancies [96]. Both deeper states exhibit strong temperature dependence and slow emission, explaining the persistent current collapse in Fe-doped devices.

At the lower channel temperature T , the associated emission times span from $\sim 10^{-2}$ to $\sim 10^{1}$ s, explaining the persistent current collapse after high-V_{DQ} stress at cryogenic temperatures.

The extracted σ for all three traps were up to three orders of magnitude lower than reported at higher temperatures. This is attributed to reduced trap–carrier interaction rates at cryogenic temperatures, where thermal activation is suppressed. Similar trends of underestimated σ values have been observed in prior DCTS studies (Chapters 3.1 and 3.2), although to a smaller degree.

Overall, these results give indications that Fe-induced buffer traps dominate cryogenic trapping behavior. Their absence in undoped buffers and partial mitigation via field plates underscores the importance of both epitaxial and layout design for reliable low-temperature GaN HEMT operation.

Chapter 4

Harnessing deep-level charge effects in varactor applications

As detailed in Chapter 3, trap states are typically considered detrimental to device performance. However, under specific AC signal regimes, these same states may behave as quasi-static charges, modifying the electrostatic potential and enabling tailored depletion behavior. When properly harnessed, such effects can enable engineered C–V profiles with enhanced linearity and reproducibility. With the quasi-static charge behavior being in center for the subsequent parts of this chapter, these states will henceforth be referred to as "charge states" rather than "trap-states", which was the convention in the previous chapter.

In high-frequency microwave and millimeter-wave applications, the ability to dynamically control circuit elements such as phase shifters, filters, and matching networks is essential. Central to these functionalities are varactors (voltage-controlled capacitors), which support tunable frequency response and adaptive matching.

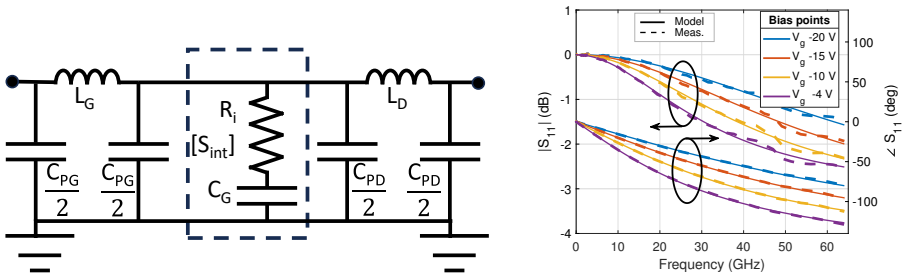
This chapter explores how charge-state engineering, via plasma treatment and annealing, can be used to modulate the reverse-bias C–V characteristics of GaN varactors. The goal is to realize devices with both high linearity and sufficient tuning range by leveraging deep-level charge effects introduced during HEMT fabrication.

4.1 The GaN HEMT Varactor development

GaN-based varactors are increasingly favored due to their high breakdown voltage, excellent Q-factor (e.g., in MSM varactors), and compatibility with monolithic GaN MMIC integration [97, 98]. GaN tunable filters and phase shifters have demonstrated superior power handling and signal integrity [99], while GaN VCOs now rival GaAs-based solutions in phase noise and tuning performance [9].

To mitigate the inherent nonlinearity of the C–V response in tunable matching networks (TMNs), anti-series configurations are often employed. These improve effective linearity and increase breakdown tolerance, but introduce added circuit complexity and parasitic effects [100]. While such configurations have recently been demonstrated in GaN-based designs [101], they still fall short of providing predictable, wide-range linear behavior.

Despite these advancements, achieving varactors with intrinsically linear C–V char-



(a) (b)

Figure 4.1: the small-signal model and verification [C]: (a): Small-signal equivalent circuit, where the intrinsic circuit is within the striped lines. **(b)**: Intrinisc model (filled) and measurement (striped) S_{11} magnitude and phase at different gate reverse bias points.

acteristics across a broad voltage span remains a significant challenge. Nonlinearity in the capacitance response can lead to undesirable phase deviations and inconsistent tuning behavior, especially problematic in beamforming and adaptive RF front-end applications [19].

To date, no varactor structure has been demonstrated that combines reproducibly linear C–V behavior with full MMIC compatibility in GaN technology.

4.1.1 C–V modulation using F plasma and annealing

This study, [Paper C] branched from an unexpected discovery made concerning the device behavior in study [Paper B], described in Chapter 3.2. Hence all the study splits detailed in Fig. 3.7a were available for the study discussed here. This work addresses the above described research gap by investigating how standard HEMT processing steps, specifically fluorine-based plasma etching and subsequent annealing, can be leveraged to control charge-state formation and thereby engineer the C–V response.

Central to the capacity for C–V modulation are the charged states introduced due to F plasma treatment, acceptor (F^-) and donor (O^+) states [102–104], forming a high concentration of charge-states in the gated region. This altered charge state distribution directly impacts the depletion width for a given gate voltage, and thereby modulates the C–V profile. Furthermore, many of the fluorine-induced acceptor states are thermally unstable [82], allowing further control via post-etch annealing.

This work proposes that such plasma-induced charge-states, can be deliberately exploited to produce highly linear and reproducible C–V characteristics. Small-signal measurements demonstrate the feasibility of this approach, while TCAD simulations provide physical insight into the mechanisms involved, including the effects of SiN_x relative-permittivity ε_r, field-plate geometry, and the spatial distribution and concentration of O and F states.

4.1.2 Small-Signal Modeling

To evaluate the C–V characteristics of the fabricated GaN varactors, S-parameter measurements were performed. Devices were biased with V_{GS} swept from -30 V to $+1$ V in 0.1 V steps, while $V_{DS} = 0$ V.

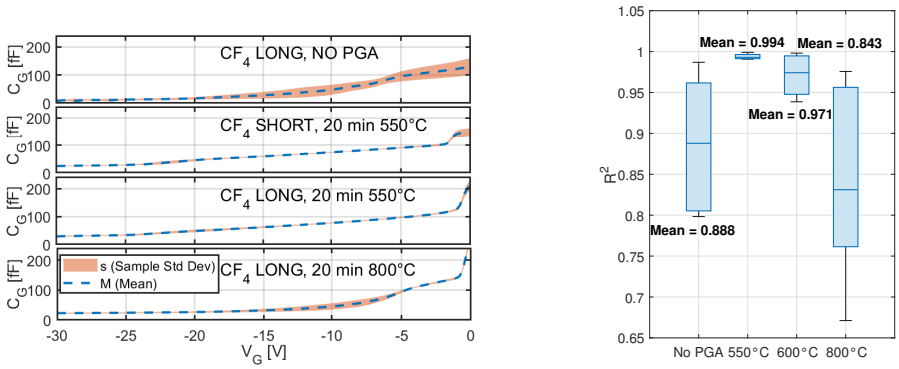


Figure 4.2: Summary of statistical analysis on the CF_4 plasma treated devices [C]: (a): Ranging from no annealing up to 800 °C, the mean and sample standard deviation is provided for 5 devices per study-split. **(b)**: By grouping together all over-etching treatments, four different splits (10 devices per category)in relation to thermal treatment is obtained, the R^2 serves to estimate the linearity of the C–V profile in the Vg = - 20 V to V_g = - 4 V range.

The HEMTs operated as varactors had the layout dimensions shown in TABLE 4.1. Parasitics were de-embedded through the procedure described in [105], and the intrinsic response was modeled as a gate capacitance C_g in series with resistance R_i Fig. 4.1a, which was found to agree well with measurement data Fig. 4.1b.

Extracted C–V Characteristics

CF_4 plasma-treated and 550°C annealed devices showed significantly more linear C–V profiles than reference or NF_3-etched samples. Linearity was assessed via linear regression over $-20\ \text{V} \leq V_G \leq -4\ \text{V}$, with CF_4-treated devices consistently achieving $R^2 > 0.99$, exceeding litterature value of $R^2 > 0.99$ up to 0.962 [9]. With the CF_4 plasma treated devices overwhelmingly providing a more linear C–V profile, additional investigations was made on five devices in each study-split to establish the statistical reproducibility of the C–V profile. When comparing across different plasma over-etching degrees from SHORT to LONG and an additional dimension being the pre-gate annealing temperature, it was concluded that the most linear responses came from the devices annealed at 550 °C. Additionally, low variation in C–V profile and tuning range was confirmed for both SHORT and LONG plasma treatments Fig. 4.2a. Thus, when making an aggregated comparison of linearity using box-plots of the R^2 for different annealing temperatures, the SHORT and LONG samples are grouped together, thus eah category consists of 10 samples Fig. 4.2b.

The specified gate voltage range provides a tuning range of 2.3:1, which together with the Q-factor was used to compare to previously studied GaN HEMT varactors.

$$Q = \frac{1}{\omega_0 R_i C_g} \tag{4.1}$$

It was concluded that the Q-factor of 17 observed (at 10 GHz and $V_G = -3.5$ V), matched previous GaN HEMT varactor results [9, 106]. While the mean linearity R^2 of 0.994 was well above the best C–V linearity found in literature with R^2 of 0.968 [9].

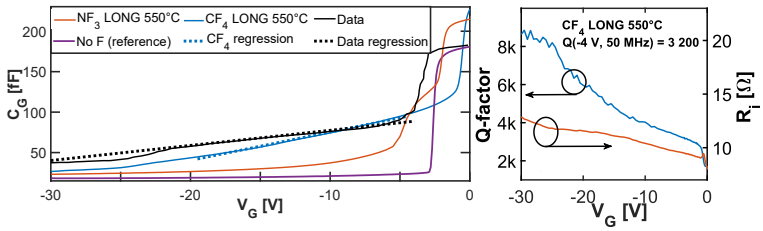


Figure 4.3: To the left: Capacitance–voltage (C–V) characteristics at 50 MHz for a CF_4 plasma–treated GaN HEMT varactor (annealed at 550 °C). Within the study, the results are compared with typical C–V curves from devices without fluorine plasma treatment and with NF_3 plasma exposure. For the CF_4-treated device, linear regression over the bias range ($V_G = -20$ V to $V_G = -4$ V) yields $R^2 = 0.994$ and a tuning ratio of 2.3:1. For the same tuning ratio, literature data from [9] ($V_G = -30$ V to $V_G = -4$ V) produce a linear fit with $R^2 = 0.962$. **To the right:** Q-factor at 50 MHz as a function of V_G, calculated using R_i extracted at 67 GHz [C].

These results confirm that fluorine plasma processing and controlled annealing can produce reproducible, linear C–V profiles suitable for MMIC-integrated RF tuning applications.

4.1.3 TCAD simulations

Simulation objectives and overview

Technology Computer-Aided Design (TCAD) AC simulations were employed to investigate the physical mechanisms responsible for the observed modulation of the C–V characteristics in GaN HEMT varactors subjected to fluorine plasma treatment and subsequent annealing. Specifically, the simulations aim to reproduce key features observed in the experimental data to isolate which process/layout parameters (e.g., charge-state, dielectric properties, field plate geometry) drive these effects.

In addition to validating experimental findings, the simulations are used to identify how charge-based mechanisms and geometric factors can be co-optimized to achieve highly linear and tunable C–V responses suitable for MMIC varactor applications.

Device structure, physics and meshing strategy

The simulated device structure is based on a two-dimensional (2D) cross-section of the fabricated GaN HEMT varactors, reflecting the layout parameters summarized in TABLE 4.1. The epitaxial stack starts from a SiC substrate, upon which an AlN nucleation layer and a Fe-doped GaN buffer layer is grown, that gradually transitions from a peak concentration of $2 \cdot 10^{18}$ cm^{-3} into an unintentionally doped (UID) GaN channel as the Fe concentration decays to $7 \cdot 10^{15}$ cm^{-3}, Fig. 4.5b. This is followed by an AlN interlayer, an AlGaN barrier and a GaN cap, with a 15 nm thick SiN_x passivation layer on top. The corresponding layer dimensions are illustrated in Fig. 4.4. Polarization charges due to the spontaneous and piezoelectric properties of GaN, AlN and AlGaN are included at the heterointerfaces. The passivation was modelled as a leaky dielectric with a $\varepsilon_r = 8$, consistent with LPCVD Si-rich stoichiometry , assuming static values apply at 67 GHz and below [107]. To reduce computational time, the SiC substrate was excluded from the simulation. Devices treated with CF_4 plasma are modeled with a gate recess extending 6.5 nm into the top barrier, thus diverging

TABLE 4.1: DEVICE GEOMETRY PARAMETERS

Feature	[μm]
L_{gs}	0.75
L_{FPS}	0.1
L_{gd}	1.75
L_{FPD}	0.25
L_g	0.2
W	100

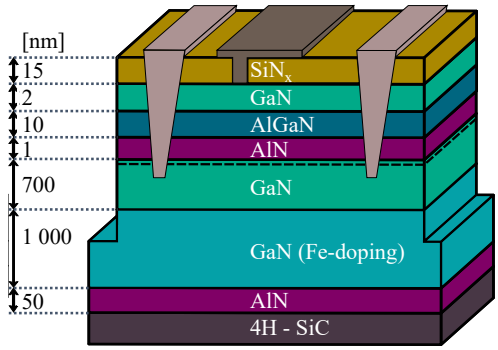


Figure 4.4: the epitaxial structure of the measured HEMTs operated as varactors in Paper [C], which are the same devices as in [Paper B]. Together with the layout parameters specified in TABLE 4.1 a full device geometry overview is provided.

from the simulated NF_3 plasma treated devices Fig. 4.5a, corresponding to the LONG over-etch split described in Section 3.2.

To ensure numerical convergence and accurate resolution of steep potential gradients, fine meshing is applied in the critical regions, particularly under the gate foot, near the field plates, and at the ohmic contacts. These are areas where depletion regions form and collapse during the bias sweeps, and where the charge-state dynamics most strongly affect the local electric field and carrier distribution.

the primary transport mechanism is the drift-diffusion model, which is commonly used in AlGaN/GaN device simulators for reverse-biased varactor-type structures, especially at low-frequency AC. This approach, when coupled to trap-rate (SRH) models, reliably captures the effects of charge-states, without requiring complex high-field or non-local transport physics (which become significant only at high AC frequencies or extreme bias) [108].

The charged states introduced by fluorine plasma are modeled using Gaussian spatial distributions, with the concentration peaking near the surface and decaying according to a spatial standard deviation σ_{sp} in both the lateral (x) and vertical (y) directions. This applies to both F^- (acceptor) and O^+ (donor) states, as shown in Fig. 4.5b. The corresponding concentration and depth profiles were calibrated using X-ray photo-electron spectroscopy (XPS) measurements (Fig. 3.9a), from which estimates were made regarding the fraction of implanted fluorine that contributes to charged F^- states.

Based on prior work [77], it is assumed that only approximately 5% of the fluorine atoms introduced by CF_4 plasma etching form negatively charged acceptor states. Furthermore, pre-gate annealing has been shown to reduce the F^- concentration [82], by as much as 60% as discussed in Chapter 3.2. This leads to an effective charged fluorine concentration in the range of 10^{19} to 10^{20} cm^{-3}, depending on the plasma chemistry used (CF_4 vs. NF_3).

However, the formation of F^- states in NF_3 plasma-treated devices remains more uncertain. Unlike CF_4 treatments, NF_3 does not cause a significant threshold voltage (V_T) shift (see Fig. 3.10), making it difficult to assess how many negatively charged fluorine states are actually generated. Nevertheless, as shown in the simulations, these states significantly impact the depletion characteristics and electrostatics of the gated region.

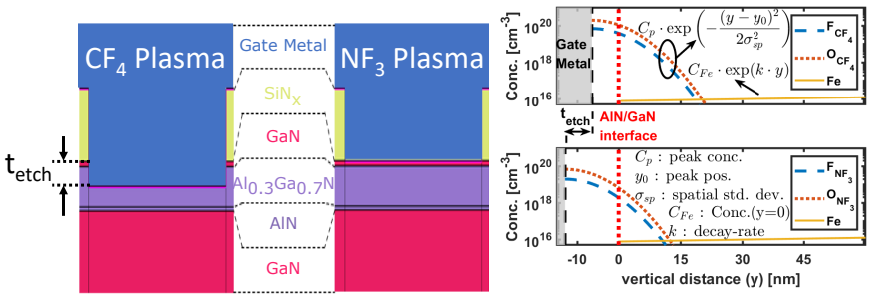


Figure 4.5: Overview of 2D layout and charge state distribution in the near gate region:(a): Zoomed in 2D perspective of the gated region in the structure used for TCAD simulations. The left-hand (right-hand) figure represents the device subject to CF_4 (NF_3) plasma LONG over-etching. Note that the t_{etch} marks a recessing of the gate corresponding to 6.5 nm. **(b)**: in accordance with the differences in barrier etching, the CF_4 (top) and NF_3 (bottom) obtains different vertical depths of the implanted F and O states. The general gaussian expression used to model the O and F state distributions is provided, where y_0 is set at the metal/surface interface. Additionally, an exponential expression for the Fe states is shown. The vertical depth of y = 0, is defined as the interface between the AlN/GaN interface.

Device biasing and solver settings

A bias sweep is performed in the time domain to capture the influence of slow charge-state dynamics under varying bias conditions. At each steady-state bias point, small-signal AC simulations are conducted to evaluate the frequency-dependent C–V characteristics.

Initially, all terminals are set to 0 V bias. The gate voltage is then linearly swept from 0 V to −30 V over 0.1 s, after which it is stepped upward to +2 V in 0.75 V increments. Each step is held for 1 s to allow the system to reach quasi-static equilibrium before AC analysis. At each DC bias point, small-signal AC simulations are performed across the frequency range of 50 MHz to 67 GHz. These analyses solve both Poisson's and the continuity equations self-consistently:

$$\rho = q\left(p - n + N_D^+ - N_A^- + \rho_{\text{fixed}}\right) \tag{4.2}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}_n + G_n - R_n \tag{4.3}$$

Here, ρ is the total charge density, n and p are the concentrations of electrons and holes, N_D^+ and N_A^- are ionized donors and acceptors, and ρ_{fixed} includes polarization, interface, and charge-states. The electron continuity equation captures carrier transport via drift and diffusion, as well as recombination and generation dynamics. Solver convergence is validated by checking current continuity at each terminal, ensuring Kirchhoff's current law is satisfied throughout the simulation.

Simulation calibration using reference device

To enable meaningful physical interpretation and predictive modeling, the TCAD simulations were first calibrated against the measured characteristics of a reference

TABLE 4.2: MAIN SETTINGS FOR TCAD SIMULATIONS DEMONSTRATED IN FIG. 4.6

	Main Parameters	NF_3 Plasma	CF_4 Plasma	No F (Ref)
Layout	L_{FPD} [μm]	0.25		-
	t_{etch} [nm]	0	6.5	0
SiN_x (n = 2.3)	Thickness [nm]	15		No SiN_x
	ε_r	8		
Fluorine (acceptors)	Peak conc. [cm^{-3}]	$2 \cdot 10^{19}$	$7 \cdot 10^{19}$	No F
	E_a [eV]	0.2		
	σ [cm^2]	$4 \cdot 10^{-21}$		
	FWHM (x, y) [nm]	(2, 6)		
Oxygen (donors)	Peak conc. [cm^{-3}]	$7 \cdot 10^{19}$	$2 \cdot 10^{20}$	No O
	E_a [eV]	0.44		
	σ [cm^2]	$1 \cdot 10^{-18}$		
	FWHM (x, y) [nm]	(2, 6)		
Fe (acceptor)	C_{Fe} [cm^{-3}]	$7 \cdot 10^{15}$		
	Buffer Conc. [cm^{-3}]	$2 \cdot 10^{18}$		
	E_a [eV]	0.5		
	σ [cm^2]	$1.4 \cdot 10^{-16}$		
Surface (donors)	Surface Conc. [cm^{-2}]	$2.8 \cdot 10^{13}$		
	E_a [eV]	0.3		
	σ [cm^2]	$1.4 \cdot 10^{-19}$		

device. This device, fabricated without any fluorine plasma treatment or SiN_x passivation, features a block-gate structure and exhibits a well-defined threshold voltage ($V_T \approx -2.8$ V) in measurement. Its well-controlled electrostatics make it ideal for establishing the baseline conditions, particularly the dominant fixed charge states, that govern the depletion behavior in the absence of intentionally introduced charged states.

The calibration began by adjusting the surface donor charge density to reproduce the V_T in the measured C–V curve. A uniform donor-like surface charge distribution at the AlGaN/air interface was implemented, with a sheet concentration of $2.8 \cdot 10^{13}$ cm^{-2}, an activation energy of 0.3 eV, and a capture cross-section of $1.4 \cdot 10^{-19}$ cm^2. These parameters were iteratively tuned until the simulated 2DEG density ($\sim 1 \cdot 10^{13}$ cm^{-2}) matched Hall measurement data and the simulated C–V curve reproduced the measured threshold voltage and slope.

Additionally, the Fe-doped GaN buffer layer was modeled using a spatially varying acceptor trap profile, starting from a peak Fe concentration of $2 \cdot 10^{18}$ cm^{-3} near the substrate and exponentially decaying toward the channel, where the residual trap concentration approaches $7 \cdot 10^{15}$ cm^{-3}. These acceptor states, with an activation energy of 0.5 eV, were necessary to model the background compensation and buffer leakage control typical of Fe-doped HEMT structures.

With this charge environment defined, comprising surface donors and Fe-related buffer acceptors, the simulated device accurately reproduced the static electrostatics, depletion characteristics, and gate modulation observed in the reference sample. Importantly, the C–V response showed minimal variation below threshold, confirming the absence of additional charge contributions (such as F or O species), and validating

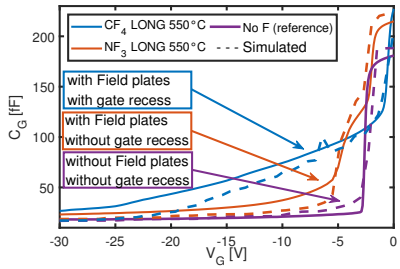


Figure 4.6: Measured and simulated C–V characteristics of the three varactor types. The reference device shows a sharp transition at V_T with minimal modulation below. The NF_3 device exhibits step-like depletion from 2DEG modulation under both the gate and field plates, while the CF_4 device shows enhanced sub-V_T modulation from combined field-plate effects and charge states near the gate and in the channel.

this as a clean calibration point.

Establishing a platform for charge-state engineering

Once the reference model was validated, it served as the foundation upon which additional structural and material modifications could be systematically introduced. Enabling isolated study of the effects on C–V characteristics caused by the parameters listed below:

- SiN_x passivation with varied permittivity (ε_r),
- Gate-connected field plates of adjustable length (L_{FPD}),
- Fluorine (F^-) and oxygen (O^+) charge-states with controlled spatial profiles and concentrations,

This modular approach allowed the simulations to transition from reproducing the reference structure to accurately modeling the measured C–V profiles of fluorine plasma-treated and annealed devices. Ultimately, it provided the insight necessary to deconvolve the contributions of field-plate-enhanced depletion, dielectric coupling, and implanted charge effects—all of which are essential to understanding and optimizing C–V linearity in GaN HEMT varactors.

Simulation-based optimization of C–V linearity

The calibrated TCAD models were used to analyze the individual and combined effects of field-plate length, SiN_x permittivity, and charge-state distributions introduced by plasma and annealing treatments. The goal was to identify how these parameters interact to shape the measured C–V characteristics and to explore design pathways toward even more linear and tunable varactor performance.

Field-plate

Simulations show that increasing the field-plate-to-drain length (L_{FPD}) results in a clear increase in the maximum achievable capacitance before pinch-off (C_{knee}) without significantly altering the threshold voltage $V_{T,FP}$, Fig. 4.7a. This is attributed to enhanced

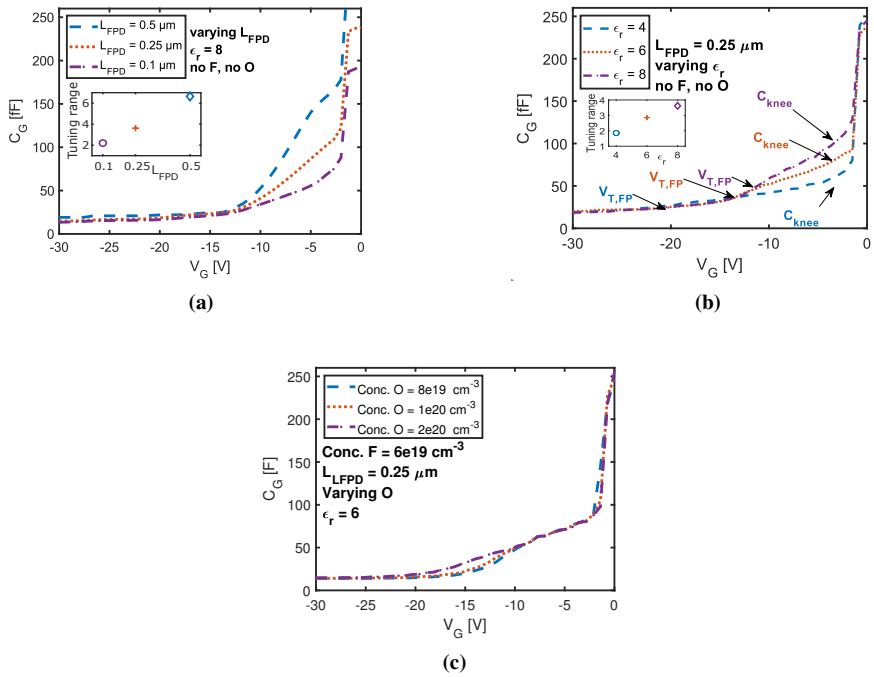


Figure 4.7: Simulation results illustrating the impact of key design parameters on C–V characteristics: (a): increasing field-plate length (L_{FPD}) raises the maximum capacitance (C_{knee}) with minimal change in $V_{\mathrm{T,FP}}$; **(b):** higher SiN_x relative permittivity (ε_r) enhances dielectric coupling, increasing C_{knee} and reducing $|V_{\mathrm{T,FP}}|$; **(c):** for devices with SiN_x, field plates, and both F^- and O^+ charge states, higher oxygen concentration produces a more linear C–V profile by maintaining 2DEG under the field plate and smoothing the capacitance roll-off.

capacitive coupling between the field plate and the 2DEG, effectively extending the charge-controlled region. This behavior enables more gradual capacitance roll-off with increasing reverse bias, contributing to improved C–V linearity.

SiN_x permittivity

The simulations further confirm that the relative permittivity of the SiN_x passivation layer plays a key role in modulating the gate electrostatics. Increasing ε_r from values associated with stoichiometric to Si-rich SiN_x formulations raises C_{knee} and reduces $|V_{\mathrm{T,FP}}|$, Fig. 4.7b. This effect stems from enhanced dielectric coupling, which strengthens the gate's control over the depletion region at moderate biases. LPCVD Si-rich SiN_x with $\varepsilon_r \approx 8$, extrapolated from reported values [107], was found to be optimal for achieving high tuning range without compromising linearity.

Fluorine and oxygen-related charge states

The introduction of fluorine and oxygen during CF_4 plasma exposure and the subsequent thermal treatment creates donor- and acceptor-like charge states with depth profiles centered near the barrier surface. Simulations show that a higher F^- concentration near the gate region and a distributed O^+ donor profile extending into the

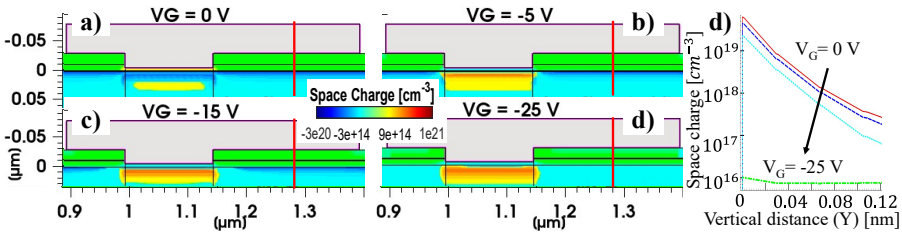


Figure 4.8: Space charges in a 2D countour plot for the device used to simulate the CF_4 strucutre seen in Fig. 4.6, at four different V_G bias points. The cutline (red) provides the charge state with respect to the vertical distance under the field plate for all bias points [C].

AlGaN/GaN interface significantly improve linearity at high reverse bias, Fig. 4.7c. These charge states act quasi-statically under small-signal conditions, modulating the depletion width and effectively "smoothing" the capacitance transition with increasing gate bias.

Notably, the donor-like O^+ states, located primarily near the access region, form a compensating positive charge that helps maintain the 2DEG under the field plate. This prevents abrupt depletion and enables a more uniform capacitance drop across the linear region.

Matching with measurement

When these three mechanisms, field-plate extension, high-ε_r SiN_x, and adjusted F/O charge distributions, are simultaneously implemented in the TCAD models, the simulated C–V profiles exhibit similar profiles as measurement data across all device variants, Fig. 4.6.

This comprehensive modeling approach demonstrates that C–V linearity and tuning range can be co-optimized by combining electrostatic design strategies, such as adjusting the relative permittivity (ε_r) and employing field plates, with controlled charge-state engineering via fluorine plasma and annealing treatments. A detailed analysis of the XPS data (Fig. 3.9a) reveals two distinct oxygen distributions, one at the surface, and another pronounced O peak located below the AlN/GaN interface. Notably, this deeper located O peak was not included in the current simulation, (Fig. 4.6). Incorporating this distribution in future models may be essential for achieving a more realistic representation of the impact that both fluorine and oxygen states have on the C–V characteristics.

Implications for MMIC integration.

The ability to engineer C–V profiles through process-integrated techniques offers a significant advantage for MMIC-compatible varactor design. Since no additional material insertions or post-process steps are required, this method is compatible with existing GaN HEMT fabrication flows. Moreover, the flexibility to tune ε_r through SiN_x stoichiometry and to spatially control plasma-induced charge states via over-etch time and annealing temperature enables a high degree of design freedom. These findings establish a foundation for further transitioning toward fully passive-integrated or MSM topologies with minimal parasitics and improved Q-factors.

Chapter 5

Conclusions and Future Outlook

This thesis has investigated strategies to enhance the performance and reliability of GaN-based high electron mobility transistors (HEMTs) by addressing charge-trapping phenomena, a central limitation for efficiency, linearity, and RF stability in advanced microwave and millimeter-wave applications. The work has encompassed material-level optimisation, process-induced trap management, and design strategies for improved device behaviour, with the aim of informing future generations of high-performance GaN HEMTs.

At the epitaxial level, a systematic study of carbon-doped AlGaN back-barriers demonstrated that careful tuning of the carbon concentration can strengthen two-dimensional electron gas (2DEG) confinement while mitigating current dispersion and short-channel effects. However, excessive doping was found to introduce trap-related degradation, underlining the need for precise control of the carbon profile at the channel/back-barrier interface. These findings emphasise that performance improvements at the material level depend on achieving a balance between beneficial confinement and the suppression of detrimental trap states Paper [A].

In the domain of process-induced trapping, comparative assessments of plasma-based gate processing showed that CF_4-induced states can be partially deactivated by annealing at temperatures up to 600 °C, whereas NF_3 treatments exhibited negligible effects on threshold voltage. Although thermal recovery processes generally improved device performance, operation beyond the optimal annealing temperature introduced adverse voltage shifts and dynamic effects, illustrating the trade-offs inherent in processing optimisations. Thereby providing valuable tools for optimizing a recovery strategy after F plasma treatment of GaN devices paper [B].

The thesis also explored device-level strategies to mitigate trap effects and enhance functional performance. Under cryogenic operation, Fe-related traps in the buffer were found to significantly hinder recovery in low-noise devices. The introduction of source- and drain-connected field plates provided an effective means of alleviating these effects, improving stability for applications such as spaceborne and radio astronomy low-noise amplifiers paper [D]. Furthermore, by deliberately introducing and stabilising charged states during processing, it was possible to realise varactors with exceptionally linear capacitance–voltage characteristics, overcoming a common limitation in GaN-based tunable RF circuits without adding complexity to the fabrication flow paper [C].

Looking forward, the approaches developed here suggest several promising directions for further work. Understanding how both epitaxial design choices—such as controlled carbon doping in back-barriers, and processing techniques, such as fluorine-based plasma treatments combined with optimized annealing. Can be used to minimize trapping effects may accelerate the development of high-frequency GaN HEMTs with improved efficiency, linearity, and reliability for beyond-5G/6G communication systems, advanced radar, and space-qualified electronics. Long-term cryogenic reliability studies that combine the effects of thermal cycling and radiation will be essential for the qualification of spaceborne designs. The demonstrated varactor concept, meanwhile, provides a pathway to more compact and efficient GaN-based monolithic microwave integrated circuits (MMICs) by reducing the reliance on external tuning components. Together, these strategies have the potential to advance GaN HEMT technology toward greater stability, efficiency, and adaptability across terrestrial, aerospace, and deep-space applications.

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