THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

# Downscaled III-Nitride Power HEMTs with Thin GaN Channel Layers: Fabrication, Characterization, and Physics-Based Modeling

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Göteborg, Sweden, 2025

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# Abstract

The unique polarization properties of the III-nitride materials have motivated research into gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) for both power electronics and microwave applications. In these devices, compensation-doped buffer layers and strain-relief layers are typically incorporated into the III-nitride layer stack to reduce off-state currents and to achieve high-crystal-quality GaN and aluminum GaN (AlGaN) layers. However, thin-channel AlGaN/GaN/AlN heterostructures have been presented as a viable alternative to the conventional technology. Among these types of heterostructures, the buffer-free QuanFINE® concept has been suggested. This material uses the AlN nucleation layer and the silicon carbide substrate to improve the electron confinement in the GaN channel layer. In this thesis, high-voltage buffer-free GaN power HEMTs are evaluated. The devices are characterized in terms of their on-state, off-state, and dynamic performance. The impact of critical processing modules—including isolation techniques, dielectrics, and field plate configurations—is investigated. Due to the high electron confinement in the GaN channel layer, a power figure of merit of 729 MW/cm$^2$ at sub-100 nA/mm drain-source current could be achieved, which is comparable to most state-of-the-art technologies reported in the literature.

In contrast to heterostructures with buffer designs, no compensation dopants that can adversely affect the dynamic performance are intentionally incorporated into GaN or AlN layers. However, it is not fully understood how, or to what extent, unintentional defects and impurities will affect the dynamic performance in buffer-free HEMTs. A physics-based technology computer-aided design model is presented to explain the capture and emission processes involved during and after high-voltage conditions. It is hypothesized that a highly ionized donor concentration exists in the GaN layer near the GaN/AlN interface. The trap is thought to be related to defects and impurities that naturally coalesce near the GaN/AlN interface. These states are needed to prevent a semipermanent current reduction after high-voltage conditions. However, it is also shown that the spatial distribution has to be controlled to prevent excessive off-state drain-source leakage currents.

An alternative measurement technique for estimating drain-induced barrier lowering in GaN HEMTs is also suggested. The new method is based on the drain current injection technique (DCIT), which facilitates the measurement of threshold voltage variations at different drain-source voltages. GaN HEMT with short gate lengths ($L_G$) and different epitaxial designs were used to demonstrate the viability of the method. For high-voltage buffer-free HEMTs, the DCIT can be used in the optimization of channel layer thickness and $L_G$ to improve dynamic performance while minimizing the adverse effects of $L_G$ reduction.

Overall, the thesis contributes to the advancement of III-nitride technologies tailored toward power applications through the development of thin-channel buffer-free materials.

**Keywords:** AlGaN/GaN, HEMT, power electronics, high-voltage, breakdown, traps, downscaling, buffer-free, TCAD, simulations, DCIT, SCE, DIBL

# List of Publications

## Appended Publications

This thesis is based on work contained in the following papers:

[A] B. Hult, M. Thorsell, J.T. Chen, N. Rorsman, “High Voltage and Low Leakage GaN-on-SiC MISHEMTs on a “Buffer-free” Heterostructure”, IEEE Electron Device Letters, vol. 43, no. 5, pp. 781-784, May 2022.

[B] B. Hult, M. Thorsell, J.T. Chen, N. Rorsman, “Investigation of Isolation Approaches and the Stoichiometry of $SiN_x$ Passivation Layers in “Buffer-free” AlGaN/GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors”, Physica Status Solidi (a), vol. 220, no. 8, Apr. 2023.

[C] B. Hult, A. Ranjan, L. Zeng, E. Olsson, N. Rorsman, A. Vorobiev, “Investigation of Electrical Breakdown in AlGaN/GaN/AlN HEMTs Through Nanoscale Analysis and Physical Modeling”, *submitted to IEEE Transactions on Device and Materials Reliability, 2025*

[D] B. Hult, J. Bremer, H. Hjelmgren, M. Thorsell, N. Rorsman, “Measurement and Physics-Based Modeling of Traps at the GaN/AlN Interface and their Effect on Drain Current Recovery in Double Heterostructure AlGaN/GaN/AlN HEMTs”, *submitted to IEEE Transactions on Electron Devices, 2025*

[E] B. Hult, J. Bergsten, R. Ferrand-Drake Del Castillo, V. Darakchieva, A. Malmros, H. Hjelmgren, M. Thorsell, N. Rorsman, ”Characterization of Drain-Induced Barrier Lowering in GaN HEMTs Using a Drain Current Injection Technique”, IEEE Transactions on Electron Devices, vol 71, no 12, pp. 7383-7389, Dec. 2024.

# Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

[a] J. Bremer, B. Hult, N. Rorsman, M. Thorsell, "Static and Dynamic Breakdown Characteristics of Microwave GaN HEMTs", *to be submitted to IEEE Transactions on Electron Devices, 2025*

[b] R. Ferrand-Drake Del Castillo, B. Hult, M. Thorsell, N. Rorsman "Linear C–V Characteristics in GaN HEMT Varactors by Fluorine Plasma-Enhanced Gate Engineering", *submitted to IEEE Electron Device Letters, 2025*

[c] A. Papamichail, A. Kakanakova-Georgieva, E. Ö. Sveinbjörnsson, A.R. Persson, B. Hult, N. Rorsman, V. Stanishev, S.P. Le, P.O.Å. Persson, M. Nawaz, J.T. Chen, P.P. Paskov, V. Darakchieva, "Mg-doping and free-hole properties of hot-wall MOCVD GaN", Journal of Applied Physics, vol. 131, no. 18, May 2022

# Abbreviations and Notations

| | |
|---|---|
| GaN | Gallium Nitride |
| AlN | Aluminum Nitride |
| AlGaN | Aluminum Gallium Nitride |
| InAlGaN | Indium Aluminum Gallium Nitride |
| III-nitride | Semiconductor compound materials consisting of at least one group III element and nitrogen |
| HEMT | High Electron Mobility Transistor |
| SiC | Silicon Carbide |
| Si | Silicon |
| $SiN_x$ | Silicon Nitride |
| $Si_3N_4$ | Stoichiometric Silicon Nitride |
| $SiO_x$ | Silicon Oxide |
| $AlO_x$ | Aluminum Oxide |
| DC | Direct Current |
| AC | Alternating Current |
| FET | Field-Effect Transistor |
| BJT | Bipolar Junction Transistor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| IGBT | Insulated-Gate Bipolar Transistor |
| GTO | Gate Turn-Off thyristor |
| MMIC | Monolithic Microwave Integrated Circuit |
| TCAD | Technology Computer-Aided Design |
| DIBL | Drain-Induced Barrier Lowering |
| MOCVD | Metal-Organic Chemical Vapor Deposition |
| MBE | Molecular-Beam Epitaxy |
| 2DEG | Two-Dimensional Electron Gas |
| SRL | Strain-Relief Layer |
| SL | Super Lattice |
| UID | Unintentionally Doped |
| KCL | Kirchhoff's Current Law |
| ICP | Inductively-Coupled Plasma |
| PF | Poole-Frenkel |
| PECVD | Plasma-Enhanced Chemical Vapor Deposition |
| LPCVD | Low-Pressure Chemical Vapor Deposition |
| SC | Standard Clean |
| TLM | Transfer Length Method |
| RTP | Rapid Thermal Processing |
| DCT | Drain Current Transient |
| DCTS | Drain Current Transient Spectroscopy |

| | |
|---|---|
| 2DHG | Two-Dimensional Hole Gas |
| SCE | Short-Channel Effect |
| DCIT | Drain Current Injection Technique |
| SS | Subthreshold Swing |
| SILC | Stress-Induced Leakage Currents |
| SRH | Shockley-Read-Hall |
| SIMS | Secondary Ion Mass Spectroscopy |
| SEM | Scanning Electron Microscope |
| TEM | Transmission Electron Microscope |
| E-mode | Enhancement mode (normally-off) |
| D-mode | Depletion mode (normally-on) |
| I | Current |
| V | Voltage |
| $I_D$, $I_d$ | Drain current |
| $I_G$, $I_g$ | Gate current |
| $I_S$, $I_s$ | Source current |
| $V_{DS}$, $V_{ds}$ | Drain-source voltage |
| $V_{GS}$, $V_{gs}$ | Gate-source voltage |
| $V_{DSq}$, $V_{dsq}$ | Quiescent drain-source voltage |
| $V_{GSq}$, $V_{gsq}$ | Quiescent gate-source voltage |
| $V_{th}$ | Threshold voltage |
| $L_G$, $L_g$ | Gate length |
| $L_{GD}$, $L_{gd}$ | Gate-drain distance |
| $L_{GS}$, $L_{gs}$ | Gate-source distance |
| $L_{GFP}$ | Gate-connected field plate length |
| $L_{SFP}$ | Source-connected field plate length |
| $R_{on}$ | On-state resistance |
| $R_{on,dyn}$ | Dynamic on-state resistance |
| PFOM | Power Figure of Merit |
| $E_{crit}$ | Critical electric field |

# Contents

# Chapter 1

# Introduction

Energy-efficient electronics have become increasingly important as developing countries industrialize and as developed countries shift from the use of fossil fuels to hybrid or fully electric alternatives in automotive transport. The ability to transform electric energy from one form to another with minimal losses is dependent on the performance of the power electronic converters. The magnitude of the losses induced in the circuit is, in turn, heavily dependent on the performance of the converter's solid-state power electronic switching devices, consisting of diodes, field-effect transistors (FETs), thyristors, and bipolar transistors (BJTs). These devices allow for up-conversion or down-conversion of direct current (DC) voltage levels, generation of alternating current (AC) waveforms, and current rectification (Figure 1.1). Power conversion losses are predominantly caused by non-idealities in the switching devices. Although these losses may appear negligible at the level of a single converter, their cumulative effect is significant. When viewed on a global scale, even small increases in efficiency – on the order of just a few percentage points – may lead

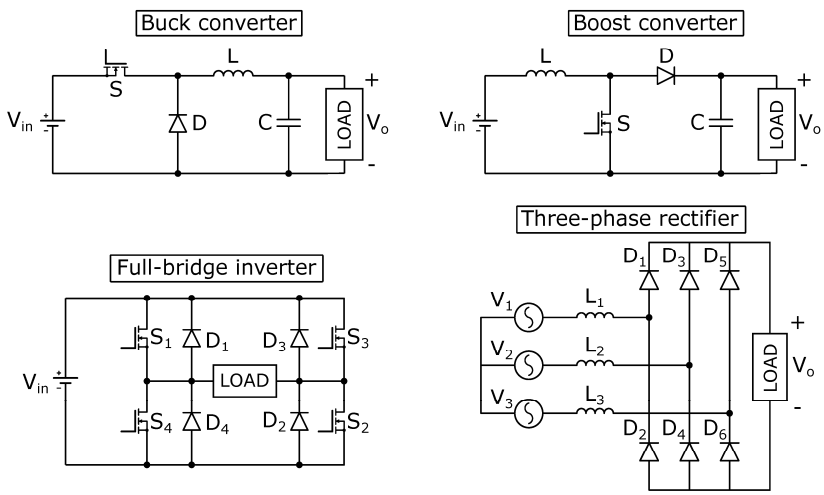


**Figure 1.1.** Simplified circuit diagrams of DC-DC (buck/boost) DC-AC (full-bridge), and AC-DC (three-phase) converters containing solid-state active switches (S) and diodes (D).

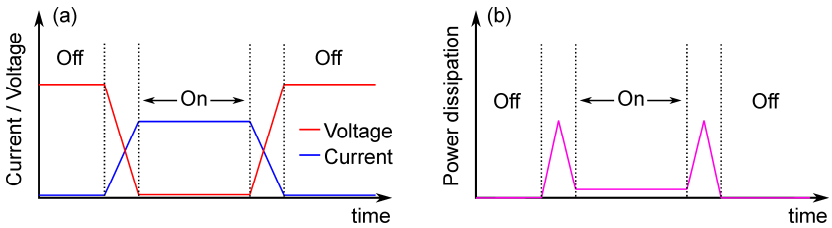


**Figure 1.2.** Simplified (a) current/voltage waveforms and (b) resulting power dissipation of an active power electronic switch.

to annual energy savings in the range of 0.3 to 1.5 PWh[1]. Additionally, improvements in the efficiency of these converters also reduce the requirements of the surrounding cooling system, allowing for a reduction in the size of the whole converter. Improving the performance of the solid-state switching devices is therefore essential.

## 1.1 Material Properties and Device Performance

The losses induced by the switching devices are commonly divided up into two categories: on-state (or conduction) losses, where energy is lost as the switch conducts a high constant current, and switching losses, where the current and voltage waveforms momentarily overlap as the switching device transitions from the on-state to the off-state or vice versa (Figure 1.2a-b). The amount of heat being dissipated in the power electronic device is dependent on the type of switching device, the device design, and the semiconductor material from which the device is made. Semiconductor materials with a higher critical electric field ($E_{crit}$) allow for a reduction in size of the components, and, as a consequence, a reduction of the on-state resistance ($R_{on}$). Switching losses are dependent on the transition period of the current waveforms when the device changes operating state (on-to-off or off-to-on). The transition times[2] are, in turn, affected by intrinsic capacitances and the amount of trapped charges accumulated during the off-state. Additionally, switching losses are also directly proportional to the switching frequency, since every period produces an overlap between the current and voltage waveforms as they change state. Consequently, by minimizing the intrinsic elements in the power switching devices, it is possible to increase the switching frequency while maintaining a high efficiency. Furthermore, when the switching devices are capable of operating at higher frequencies without degrading the efficiency, the size of passive elements in the power electronic circuit can be reduced, leading to an overall size reduction of the power electronic circuit.

Currently, silicon (Si) is the most prevalent type of semiconductor material for power electronic devices in all voltage classes (Figure 1.3a), primarily due to its low manufacturing cost and the ease with which n-type and p-type doping can be

[1] This estimate is based on global electricity consumption of approximately 29,471 TWh in 2023 {Ember, Global Electricity Review 2024}, and assumes a 1% to 5% improvement in average conversion efficiency across power electronic systems.

[2] The transition time includes the rise/fall times of the voltage and currents, the period under which reverse-recovery and voltage/current overshoots occurs.

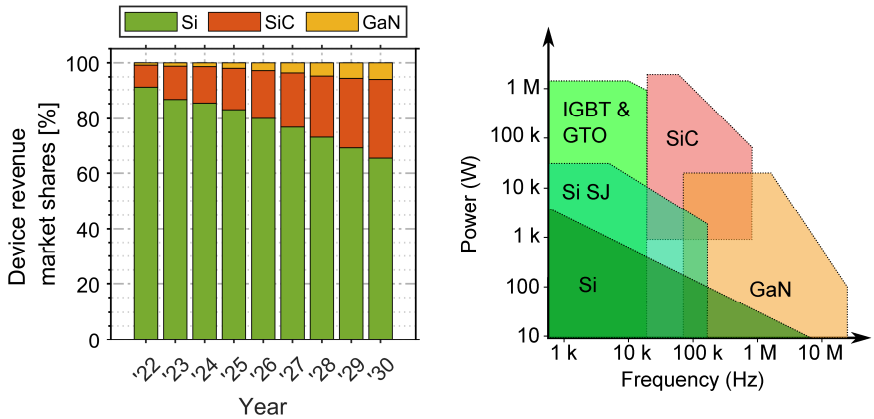


**Figure 1.3.** (a) Current and projected market share of Si, SiC, and GaN power electronic switching devices (plot re-constructed based on data from [3]). (b) Application areas based on power and frequency levels for Si, SiC, and GaN power semiconductor devices (data based on [2]).

achieved. Among active power switching devices, metal-oxide-semiconductor field-effect transistors (MOSFETs) are typically used in low-to-mid voltage classes (20 to 900 V) operating above 20 kHz. At higher voltages (>900 V), insulated-gate bipolar transistors (IGBT) and gate turn-off thyristors (GTO), operating in the 1-20 kHz range, tend to be more common (Figure 3b) [1] [2].

However, Si is not without its disadvantages. Its relatively low bandgap (~1.1 eV) results in a low $E_{crit}$. This becomes particularly problematic in the highest voltage classes, where the drift region size has to be substantially increased to withstand the required off-state voltages. In addition, losses caused by reverse recovery and slow on/off transition times limit the switching frequency in Si-based devices.

## 1.2 Beyond Si-Based Power Electronics

The dominant role of Si in power electronics is being challenged by maturing wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN). These materials exhibit higher critical electric fields (~ 3 MV/cm) and shorter rise/fall times, resulting in reduced component size and improved efficiency, facilitating operations at switching frequencies and power levels well above those of Si-based devices (Figure 1.3b). Silicon carbide pn diodes, MOSFETs, and IGBTs have started to replace their Si counterparts and are becoming more popular (Figure 1.3a).

Gallium nitride (GaN) and its ternary compound, aluminum gallium nitride (AlGaN), offer higher breakdown fields compared to SiC. However, the main advantage of GaN and AlGaN is the ability to fabricate high electron mobility transistors (HEMTs) by forming AlGaN/GaN heterostructures. The two-dimensional gas (2DEG) generated at the AlGaN/GaN interface exhibits electron sheet carrier densities in the $0.5\text{-}1\cdot10^{13}$ $cm^{-2}$ range and with mobilities around 2000 $cm^2/V\cdot s$ [4]. Additionally, the GaN-based HEMTs display negligible reverse recovery charge ($Q_{rr}$), overall lower input capacitance, and lower $R_{on}$-gate charge product ($R_{on}\cdot Q_G$) compared to the SiC

MOSFET in the same voltage class [5], enabling even higher switching frequencies (Figure 3b). Currently, GaN-based HEMTs are typically used in the ≤650 V classes, whereas SiC MOSFETs are common in both the 650 V and 1200 V classes. However, with growing interest and improvements in performance and reliability, GaN-based HEMTs may also become a viable option for higher voltage classes (≥1200 V).

Currently, AlGaN/GaN heterostructures are typically grown on Si. However, with the increased use of SiC power devices, GaN-on-SiC may become a more viable option due to the superior thermal and insulating properties of SiC. Additionally, the improved lattice match between GaN and SiC allows for a reduced epitaxial design complexity, which reduces overall growth time of the III-nitride layers.

## 1.3 Previous WBG Device Research at Chalmers

Historically, research on III-nitride-based HEMTs at Chalmers has primarily focused on studying the impact of different epitaxial designs and critical device fabrication parameters to improve the device performance of microwave devices [6]–[8]. Investing resources into research of power III-nitride HEMTs is not only of interest for studying how epitaxial designs and device fabrication parameters can be optimized for these types of devices, but also for bridging the existing expertise of microwave electronic engineering with power electronic device engineering. On a circuit level, this may involve future integration of monolithic power electronic converter designs into monolithic microwave integrated circuit (MMIC) designs. On a device level, an increased knowledge of device performance and reliability during/after high electric field conditions is also useful in the design of microwave devices with improved breakdown voltage, reduced off-state leakage currents, and reduced performance degradation due to trapping effects. This requires an in-depth understanding of the physics during and after high-voltage stresses, as well as the effect of different epitaxial design parameters (e.g., layer thicknesses and doping concentrations) and device design parameters on the off-state performance. Moreover, the knowledge and experience within the field of power electronic device engineering may lead to new research directions and increased collaborations with other universities and industrial partners.

## 1.4 Outline of the Thesis

The thesis is structured as follows: In Chapter 2, a case will be made for the use of the buffer-free GaN-on-SiC HEMTs for power electronics, including a review and comparison of current and previously used epitaxial designs, a description of the device fabrication process, as well as a discussion of critical process parameters. In Chapter 3, a hypothesis will be presented of the trap/de-trap process in the buffer-free GaN HEMTs described in Chapter 2. This chapter will include an in-depth description of the technology computer-aided design (TCAD) model used to test the hypothesis. In Chapter 4, a new technique for characterizing threshold voltage ($V_{th}$) shifts and drain-induced barrier lower (DIBL) in GaN HEMT will be presented. This technique is of interest when the gate length reduction (lateral downscaling) is critical to improve the high-frequency performance in power electronic HEMTs, as well as in GaN HEMTs tailored towards microwave power amplifier applications.

# Chapter 2

# Buffer-Free III-Nitride Power Electronic HEMTs

Commercial GaN HEMTs are normally grown on Si due to its relatively low cost. However, to enable off-state operation in the voltage classes above 1200 V, complex heteroepitaxial structures involving superlattices, step-graded AlGaN layers, and thick, highly resistive GaN buffer layers need to be employed to suppress both lateral leakage and vertical currents through the substrate. This has been one of the key constraints limiting commercial GaN HEMTs below 1200 V.

This chapter explores the viability of the buffer-free AlGaN/GaN heterostructure on a semi-insulating 4H-SiC substrate (QuanFINE®) as a platform for power electronic HEMTs. The unique feature in this type of heterostructure is that the substrate and the nucleation layer replace the role of the buffer layer as a means to reduce lateral and vertical off-state leakage currents. A comprehensive review of existing buffer technologies will be presented and contrasted with the buffer-free design.

## 2.1 Substrate Alternatives

When GaN and AlGaN layers are grown on a substrate using metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), the type of substrate and its surface properties are of critical importance. Lattice mismatches and differences in the thermal expansion coefficients between the epitaxial layer(s) and the substrate tend to result in high concentrations of defects, such as vacancies, interstitials, anti-sites, dislocations, and stacking faults [9]. Similar lattice constants between the grown III-nitride layers and the substrate are preferred, as this lowers the requirements of the nucleation layer and subsequently grown strain-relief layers (SRLs).

Moreover, for power electronics, the intrinsic carrier concentration of the substrate can affect the off-state currents. This particularly becomes a problem when the backside of the substrate is grounded. Off-state currents between the drain terminal and the substrate can become unacceptably high and also lead to a premature

**Table 2.1.** Material properties and relative cost of substrates for GaN growth.

| Parameter | GaN | AlN | 4H-SiC | Si | Sapphire ($\alpha$-$Al_2O_3$) |
|---|---|---|---|---|---|
| Bandgap (eV) | 3.44 | 6.2 | 3.26 | 1.12 | 8.1-8.6 |
| Thermal conductivity[b] (W/cm·K) | 1.23-2.1 | 2.85 | 3.7 | 1.56 | 0.23-0.32 |
| Thermal expansion coefficient[a] ($\cdot 10^{-6}$ $K^{-1}$) | 6.20 | 2.90-5.27 | 4.06 | 2.61 | 5.0[c] |
| Lattice constant[a] (Å) | 3.19 | 3.11 | 3.07 | 5.43 | 4.7-4.76 |
| Relative cost | high | high | medium[*] high[**] | low | low |
| References | [10]–[12] | [10] [12] | [10] [13] [14] | [10] | [10] [15] |

[*] n-type,[**] high-purity
[a] || a-axis, [b] || c-axis, [c] ⊥ c-axis

avalanche breakdown. This can be mitigated by including thick, highly resistive layers in the heterostructure.

Wafer cost is also a factor that has to be considered when selecting a substrate material. Although GaN, AlN, and SiC substrates are more suitable for growth in terms of lattice match and thermal expansion coefficient, Si and sapphire are currently preferred due to their lower cost (Table 2.1). Sapphire has a higher bandgap than Si, but also exhibits a low thermal conductivity. Additionally, GaN epitaxial quality tends to be worse on sapphire substrates. For these reasons, Si has become the most commonly used substrate material for GaN HEMTs in consumer-based electronics. However, due to the emergence of SiC-based power electronic devices in recent years, the manufacturing cost of n-type SiC substrates has substantially decreased, and the cost of high-purity SiC substrates is expected to follow. Additionally, the superior thermal conductivity of SiC substrates can facilitate more effective vertical heat transport generated close to the 2DEG down to the heatsink located at the backside of the substrate.

## 2.2 III-Nitride Epitaxial Design

### Nucleation Layer

Growing high-quality, crack-free GaN layers directly on foreign substrates is generally difficult due to large lattice and thermal mismatches between the two materials (Table 2.1). The high density of dislocations and point-defects formed in the GaN as a result of the direct growth on the substrate can negatively impact the electron mobility [16] [17], max drain current [18], leakage [19], and recovery behavior in GaN HEMTs [18]. It is therefore necessary to introduce an intermediary layer whose function is to promote the subsequent growth of high-quality GaN (Figure 2.2.1a). In 1985, Amano et. al proposed the use of AlN as an intermediate layer on sapphire substrates [20], which later became a widely-used material for GaN growth on foreign substrates in general. At present, AlN nucleation layers are successfully grown with thickness in the 50-200 nm range [21]–[24].

Even though AlN facilitates the growth of GaN, the type of substrate used will significantly affect the number of defects in the subsequent GaN epi-layer.

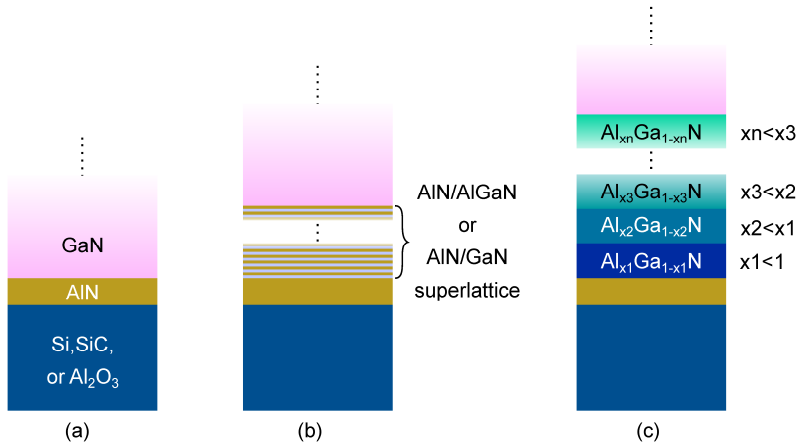


**Figure 2.2.1.** Schematics showing heteroepitaxial growth of GaN on foreign substrates with an AlN nucleation layer, (a) without additional interlayers, (b) with superlattice, and (c) with step-graded AlGaN layers. Layer thicknesses are not to scale.

Dislocation densities in the high-$10^7$ $cm^{-2}$ to low-$10^8$ $cm^{-2}$ range can be obtained for heterostructures grown on 4H-SiC [25]–[27], whereas GaN-on-Si displays densities in the high-$10^8$ $cm^{-2}$ to low-$10^9$ $cm^{-2}$ range[3] [21] [25] [28] [29]. The dislocation-related defects tend to coalesce around the GaN/AlN interface and decrease in concentration further into the GaN layer. Suppression of dislocations can be achieved by incorporating additional layers between the nucleation layer and the channel.

## Strain-Relief Layers

One commonly used technique to further reduce the number of defects formed as a result of the incompatible crystal structures of the GaN layers and the foreign substrates is to include an SRL into the heterostructure. This can consist of an AlN/GaN or AlN/AlGaN superlattice (SL) [30]–[33] (Figure 2.2.1b), a sequence of $Al_xGa_{1-x}N$ layers with a step-like variation in the Al mole fraction [34]–[37] (Figure 2.2.1c), or a combination of a step-like AlGaN profile and a SL [36]. In addition to promoting higher quality GaN growth, it has been demonstrated that SLs can have a positive effect on the dynamic $R_{on}$ ($R_{on,dyn}$) and act as a voltage blocking layer to increase the breakdown voltage in GaN-on-Si HEMTs [31]. However, to reach vertical breakdown voltages above 1000 V, the total thickness of the SL stack needs to be at least 4 µm [31] [38] [39].

## GaN Buffer Layers with Compensation Doping

GaN HEMTs fabricated on an epitaxial heterostructure without any resistive layers between the active (2DEG) and the substrate will generally exhibit a large punch-through current and, in the case of GaN-on-Si or GaN-on-SiC (n-type), a large substrate current at high-voltage off-state conditions (Figure 2.2.2a). The low resistivity is caused by the unintentional introduction of oxygen and nitrogen

[3] Assuming that GaN is grown directly on the AlN nucleation layer without intermediate layer(s).

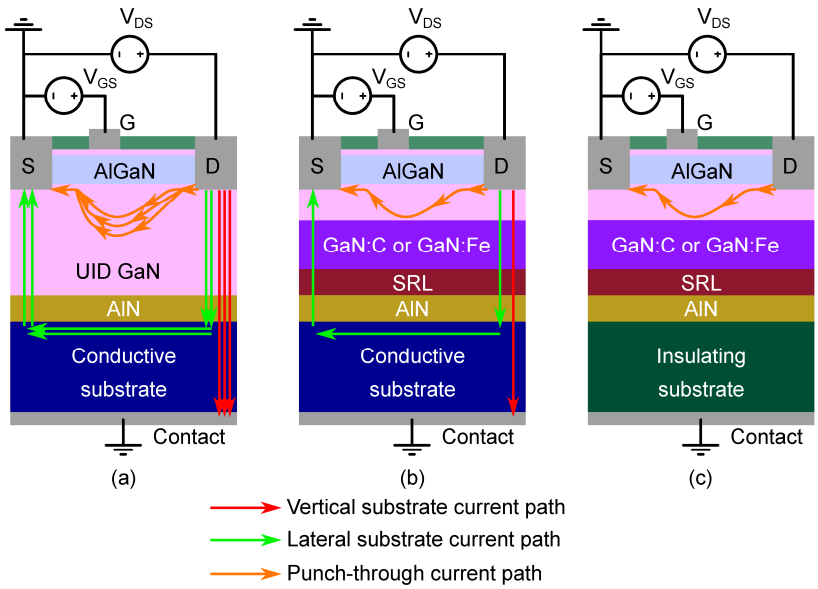


**Figure 2.2.2.** Schematic showing the different drain-source leakage paths (arrows) for a III-nitride heterostructure grown on a foreign substrate, (a) without a buffer layer and with a conductive substrate, (b) with a buffer layer and with a conductive substrate, and (c) with a buffer layer and a (semi-)insulating substrate. Multiple arrows indicate a larger current. Layer thicknesses are not to scale.

vacancies into the GaN crystal during the growth process. These defects have been shown to act as shallow donors [40] [41], which would produce an excess electron concentration when incorporated into GaN.

In order to reduce high substrate leakage currents during off-state conditions, it is common to grow a thick GaN buffer layer between the SRL or nucleation layer and the 2DEG. By intentionally doping the buffer layer with an acceptor-type dopant, it is possible to reduce the vertical off-state current levels (Figure 2.2.2b). Moreover, the high resistivity also reduces punch-through currents underneath the gate region when the device operates in high off-state voltage conditions (Figure 2.2.2c). To date, the most commonly used compensating dopants in GaN are C and Fe.

## Carbon-Doped Buffer Layers

Under optimized MOCVD growth conditions[4], carbon preferentially substitutes nitrogen ($C_N$) rather than gallium ($C_{Ga}$). An excess $C_N$ concentration is preferred since $C_N$ creates a deep acceptor-like state with an ionization energy of around 0.9 eV above the valence band, while $C_{Ga}$ forms a shallow donor state [42]. Compensating both the $C_{Ga}$ and the residual n-type dopants to obtain lateral breakdown fields above 100 V/µm requires C concentrations in the order of $10^{19}$ $cm^{-3}$ [43] [44]. Carbon concentrations at these levels display a $R_{on,dyn}$ increase by a factor of 2 [43] [44]. However, Uren et al. developed a model to explain and predict the trap behavior in GaN-on-Si HEMTs with C-doped buffers [45], where it was suggested that $R_{on,dyn}$

[4] In terms of Ga-to-N precursor gas flow ratio, or carbon precursor gas flow and/or the growth temperature.

can be mitigated by tuning the conductivity in the unintentionally doped (UID) GaN layer. This was also corroborated by Moens et al. [46], who showed that $R_{on,dyn}$ below 10% at 650 V can be achieved by optimizing the UID layer conductivity.

### Iron-Doped Buffer Layers

Iron primarily substitutes for the Ga atoms ($Fe_{Ga}$) in MOCVD-grown GaN [47]. In contrast to $C_N$ defects, $Fe_{Ga}$ tends to form acceptor states 0.5-0.7 eV from the conduction band [47] [48] [49]. Simulations of GaN HEMTs with Fe and C doped buffers have shown that Fe may be superior in terms of $R_{on,dyn}$ [50], unless the UID GaN layer conductivity is optimized to suppress significant increases in $R_{on,dyn}$. Improved dynamic performance of Fe-doped buffers was also demonstrated by Hilt et al. [51], who showed that $R_{on,dyn}$ increased by only 1.2-1.5, compared to 3-4 for GaN with a C-doped buffer. However, Fe-doped buffer layers exhibit less favorable lateral breakdown fields relative to C-doped buffers. Overall, C-doped buffer layers are preferred for power electronic GaN HEMTs.

## Buffer-Free Heterostructures

An alternative MOCVD growth method for AlN layers on on-axis semi-insulating (SI) 4H-SiC substrates was presented in 2018-2019 by Lu and Chen et al. [52] [53], that allows for the deposition of <500 nm UID GaN layers directly on the nucleation layer with dislocation densities in the low $10^8$ range, without incorporating any intermediate strain-relief layers or thick buffer layers (Figure 2.2.3a). The advantage of this heterostructure is that the AlN layer and the insulating SiC substrate act as a back-barrier, lowering the punch-through current in the GaN layer. Because of the improved electron confinement, lateral off-state currents could possibly be suppressed without adding dopants that simultaneously increase the $R_{on,dyn}$. In addition, the semi-insulating properties of the 4H-SiC substrate are capable of maintaining vertical currents well below 1 µA/mm$^2$ up to at least 3000 V (Figure 2.2.3b). In [Paper A], [Paper B], [Paper C], and [Paper D], the dynamic and off-state performance of GaN metal-insulator-semiconductor (MIS) HEMTs processed on this heterostructure were investigated. The following section will discuss the impact of critical device processing parameters in these devices.

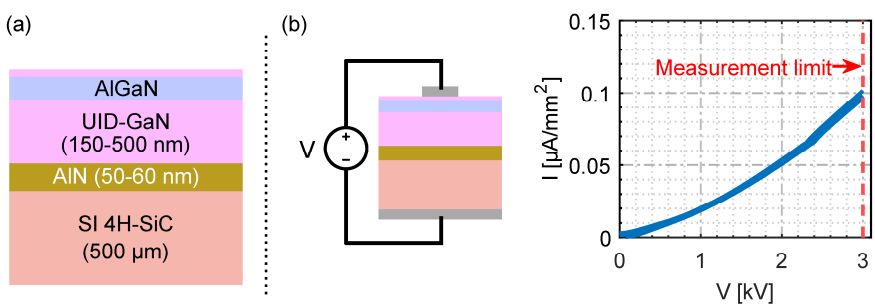


**Figure 2.2.3.** (a) Schematic showing the epitaxial structure of the buffer-free design, and (b) two-terminal (vertical) isolation I-V characteristics of a semi-insulating 4H-SiC substrate. Layer thicknesses are not to scale.

## 2.3 GaN HEMT Device Design and Fabrication

### 2.3.1 Normally-On versus Normally-Off Transistors

GaN HEMTs naturally exhibit normally-on (D-mode) behavior since the 2DEG is present at thermal equilibrium. Implementing a normally-on switch in a power electronic converter entails a greater risk since the switch can short-circuit the power source (e.g., a battery) if the gate drive suddenly fails. In order to prevent this, normally-on GaN HEMTs can be placed in a cascode topology, in which the HEMT is placed in series with a normally-off Si MOSFET (Figure 2.3.1a) [54]. With the source of the MOSFET connected to the gate of the HEMT, the potential at the drain (source on the HEMT) will be higher than the HEMT's gate potential, effectively producing normally-off behavior.

Normally-off (E-mode) operation can also be achieved in GaN HEMTs through processing and epitaxial design, and is generally more desirable than normally-on HEMTs (in cascode topology) since it reduces size and complexity of the converter as a whole (Figure 2.3.1b). However, the device processing is more complicated, and achieving normally-off behavior without time-dependent degradation effects of the gate current ($I_G$), and with a stable $V_{th}$, is generally difficult [55].

Normally-on based GaN HEMTs facilitate the comparison of the performance of different types of epitaxial heterostructures in terms of breakdown voltage, off-state currents, trap behavior, and $R_{on,dyn}$. Additionally, depositing a dielectric between the gate metal and the GaN cap to form a MIS structure simplifies the material evaluation of the semiconductor further, since it allows for the fabrication of devices with gate currents below 1 µA/mm [56].

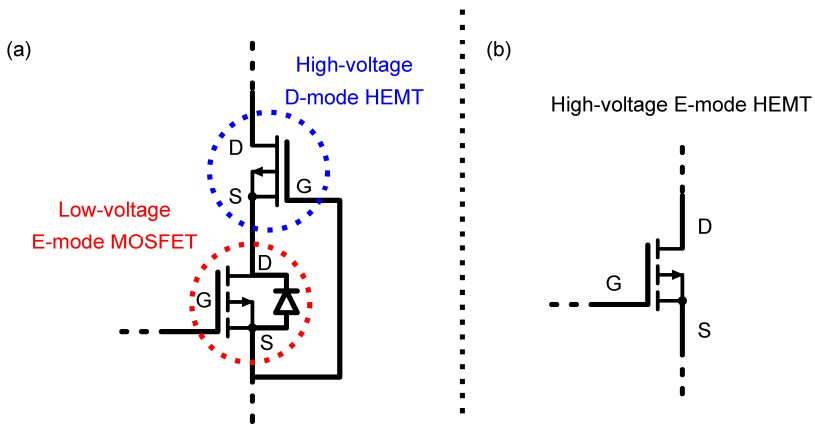


**Figure 2.3.1.** Circuit diagrams showing the two options for achieving normally-off behavior of GaN HEMTs with (a) cascode topology, and (b) with an intrinsic normally-off HEMT without cascode topology.

## 2.3.2 Lateral Isolation Techniques

Electrically isolating the areas surrounding the active regions is crucial for high voltage operation since currents between the drain and source can circumvent the gate terminal laterally (Figure 2.3.2a), leading to an excessive off-state drain-source current. For GaN HEMTs, there are primarily two device processing techniques to achieve lateral electrical isolation: mesa dry etching and ion implantation.

### Mesa Isolation

For III-nitride materials, a Cl-based inductively coupled plasma (ICP) etch process is typically used to physically and chemically remove AlGaN and GaN around the active areas [57]. This completely removes the 2DEG from these areas, and the drain-source current is instead limited by the bulk resistivity of the material where the etching stops, which is usually the buffer layer. In the buffer-free heterostructure, the UID GaN channel layer is thin enough to allow for etching down to the SiC substrate (Figure 2.3.2b), enabling use of the substrate's improved insulating properties (Figure 2.3.2c). Stopping the etch inside the GaN layer tends to result in much higher leakage current, which limits the off-state voltage below 500 V, most likely due to the unintentional n-type dopants (e.g., oxygen). The downside of using the mesa etch technique is that the plasma creates etch-induced defects (e.g., N vacancies) [58] or unwanted dopants that can form alternative current paths. The formation of these leakage paths is highly dependent on the hard mask used during the etching process and on the dry etch settings [59]. Additional mitigation of etch-induced defects can be achieved through wet etch treatments using tetramethylammonium hydroxide [7] [59] [60] or ammonium sulfide [61]. Exposing the surface to a nitrogen plasma [62] [63] and annealing at high temperatures in a nitrogen environment has also been suggested [61].

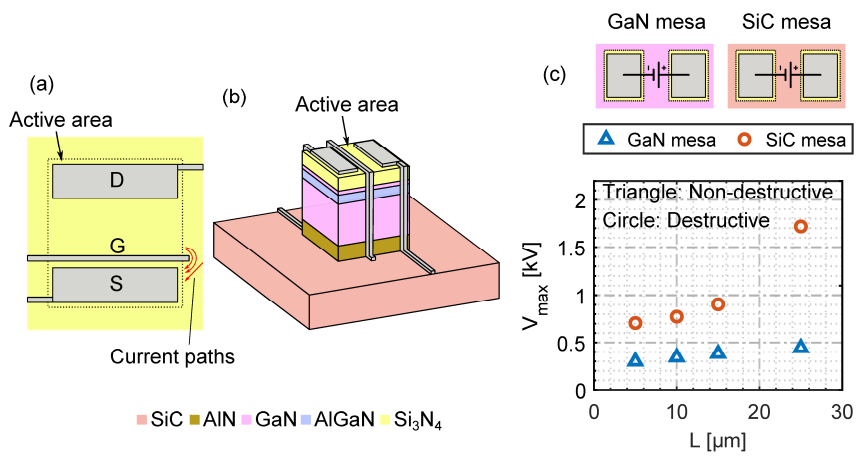


**Figure 2.3.2.** (a) Simplified schematic of a GaN-based transistor (top view perspective) indicating potential lateral current paths between drain (D) and source (S) terminals. (b) Bird's eye view of a buffer-free AlGaN/GaN transistor where the III-nitride materials have been etched away around the active (device) area. (c) Top-view schematic of two-terminal isolation structures where the active III-nitride areas have been etched into the GaN layer (top left) and SiC substrate (top right). The bottom figure in (c) shows the max voltage that can be applied between the contacts of the two types of mesa isolation structures against contact separation (L).

## Implantation Isolation

The electrical properties of the semiconductor material can be altered by accelerating ions using an electric field with voltages that typically span from 10 kV to several 100 kV (Table 2.2). The material exposed to the accelerated ions is damaged, but is not removed as in the mesa isolation techniques, resulting in a planar surface topology (Figure 2.3.3). The damage created by the accelerated ions results in the formation of defect states in the band gap, which can capture free electrons and reduce the mobility [71]. Increasing the implantation dose generally increases the resistivity since the acceptor-type defect density increases. However, at an implantation species concentration in the range of $4 \cdot 10^{18}$ to $5 \cdot 10^{19}$ $cm^{-3}$, the resistivity can start to decrease as a result of increased hopping conduction [64]. In III-nitride materials, the defect states can be associated with vacancies, anti-sites, and interstitials formed by Al, Ga, N, or by the implantation species.

Additionally, the ions used can have an impact on the type and the number of defects formed in the III-nitride crystals. As a result, a variety of different resistivities and sheet resistance values have been reported in the literature (Table 2.2). In addition to

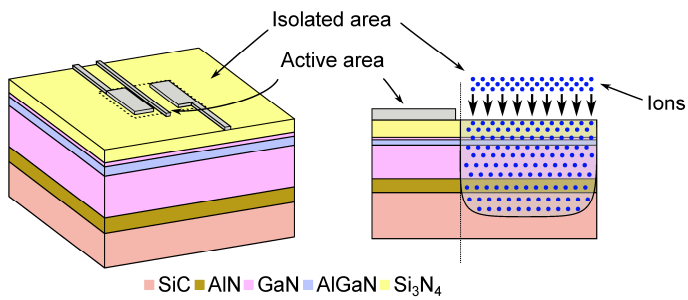


**Figure 2.3.3.** Bird's eye view (left) and side view (right) of a (simplified) buffer-free AlGaN/GaN HEMT using a planar, implantation isolation technique to define the active areas.

**Table 2.2.** Examples of ion species for implantation in GaN, including typical implantation energies, implantation doses, optimal annealing temperatures ($T_{opt}$), as well as resulting low-field sheet resistance/resistivity values.

| Ion | Energies (keV) | Doses ($cm^{-2}$) | $T_{opt}$ (°C) | $R_{sh}$ (Ω/sq) or $\rho$ (Ω·cm) | Reference |
|---|---|---|---|---|---|
| $He^+$ | 20, 90, 180 | 1.8, 3, 3.6 ($\cdot 10^{12}$) | 250-300 | $\rho = 10^{10}$-$10^{11}$ | [64] |
| $H^+$ | 10, 40, 90 | 1.1, 1.8, 2.3 ($\cdot 10^{12}$) | 100-200 | $\rho = 10^{10}$-$10^{11}$ | [64] |
| $Xe^+$ | 5, 15, 30, 45, 100 | 5, 1, 1, 1, 1 ($\cdot 10^{13}$) | 500-800 | $R_{sh} = 9.4 \cdot 10^9$ | [65] |
| $N^+$ | 30, 160, 400 | 6, 18, 25 ($\cdot 10^{12}$) | 350-600 | $R_{sh} = 3$-$9 \cdot 10^{11}$ | [66] |
| $Zn^+$ | 30, 80, 175, 350 | 1.9, 3.8, 3.5, 13 ($\cdot 10^{13}$) | 400-600 | $R_{sh} = 2.2 \cdot 10^{13}$ | [67] |
| $O^+$ | 25, 50, 75 | $5 \cdot 10^{14}$ (for each energy) | ~400 | $R_{sh} = 7 \cdot 10^{12}$ | [68] |
| $Fe^+$ | 40, 83, 200 | 1, 2, 9.2 ($\cdot 10^{13}$) | 400-600 | $R_{sh} = 2.7 \cdot 10^{15}$ | [69] |
| $C^+$ | 250, 520 | 4, 5 ($\cdot 10^{13}$) | ~400 | $R_{sh} = 6.2 \cdot 10^{13}$ | [70] |
| $Al^+$ | 300, 800 | 1, 1.5, ($\cdot 10^{13}$) | ~400 | $R_{sh} = 1.2 \cdot 10^{14}$ | [70] |

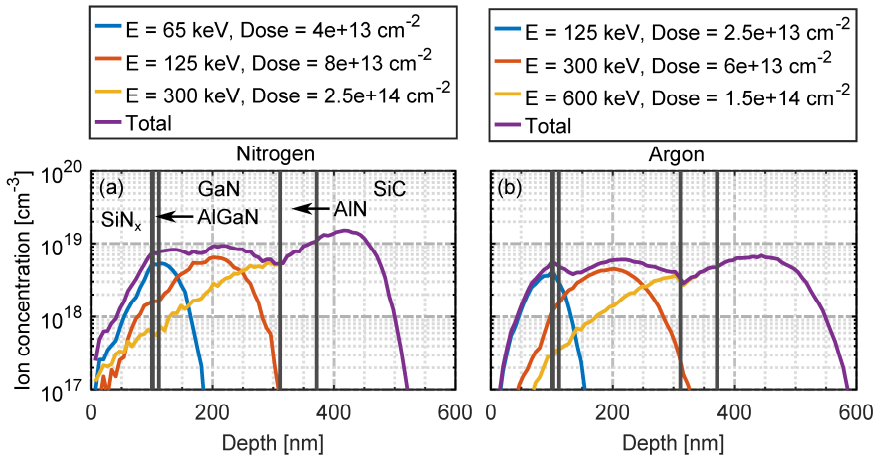


**Figure 2.3.4.** Simulated implantation profile of (a) nitrogen ions, and (b) argon ions on a buffer-free heterostructure using the Stopping Range of Ions in Matter (SRIM) software [74].

the implantation species listed above, heavy noble gases such as Ar and Kr have been studied as well [72] [73], although reports of the sheet resistance values are scarce.

The defects induced by the high-energy ions normally result in a conductive behavior that is characterized by the Poole-Frenkel (PF) mechanism [66] [67]. The current can therefore become exponentially dependent on the electric field and limit the maximum off-state operating voltage. However, this current component can be reduced through post-implantation annealing [64]. In order to improve off-state performance, implantation dose and annealing temperature have to be carefully balanced to maximize the lateral resistivity.

In buffer-free GaN HEMTs, the whole III-nitride stack can easily be electrically isolated using nitrogen or argon (Figure 2.3.4a-b), since the GaN layer is 200-500 nm thin. Nitrogen tends to be more effective in suppressing leakage currents compared to Ar (Figure 2.3.5c-d). Both species lead to an increase in the two-terminal (isolation) voltage at 1 µA/mm after post-implantation anneal. However, the Ar-implanted samples cannot reach voltages over 1 kV regardless of contact separation.

Notably, N and Ar seem to both be effective in isolating the III-nitride stack for GaN-on-Si epitaxial heterostructures (Figure 2.3.5c-d). This indicates that the AlN nucleation layer or the SiC substrate has been insufficiently isolated in the buffer-free samples when using Ar. The Ar concentrations (Figure 2.3.4b) may, in this case, be too high, leading to a reduction in the resistivity due to an excessive hopping conduction. However, in both the buffer-free and GaN-on-Si samples, nitrogen reaches the maximum resistivity after annealing at 500 °C. By contrast, it is less clear if 600 °C is sufficient to achieve the highest resistivity for Ar in the buffer-free samples. The saturation in max voltage for the GaN-on-Si samples is likely due to leakage through the Si substrate or one of the non-implanted layers in the III-nitride stack.

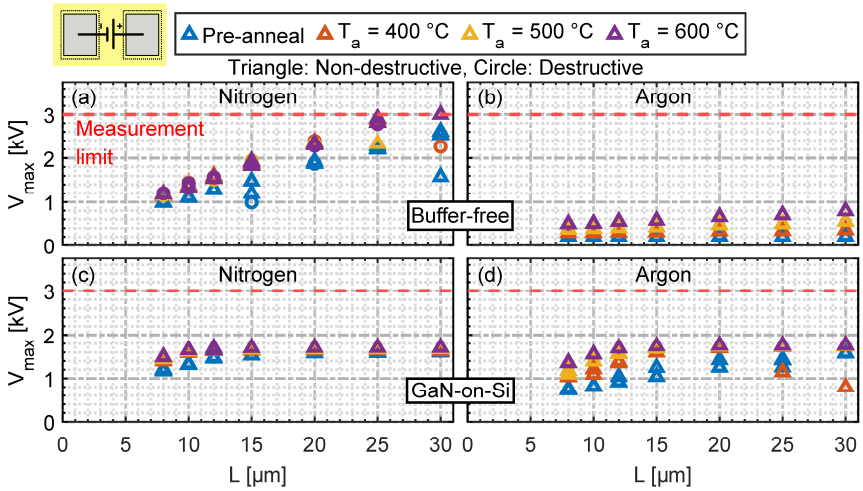


**Figure 2.3.5.** Schematic of the two-terminal isolation structure using the planar isolation technique (top left of (a)), and the maximum voltage that can be applied between the two contacts at 1 µA/mm using (a), (c) nitrogen and (b), (d) argon implantation on buffer-free heterostructures (a-b) and a GaN-on-Si heterostructure (c-d) at varying contact separations. Substrate is left floating. Measurements were performed on four isolation structures for each contact length at different annealing temperatures ($T_a$).

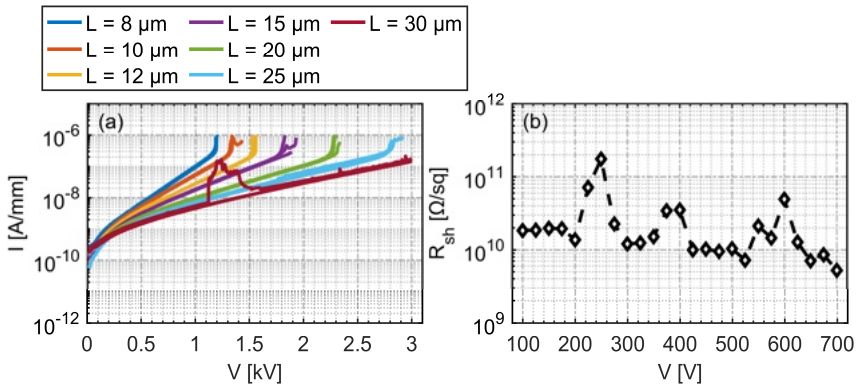


**Figure 2.3.6.** High-voltage two-terminal measurements on a buffer-free heterostructure with nitrogen implantation, where (a) displays the I-V characteristics for the different contact separations, and (b) shows the sheet resistance obtained at different voltages.

The I-V characteristics in the nitrogen-implanted samples show an exponential square root dependence on the applied voltage for most of the measurements (Figure 2.3.6a), which indicates that the primary leakage mechanism is Poole-Frenkel conduction, similar to what has been described in [66] [67]. However, close to the current compliance (1 µA/mm), the current starts to increase rapidly, possibly due to impact ionization. In several cases, the two-terminal device broke down destructively before the PF leakage current exceeded the current compliance. Sheet resistances extracted at 100 V to 700 V tend to be in the upper $10^9$ Ω/sq to the lower $10^{11}$ Ω/sq range (Figure 2.3.6b), placing them at the lower end of values commonly reported in the literature (Table 2.2). Further optimization of implantation doses, energies, and post-implantation annealing schemes could therefore be implemented to improve the lateral isolation.

Based on the mesa isolation tests and the ion implantation tests, it is clear that nitrogen implantation is the preferred choice for the buffer-free heterostructures. Because of this, nitrogen implantation was used in [Paper A-D].

### 2.3.3 Passivation Layer

The density and energetic distribution of states at III-nitride surface states are heavily influenced by the presence of external contaminants, such as oxygen and organic compounds [75]. Adsorption of this type of contaminants can have negative ramifications for the on-state performance of the HEMT, since the surface charge state affects the 2DEG sheet carrier density. Furthermore, the surface states affect the current recovery behavior when electrons are injected from the gate metal during high-voltage off-state stress conditions [76]. It is therefore necessary to deposit a dielectric that (a) protects the surface from external contaminants, (b) does not itself negatively impact the surface charge state during deposition of the dielectric, and (c) minimizes current recovery after off-state stress. Additionally, in power electronic HEMTs, it is important that the dielectric exhibits high resistivity and is capable of withstanding high electric fields over prolonged periods.

Silicon nitride ($SiN_x$) is preferred over oxides (e.g., $SiO_x$ or $AlO_x$) since it minimizes surface oxidation – especially when combined with surface pre-treatments [77] – and increases the 2DEG carrier concentration [78]. The $SiN_x$ layers can either be deposited in-situ after growing the III-nitride heterostructure in the MOCVD reactor, or ex-situ using plasma-enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD). In-situ $SiN_x$ can be deposited without exposure to air, leading to an $SiN_x$/GaN interface with negligible amounts of oxygen and ambient organic or metallic contaminants. Moreover, in-situ growth enables a reduction of interface state densities down to ~$10^{10}$ $cm^{-2}{\cdot}eV^{-1}$ [79], and is effective in suppressing off-state currents, and improving $R_{on,dyn}$ [80]. However, optimizing the deposition parameters of in-situ $SiN_x$ requires growth of the entire III-nitride heterostructure for each test, making evaluations of the film quality expensive and time-consuming. In contrast, ex-situ growth methods have been used extensively for the past two decades [81] [82], and are generally easier to evaluate. LPCVD is the preferred choice over PECVD films, due to its superior interface quality, lower surface state densities, and lower leakage currents [83] [84]. Additionally, in PECVD, the III-nitride surface is exposed to a plasma during deposition, with increased risk of implantation and plasma damage to the surface.

The Si content of $SiN_x$ films serves several key roles in the function of GaN HEMTs. Si-rich films have been shown to reduce $R_{on,dyn,}$ and current collapse [85]. However, higher Si content also reduces resistivity in $SiN_x$ films. In [Paper A] and [Paper B], it is demonstrated that LPCVD-grown, stoichiometric $SiN_x$ ($Si_3N_4$) gate dielectric and passivation layer can suppress off-state drain leakage currents below 100 nA/mm over 1000 V in the buffer-free AlGaN/GaN HEMTs, with a small impact on the $R_{on,dyn}$ up to 240 V. Additionally, devices with a Si-rich passivation resulted in similar $R_{on,dyn}$. The primary leakage mechanism at these voltages is drain-to-source current, showing that the AlN nucleation layer and the SiC substrate are effective in suppressing lateral punch-through currents underneath the gate.

The dielectrics also play an important role in shaping the electric field profile between the gate and the drain. The thickness and the dielectric constant will affect the ability of the field plates to deplete the 2DEG. Additionally, leakage through the dielectrics also affects the occupancy of the surface donor states, which, in turn, affects the extent to which the 2DEG is depleted. This aspect will be discussed in more detail in Chapter 3.

### 2.3.4 Field Plate Engineering

In power electronic devices, the electric field tends to be highly concentrated at the corners and edges of the terminal contacts. GaN HEMTs usually display one field peak at the edge of the gate metal and one at the edge of the drain metal (Figure 2.3.7a). The high electric field may cause an avalanche breakdown at a voltage which is significantly lower than in the ideal case when the field is evenly distributed between the gate and drain contacts. Alternatively, in MISHEMTs, the high field peak near the gate terminal can easily lead to irreversible dielectric failure, resulting in a shorted path between the gate and the drain terminals. To solve these problems, the metal edges have to be correctly terminated. This can be achieved through the use of field plates (Figure 2.3.7b-d). Gate-connected field plates extend the gate metal towards the drain on top of the passivation layer. They can consist of a single metal extension (Figure 2.3.7b) [86] or several extensions with a staircase profile (Figure 2.3.7c) [87]. For each edge added to the field plate metal, an electric field peak is formed inside the AlGaN barrier and GaN layers that laterally distribute the electric field between the gate edge and the drain (Figure 2.3.7b) during high-

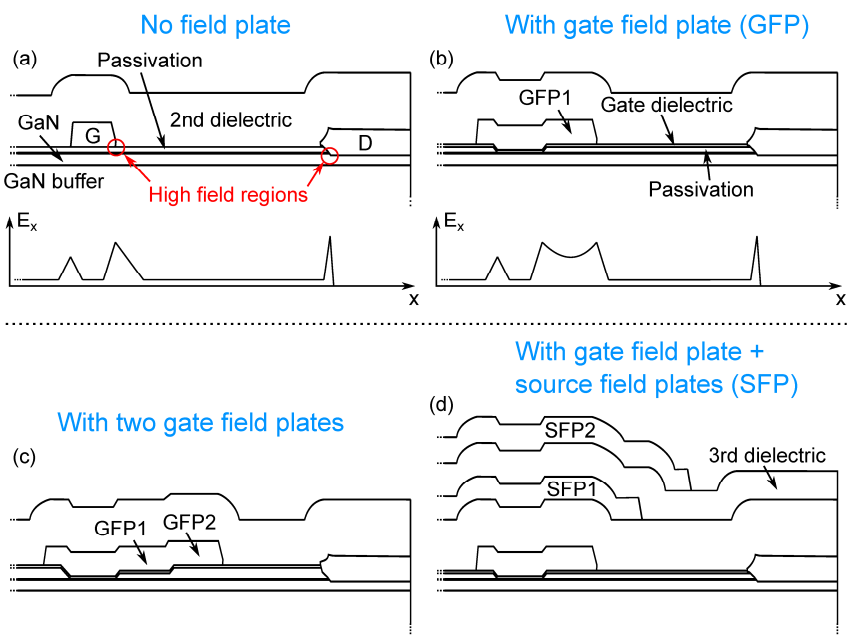


**Figure 2.3.7.** Simplified schematics showing the gate-drain region of a MISHEMT (a) without a field plate, (b) with a single gate-connected field plate, (c) with a double staircase gate-connected field plate, and (d) with gate and source-connected field plates. Figures (a) and (b) also show a (simplified) lateral electric field profile during the off-state at the AlGaN/GaN interface.

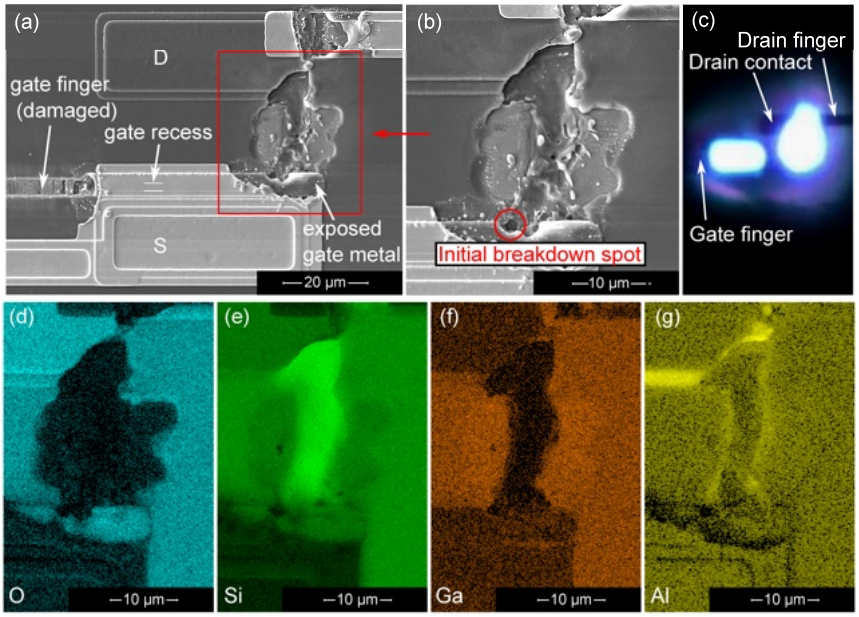


**Figure 2.3.8.** Breakdown analysis using (a)-(b) SEM, (c) optical microscope at the moment when breakdown occurs, and elemental map of (d) oxygen, (e) silicon, (f) gallium, and (g) aluminum using EDS. Dr. Alok Ranjan provided SEM and EDS images.

voltage conditions. Moreover, source-connected field plates that extend over the gate-connected field plate on top of a dielectric (Figure 2.3.7d) can assist in flattening the lateral electric field profile further [88].

Maximizing the breakdown voltage requires optimization of the field plate profile, field plate length, dielectric layer thickness, and type of dielectric used. A thin passivation layer can cause most of the potential to drop across the dielectric between the drain and one of the field plate edges, which would result in a decreasing breakdown voltage with increasing field plate length. A too-thick dielectric would result in most of the voltage to fall between the edge of the gate metal (at the gate recess) and the drain contact, leading to a constant (or near-constant) breakdown voltage with respect to increasing field plate length.

A high electric field across the dielectric not only reduces the breakdown with respect to the field plate length, but also results in reliability problems. Changes in the properties of the dielectrics can, over time, lead to excessive stress-induced leakage currents (SILC) or permanent dielectric failure as a result of a percolation path through the dielectric. In [Paper C], it is argued that the dielectric failure in the buffer-free MISHEMTs is caused by the formation of a percolation path located directly underneath the edge of the gate field plate. Additionally, the defect generation process is likely reinforced by the build-up of negative charges in the dielectric. The hypothesis is supported by optical microscopy, scanning electron microscopy (SEM), and energy dispersive X-ray analysis spectroscopy (EDS), which shows pronounced damage confined to a small area at the edge of the gate field plate (Figure 2.3.8a-c). The EDS images display a weak signal for O, Si, Ga, and Al in the same spot

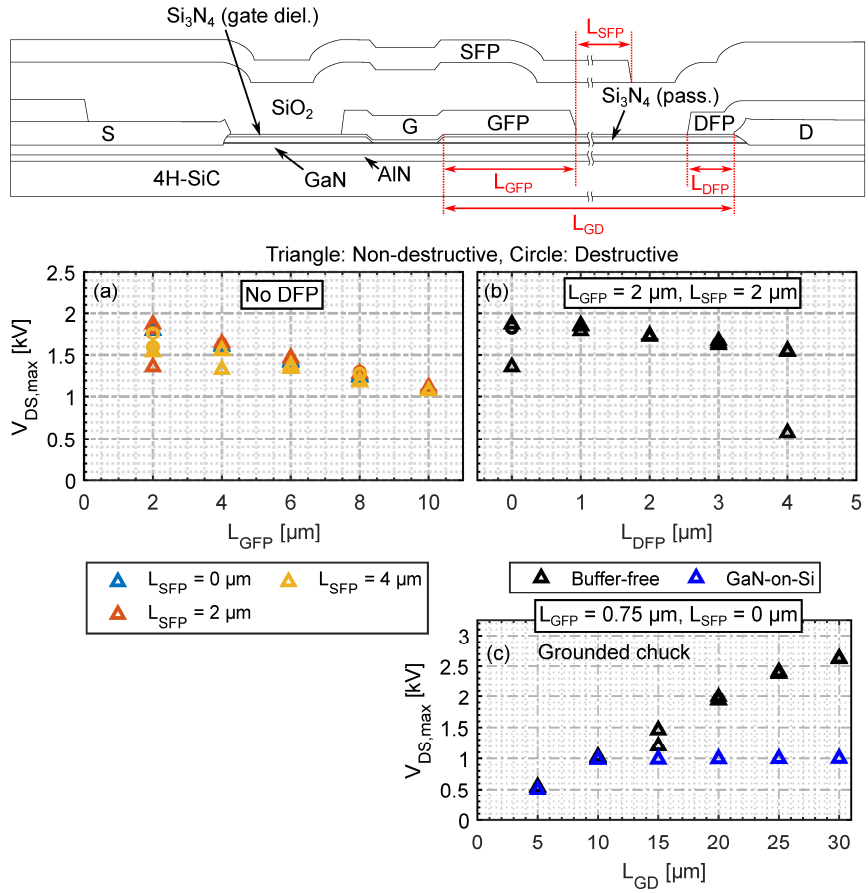


**Figure 2.3.9.** Maximum $V_{DS}$ with varying (a) $L_{GFP}$ and $L_{SFP}$, (b) $L_{DFP}$, and (c) $L_{GD}$. The relevant lengths of the GaN MISHEMT are displayed in the top figure. Measurements were performed on 3 to 5 devices.

(Figure 2.3.8d-g), indicating that the heat generated in the area has melted the whole III-nitride stack.

The pronounced electric field peak in the dielectrics may also explain the reduction in the maximum off-state drain-source voltage ($V_{DS,max}$)[5] with respect to gate-connected field plate length ($L_{GFP}$) and drain-connected field plate length ($L_{DFP}$) (Figure 2.3.9a-b). Furthermore, the source-connected field plate length ($L_{SFP}$) has a negligible impact on $V_{DS,max}$, which suggests that the 2nd dielectric (on which the source-connected field plate is deposited) could be further optimized. The shortest $L_{GFP}$ and $L_{SFP}$ lead to the highest $V_{DS,max}$ (Figure 2.3.9c), and are also an improvement on the first generation of nitrogen-implanted MISHEMTs shown in [Paper A] and [Paper B]. The buffer-free and GaN-on-Si devices display similar $V_{DS,max}$ with respect to gate-drain distance ($L_{GD}$) up to 1000 V. However, at $L_{GD}$ above 10 µm, the

[5] $V_{DS,max}$ is extracted from the drain current injection technique (DCIT) characteristics using an injection current of 1 µA/mm. The DCIT is explained in greater detail in Chapter 4.

buffer-free devices display a linear increase in $V_{DS,max}$, whereas the GaN-on-Si devices saturate due to excessive substrate current.

It is not clear whether the $V_{DS,max}$ reduction with respect to field plate lengths in Figure 2.3.9a-b, is merely a result of an insufficiently optimized dielectric/field plate configuration. The UID GaN region can also influence the ability to distribute the electric field near the III-nitride surface laterally. Uren et al. showed that the surface field in GaN HEMTs with a UID-GaN/GaN:C buffer design can be reduced by introducing non-Ohmic vertical conduction paths between the 2DEG and the C-doped buffer layer, resulting in a set of equipotential lines that roughly follow the potential of the partially depleted 2DEG in the access region [50]. Therefore, there is an interplay between field plate lengths, dielectric thicknesses on the one hand, and buffer doping concentration and distribution on the other. It is an open question whether a similar technique can be employed for buffer-free HEMTs.

### 2.3.5 GaN MISHEMT Fabrication Summary

The GaN HEMTs fabricated for studies of buffer-free III-nitride heterostructures ([Paper A-D]) were produced using identical or similar process steps, which are detailed in the following list. An overview of the device process is seen in Figure 2.3.10. Additionally, SEM and transmission electron microscopy (TEM) images of a completed MISHEMT are shown in Figure 2.3.11.

1. **Deposition of $SiN_x$ passivation layer**
   The sample surface was first prepared by removing organic and metallic contaminants using the standard clean (SC) process. A ~60-160 nm $SiN_x$ layer was deposited in a LPCVD system at 770 °C or 820 °C. The two types of films deposited at high and low temperatures were stoichiometric and Si-rich, respectively.
2. **Mesa etch**
   Active areas were defined using photolithography. When ion implantation is employed, only areas used for the transfer length method (TLM) were defined, and the remaining material was protected from subsequent etching steps. The passivation layer and III-nitride layers were removed using an ICP etch. The $SiN_x$ was removed in an $NF_3$/Ar plasma, while the AlGaN and GaN are etched in a $Cl_2$/Ar plasma. Mesas with etch heights ~300 nm were defined.
3. **Gate recess etch**
   Gate regions were formed by removing the $SiN_x$ in the active areas using an $NF_3$/Ar plasma. Gate lengths of 2-4 μm were designed in the lithography step, but with ±10% variations after the etch step.
4. **Gate dielectric deposition**
   A second SC process was performed. A ~40 nm LPCVD $Si_3N_4$ is then deposited at 770 °C.
5. **Ohmic contact lithography, recess etch, metal deposition, and post-metallization annealing**
   The ohmic contact process presented by Lin et al. [89] was employed. A recess etch with a 5-10 nm depth below the AlGaN/GaN interface was formed through a Cl-based dry etch technique before the deposition of a 20/280/15 nm Ta/Al/Ta stack using electron beam evaporation. Afterwards,

the contacts were annealed at 550-575 °C up to 60 min in an $N_2$ atmosphere using a rapid thermal processing (RTP) system to reduce contact resistance.

6. **Ion implantation**
   The active areas were protected with a ~3.2 μm photoresist, while the remaining areas were exposed to the implantation ions. Nitrogen and argon ions were utilized for isolation as described in Section 2.3.2. Post-implantation annealing was implemented to improve the isolating properties (Figure 2.3.4c-d).
7. **Gate metal lithography and deposition**
   A one-step lift-off photolithography process was used to define resist openings with a negative sidewall around the gate recess areas. A metal stack consisting of 30/20/300/20 nm Ni/Pt/Au/Ti was deposited onto the resist and resist openings using electron beam evaporation. The metal was deposited into the gate recess (on top of the gate dielectric), as well as onto the gate dielectric/passivation stack, creating a one-step field plate profile.
8. **Dielectric and source field plate deposition**
   To enable the deposition of the source field plate metal, a ~600 nm $SiO_x$ was first deposited onto the gate metal and gate dielectric using PECVD. Via openings were formed through the $SiO_x$ to the source contact, and a 20/280/20 nm Ti/Au/Ti metal stack was deposited on top of the $SiO_x$ layer and into the via opening. The deposited metal extends from the source contact over the gate field plate.

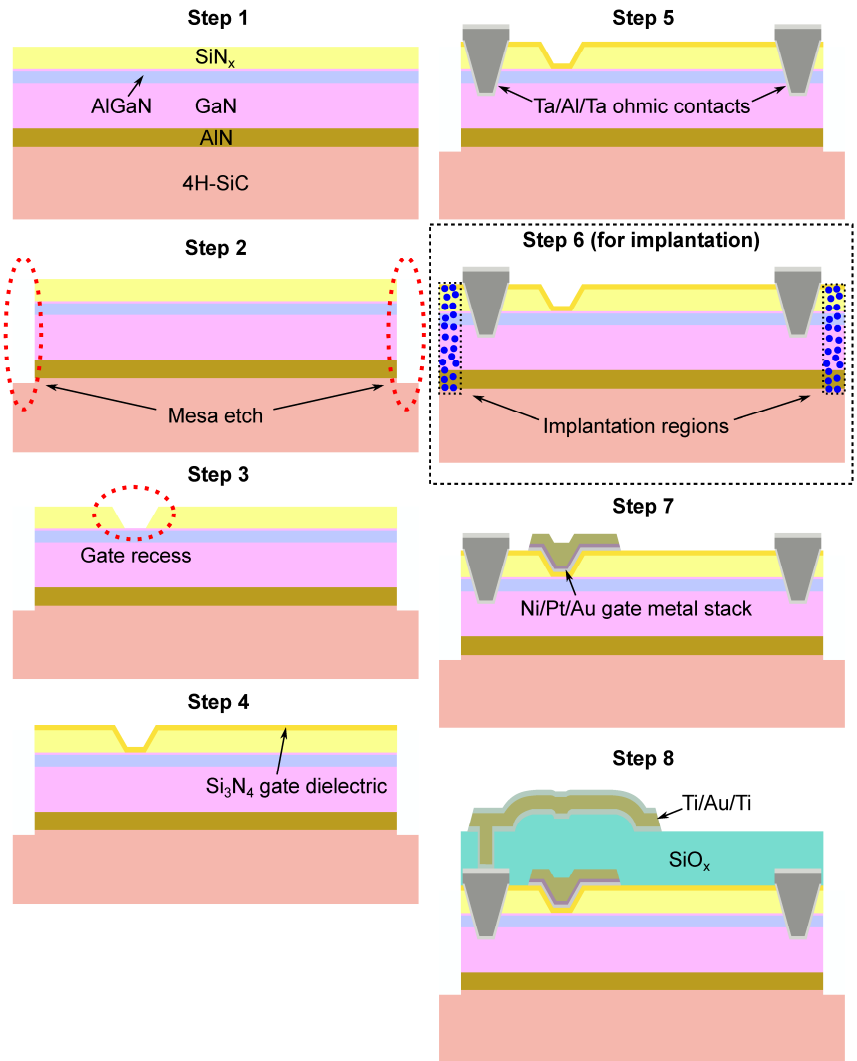


**Figure 2.3.10.** Schematics showing the step-by-step device fabrication process of GaN MISHEMT. Mesa etching around devices (Step 2) is not used when ion implantation is employed (Step 6).

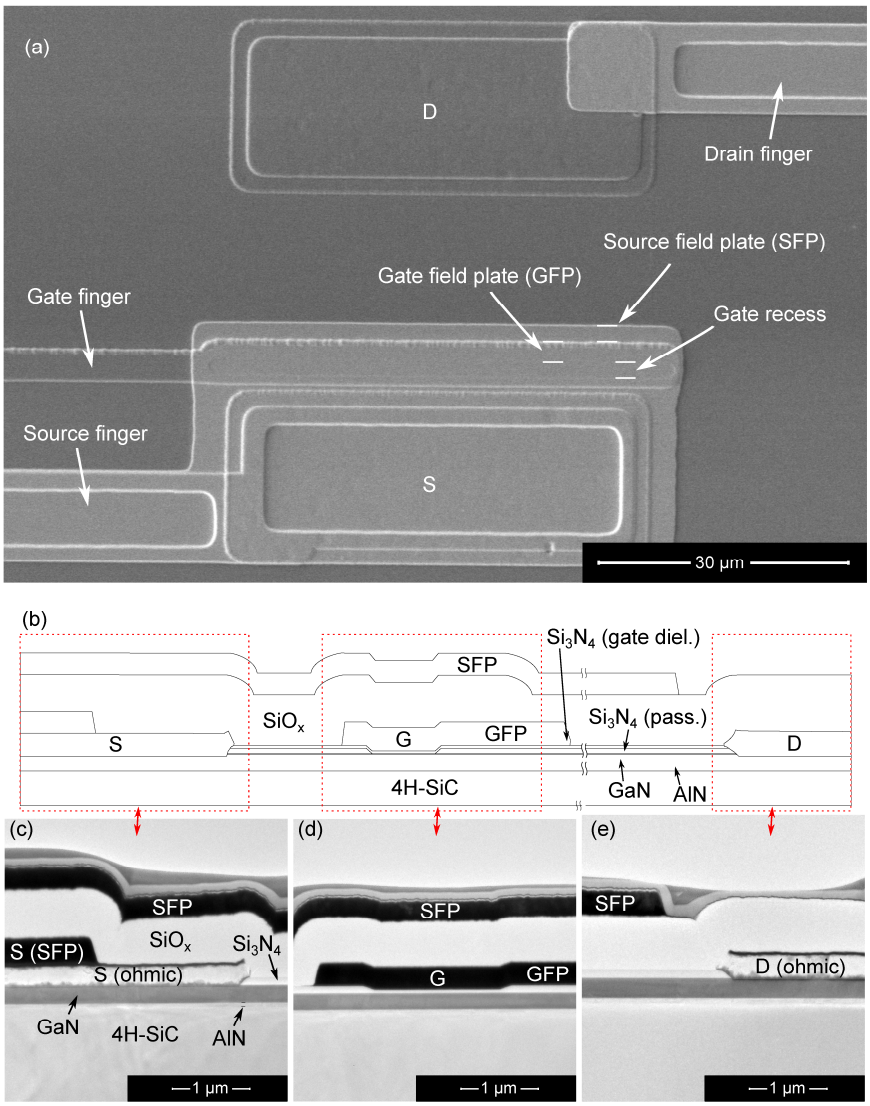


**Figure 2.3.11.** Images showing a completed GaN MISHEMT on a buffer-free heterostructure, where (a) is a top-view SEM image of the active area, (b) is a side-view schematic of the device with the source region, gate region, and drain region highlighted in the red rectangles. TEM side-view images of the (c) source region, (d) gate region, and (e) drain region corresponding to the three highlighted regions in (b) are also shown. SEM and TEM images courtesy of Dr. Alok Ranjan.

## 2.4 Buffer-Free Power MISHEMT Benchmarking

Comparisons between different GaN device technologies can be challenging since the measurement conditions and the definitions used for extracting key performance metrics differ between research groups. For instance, an unambiguous criterion for the breakdown voltage has been the subject of debate within the power semiconductor device community. Theoretically, breakdown occurs when the integral of the impact ionization coefficient ($\alpha$) along some one-dimensional path reaches one, i.e.

$$\int_{x_1}^{x_2} \alpha \, dx = 1 \,, \tag{2.1}$$

which results in a multiplication coefficient that approaches infinity. However, determining the impact ionization coefficient directly from the off-state breakdown characteristics of an HEMT is challenging. It is therefore common to define the breakdown voltage at which the current through any terminal exceeds a certain pre-defined current density criterion. This value is typically obtained through a current or voltage sweep while the transistor is biased in an off-state condition. The advantage of this type of approach is that it facilitates comparisons between devices in the literature. For GaN-based HEMTs, 1 mA/mm was initially used as a criterion [90]–[92]. More recently, however, the criterion has been lowered to 1 µA/mm due to improvements in device processing and epitaxial film quality [93] [94]. Defining the breakdown voltage using a fixed current criterion will encompass scenarios when the device breaks down as a result of a current surge that destroys the device (hard breakdown), but also scenarios where the measurement stops due to excessive leakage through one of the terminals (soft breakdown). Nevertheless, it is currently the best way to compare different GaN-based technologies.

In addition to the breakdown voltage, it is common to compare the power figure of merit (PFOM), given by

$$PFOM = \frac{BV^2}{R_{on,sp}}, \tag{2.2}$$

where $BV$ is the breakdown voltage, and $R_{on,sp}$ is the specific on-state resistance, calculated by multiplying the active area,

$$A_{active} = (L_{SD} + 2L_T)W, \tag{2.3}$$

with the on-state resistance ($R_{on}$). In Equation 2.3, $L_{SD}$ is the source-drain distance, $L_T$ is the transfer length extracted from TLM, and $W$ is the width of the active area.

The lower current criterion will be used when the buffer-free MISHEMTs are compared to other GaN-based HEMTs reported in the literature, as it is the most commonly used criterion over the past 7-8 years. The first generation of buffer-free MISHEMTs presented in [Paper A] display a breakdown voltage of 1621 V with a PFOM of 729 MW/cm$^2$, which is similar to most GaN HEMTs on Si, SiC, and

Sapphire (Table 2.3). In the second generation, a buffer-free epitaxial heterostructure with a lower 2DEG sheet resistance was used. Additionally, shorter field plate lengths were employed, and the lateral isolation was improved compared to the first generation. With these changes, a $V_{DS,max}$ (measured with the DCIT) of 1997 V and a PFOM of 1559 MW/cm$^2$ could be achieved. In order to realize higher PFOMs, the thicknesses of the first and second dielectrics need to be tuned. Furthermore, changing the implantation species may also improve lateral isolation, as was described in 2.3.2. It could also be possible to achieve higher breakdown voltages by reducing the UID GaN channel layer thickness, as was demonstrated by Hilt et al. using an AlGaN/GaN/AlN double heterostructure with an AlN buffer layer instead of an AlN nucleation layer [95]. In summary, the buffer-free shows great potential in terms of $R_{on,sp}$, breakdown voltage, and PFOM.

**Table 2.3.** Comparison between the buffer-free MISHEMT in this work and GaN-based HEMTs reported in the literature.

| BV @ 1 µA/mm (V) | D/E-mode | Sub. | $R_{on,sp}$ (mΩ·cm$^2$) | PFOM (MW/cm$^2$) | Organisation (year) reference |
|---|---|---|---|---|---|
| 792[a] | D | Si | 0.91 | 689 | EPLF (2017) [94] |
| 1370[a] | D | Si | 2.67 | 703 | |
| 3000[a] | D | Si | 13 | 692 | IEMN (2018) [96] |
| 960[b] | E | Si | 1.76 | 523 | EPLF (2019) [93] |
| 1650[a] | E | Si | 1.76 | 1549 | |
| 1272[a] | D | 4H-SiC | 2.35 | 689 | XDU (2020) [97] |
| 852[b] | E | Si | 2.73 | 266 | SINANO (2021) [98] |
| 1449[a] | E | Si | 2.73 | 769 | |
| 1344[b] | E | Si | 3.92 | 461 | HKUST (2021) [99] |
| 1790[c] | D | 4H-SiC | 1.33 | 2400 | FBH (2023) [95] |
| 2230[c] | E | Sapp. | 6.42 | 774 | PKU (2023) [100] |
| 2573[c] | E | Sapp. | 7.33 | 903 | PKU (2024) [101] |
| 1621[a,d] | D | 4H-SiC | 3.61 | 729 | This work 1st generation [Paper A] |
| 1783[a,e] | D | 4H-SiC | 3.44 | 923 | This work 1st generation |
| 1997[a,e] | D | 4H-SiC | 2.60 | 1559 | This work 2nd generation |

[a] Floating substrate [b] Grounded substrate [c] Substrate bias is not stated

[d] Measured using voltage sweep

[e] Measured using the DCIT (taking $V_{DS,max}$ as the breakdown voltage) with 1µA/mm injection current.

# Chapter 3

# Interfacial Traps in Buffer-Free GaN HEMTs

The presence of recombination-generation (r-g) centers in III-nitride crystals results in degradation of the on-state performance when switching between a high-voltage off-state and a low-voltage, high-current on-state in GaN HEMTs. During off-state conditions, trap centers at the GaN cap surface, in the barrier layer, at (or near) one of the III-nitride interfaces, or inside the buffer/back barrier layer can capture electrons, leading to a temporary reduction in the drain current ($I_D$) (Figure 3.1.1a). Electron capture processes can involve tunneling from the gate metal to positively charged surface donor states, or bulk trap states in the AlGaN barrier, such as fluorine or carbon. It is also possible for electrons in the 2DEG to get displaced into the buffer region, resulting in the capture by compensating dopants such as C or Fe.

In heterostructure designs with thick GaN buffer layers, the capture and emission of electrons of defects near the AlN nucleation layer is unlikely because of its large separation from the 2DEG. Instead, Fe or C dopants are more likely to affect the trap dynamics. However, in heterostructures where the barrier/GaN junction is near the GaN/AlN interface (whether it is a nucleation layer or AlN buffer layer), any near-interfacial defect states are going to have a larger influence on the device performance (Figure 3.1.1b). In this chapter, an extended explanation of the hypothesis presented in [Paper D] will be provided.

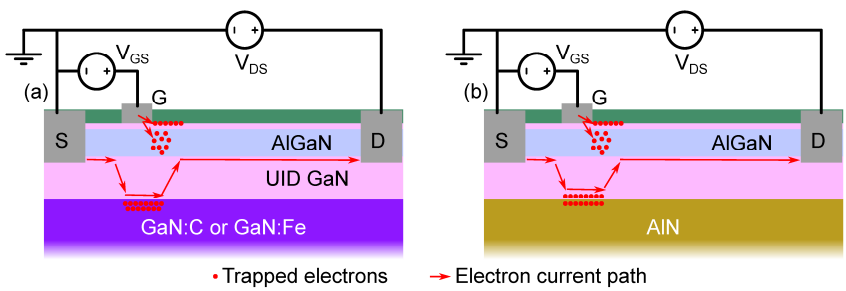


**Figure 3.1.1.** Potential trap locations and current paths during a high-voltage off-state in (a) a GaN HEMT with a thick buffer layer, and (b) in a buffer-free HEMT.

# 3.1 Trap Characterization

## 3.1.1 Drain Current Transient Measurements

The influence of traps can readily be observed by performing drain current transient (DCT) measurements. With this measurement technique, the gate-source voltage ($V_{GS}$) is ramped to an off-state condition ($V_{GS}<V_{th}$), while the $V_{DS}$ is maintained at 0 V (Figure 3.3.2a-b). After making sure that the channel is depleted of electrons, $V_{DS}$ is ramped to a high positive voltage and maintained at this voltage for a predefined amount of time. When the off-state (stress) time has elapsed, the $V_{DS}$ and $V_{GS}$ are ramped to an on-state condition, which is usually set to 0.5-1 V for $V_{DS}$ and 0 V for $V_{GS}$ (for normally-on transistors). The drain current is then monitored over time, where changes in the current can occur from a few µs up to several thousand seconds. The shape of the current over time can be used to extract information about the traps.

## 3.1.2 Temperature Dependence

The trap's energetic location in the band gap and its corresponding cross-section can be estimated by employing a stretched exponential model (Equation 3.1), where the current produced by emitted charge carriers from a unique trap $i$ contains an amplitude $I_{D,i}$, a characteristic time constant $\tau_i$, and a semi-empirical fitting parameter $\beta_i$ [102].

$$I_D = I_{D,0} - \sum_{i=1}^{N} I_{D,i} e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{3.1}$$

The drain current may exhibit a behavior characteristic of several trap states, making it appropriate to include several sets of trap parameters ($I_{D,i}$,$\tau_i$,$\beta_i$). The total number of parameter sets $N$ should be equal to the number of traps. Adding more parameter sets may result in a better fit, but will not necessarily reflect any real emission of charge carriers from trap centers.

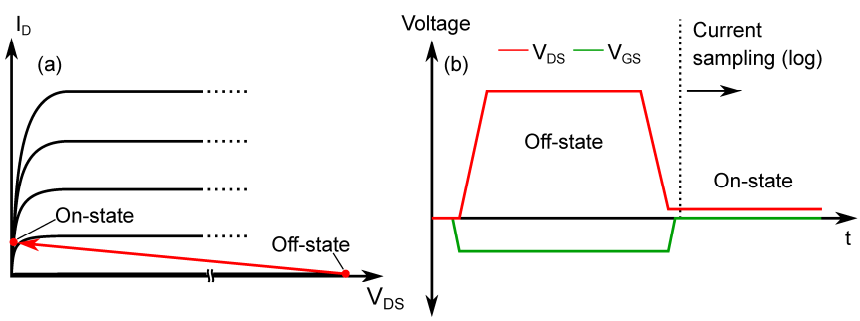


**Figure 3.1.2.** Schematics showing the two operating states in a DCT measurement in (a) the output characteristics of the transistor, and (b) in the time domain.

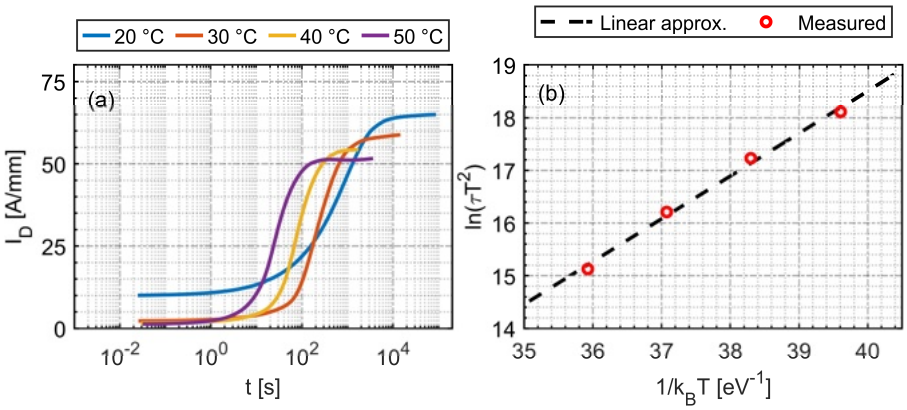


**Figure 3.1.3.** Example of a (a) DCT characteristic with one significant time constant at different temperatures, and (b) Arrhenius plot of the measured $\ln(\tau T^2)$ and a linear approximation is used for the extraction of the activation energy and cross-section.

The characteristic time constant $\tau_i$ extracted from the fit of the stretched exponential model is the inverse of the emission rate ($e_i$) of the r-g center. According to Shockley-Read-Hall (SRH) theory [103], the emission rate is, in turn, related to the energy of the trap level $E_{T,i}$ and the capture cross section $\sigma_i$ through the following relation,

$$\tau_i = \frac{1}{e_i} = \frac{1}{2}\frac{g_n}{\sigma_{n,i}}\left(\frac{3k_BT}{m_n^*}\right)^{-1/2}\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{-3/2} e^{\frac{E_{A,i}}{k_B T}}, \tag{3.2}$$

where $g_n$ is a degeneracy factor, $k_B$ is the Boltzmann's constant, $m_n^*$ is the effective mass of the semiconductor, and $h$ is Planck's constant. From Equation 3.2, the activation energy ($E_{A,i} = E_C - E_{T,i}$) and capture cross-section ($\sigma_{n,i}$) can be extracted by performing DCT measurements at several temperatures. If the $I_D$ increase is caused by an emission process from an r-g center, then the time constant will tend to shift towards lower values as the temperature increases (Figure 3.1.3a). Using Equation 3.2, $E_{A,i}$ and $\sigma_{n,i}$ can be straightforwardly extracted by using the fact that $\ln(\tau_i T^2)$ exhibits a linear relationship with respect to $1/k_BT$ (Equation 3.3).

$$\ln(\tau_i T^2) = \frac{E_{A,i}}{kT} - \ln(\sigma_{n,i}) + \ln\left(\frac{g_n h^3}{3^{1/2}2(2\pi)^{3/2}k_B^2 m_n^*}\right) \tag{3.3}$$

The activation energy and cross-section are extracted from the slope and y-intercept of the linear approximation of the Arrhenius plot (Figure 3.1.3b), respectively.

In some instances, a quasi-continuous energetic distribution of states can be present in a region with a high impurity or defect concentration, which will affect the behavior of the $I_D$ recovery. Broader distributions tend to result in a more gradual current recovery with a lower $\beta$ in Equation 3.1 [104]. Energetic distribution can, for instance, be present in heavily doped buffer layers or defect bands near interfaces — the latter being of more relevance for buffer-free heterostructure due to high current densities near the GaN/AlN during high-voltage off-state conditions.

## 3.2 Modeling of the Off-State Leakage and Drain Current Recovery in Buffer-Free MISHEMTs

DCT measurements are useful for analyzing the $I_D$ response after subjecting the device to high-voltage conditions and extracting activation energies and capture cross sections. However, it is generally challenging to draw any firm conclusion about the spatial position, the distribution, and the capture–emission process solely from the DCT measurements. Physics-based modeling using TCAD facilitates the investigation of the dominant capture–emission processes. This section aims to understand the impact of critical processing-related and growth-related parameters in buffer-free heterostructures. Model assumptions and parameters are presented in Appendix A and Appendix B, respectively.

### 3.2.1 Ideal GaN/AlN Interfaces

The difference in the polarization of the GaN channel layer and AlN nucleation layer is expected to produce a negative sheet charge density at the GaN/AlN interface (Figure 3.2.1a), according to

$$\Delta P_z = P_{z,GaN} - P_{z,AlN} = -\sigma_{bound}, \tag{3.4}$$

where $P_z$ is the polarization component along the c-axis, and $\sigma_{bound}$ is the bound polarization sheet charge density [105]. GaN deposited on AlN substrates has a critical thickness of ~1 nm [106], while AlN deposited on 4H-SiC can have critical thicknesses up to 40 nm [27]. Assuming that both GaN and AlN layers are relaxed, only the difference in the spontaneous polarization will produce a sheet charge. The spontaneous polarization in metal-polar GaN and AlN will produce a negative sheet

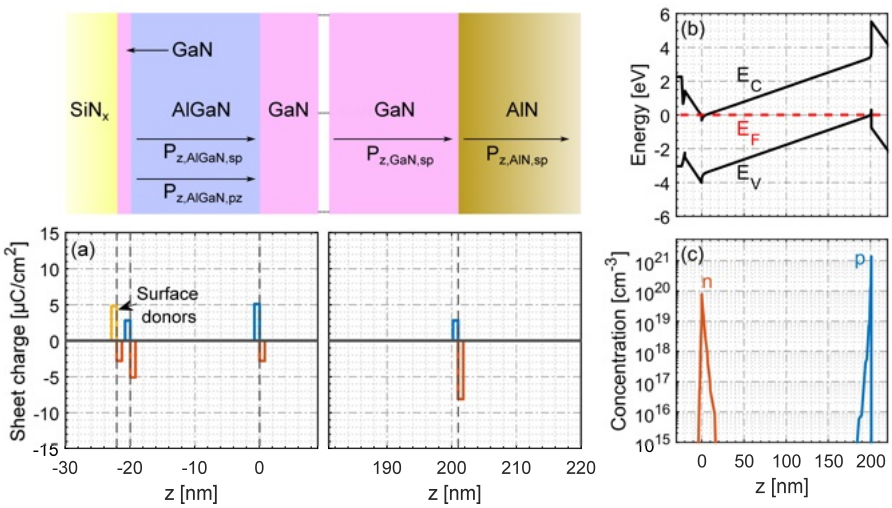


**Figure 3.2.1.** Sheet charge contributions from each layer in a buffer-free heterostructure (a), including from the c-axis spontaneous polarization ($P_{z,sp}$), piezoelectric polarization ($P_{z,pz}$), and surface donor sheet charges. Zero-bias simulations showing the Fermi level relative to the conduction band minimum and valence band maximum with respect to vertical position (b). Resulting electron and hole concentrations with respect to vertical position are shown in (c).

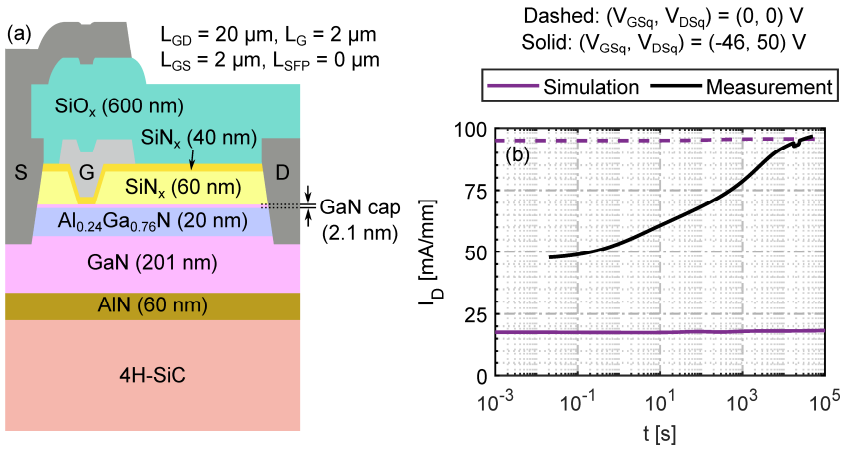


**Figure 3.2.2.** Measured and simulated buffer-free GaN MISHEMT, where (a) is a cross-sectional schematic of the device used in the simulation, and (b) is the DCT characteristics. Only surface trap states have been considered in the simulations.

charge at the GaN/AlN interface of -4.7 μA/cm$^2$ to -7.1 μC/cm$^2$ (based on values in Table B1-B2). If the system is in thermal equilibrium (spatially uniform Fermi level), the bound charge should be screened by a positive free sheet charge,

$$\sigma_{free} = -\sigma_{bound} + \Delta(\varepsilon E_z) > 0, \tag{3.5}$$

where $\varepsilon$ is the dielectric constant and $E_z$ is the electric field component along the z-axis. In an ideal GaN/AlN heterostructure with no defects around the interface, the Fermi level will be positioned (energetically) below the valence band maximum (Figure 3.2.1b), leading to the formation of a two-dimensional hole gas (2DHG) close to the GaN/AlN interface (Figure 3.2.1c). If the AlN exhibits a compressive strain, the 2DHG sheet charge will be smaller. Conversely, if the AlN layer has a tensile strain, the sheet charge will be larger.

If the 2DHG does indeed exist, a prolonged on-state current degradation relative to the equilibrium state should be observed after stressing a GaN MISHEMT with a large negative off-state gate bias (Figure 3.2.2a-b). There are primarily three mechanisms that could produce this effect. The first—and most likely the dominant mechanism—is (mobile) electron loss through the drain and source terminals. During the off-state bias condition, the boundary conditions imposed on the system should produce a hole current from the 2DHG toward the gate contact and the source contact (Figure 3.2.3a-b). To preserve charge neutrality and maintain Kirchhoff's current law (KCL), an electron current out of the drain terminal or source terminal (electrons flowing into the terminal) should offset the hole current into the source/gate, effectively reducing the amount of mobile charge carriers in the system. Assuming only thermal generation from the valence band, the system should enter a metastable state in which the time until full recovery is longer than $10^5$ s (Figure 3.2.2b). In a MISHEMT, the proportion of the hole current into the source or gate contacts is also affected by the conductivity in the gate dielectric. In a perfect dielectric where the hole current density is zero, the holes should accumulate underneath the gate dielectric, which increases the potential in the 2DHG, and allows for a large hole flow

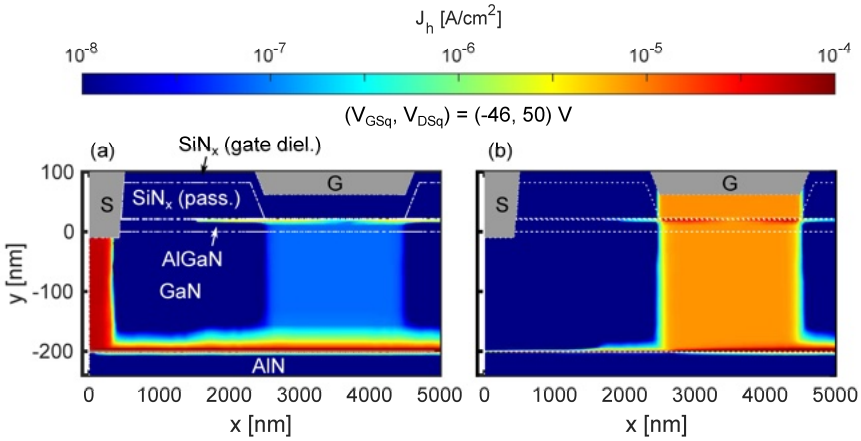


**Figure 3.2.3.** Hole current density in the source-gate region during the off-state in a buffer-free GaN MISHEMT with (a) a perfect gate dielectric, and (b) a leaky gate dielectric.

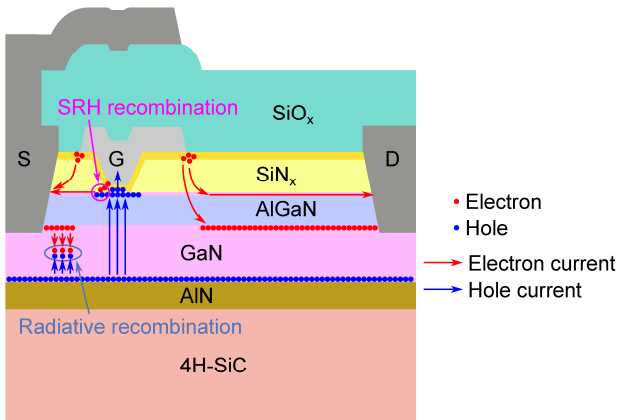


**Figure 3.2.4.** Cross-sectional schematic showing two potential recombination mechanisms resulting in a metastable on-state.

into the source contact (Figure 3.2.3a). By contrast, if the dielectric is leaky, the potential in the 2DHG is lower (more negative) across the whole device, and a majority of the holes will flow into the gate contact instead (Figure 3.2.3b).

The other two possible processes in which mobile charge carriers are lost are through radiative and SRH recombination (Figure 3.2.4). Radiative recombination can occur when the electron concentration in the gate-source region increases inside the GaN layer (e.g., under high $V_{DS}$ stress), resulting in a large $np$-product, which increases the radiative recombination term in the continuity equations, since

$$R_{rad} = C_{rad} \cdot \left(np - n_{i,eff}^2\right), \tag{3.6}$$

where $C_{rad}$ is a constant in the order of $10^{-10}$ cm$^3$/s, and $n_{i,eff}$ is the effective intrinsic density. In GaN, $n_{i,eff}$ is ~$10^{-10}$ cm$^{-3}$ at room temperature and is therefore negligible compared to the $np$-product. The low $V_{DS}$ bias used in the simulations in Figure 3.2.3 produced a relatively low radiative recombination. Increasing $V_{DS}$ above 50 V will

increase the 2DHG potential in the source-gate region, resulting in a larger overlap of the electron and hole concentrations. In the simulated devices in Figure 3.2.3, bulk traps were not considered, which entail a non-existent SRH recombination through deep-level band gap states in the III-nitride materials. However, recombination through surface states could become significant if, for instance, electrons from the gate metal and holes accumulated near the $Si_3N_4$/GaN interface (assuming conduction through the dielectrics) interact (Figure 3.2.4), since the recombination rate is given by

$$R_{SRH} = \frac{np - n_{i,eff}^2}{\tau_p\left(n + n_{i,eff}e^{E_{trap}/k_BT}\right) + \tau_n\left(p + n_{i,eff}e^{-E_{trap}/k_BT}\right)}, \tag{3.7}$$

where $\tau_p$ is the hole lifetime, $\tau_n$ is the electron lifetime, and $E_{trap}$ is the trap energy level relative to the intrinsic Fermi level.

The semipermanent current degradation is not observed in a real buffer-free MISHEMT (Figure 3.2.2b), where a current recovery is seen in the $10^{-3}$ – $10^5$ s period. Therefore, additional mechanisms that prevent holes from recombining with mobile electrons or from exiting the system during high off-state biases have to be considered.

## 3.2.2 Near-Interfacial Defects and Impurities

Although a 2DHG is expected to exist in an ideal GaN/AlN heterostructure, this does not need to be the case in a real semiconductor crystal. Since the GaN layer is deposited directly onto the AlN nucleation layer, impurities such as oxygen, hydrogen, and silicon from the substrate surface or the atmosphere can be incorporated into the GaN crystal or coalesce around the GaN/AlN interface. Additionally, due to the mismatch in thermal expansion coefficient and lattice constants between GaN and AlN (Table 2.1), crystal point defects and defect clusters can form as well. These defects and impurities may act as r-g centers, whose trap occupancy is highly dependent on the proximity to the III-nitride interfaces. Donor-like defects are more likely to have a high hole occupancy (compared to the bulk case) in order to satisfy Equation 3.5, resulting in a reduced hole concentration (Figure 3.2.5).

The tendency of impurities to form Gaussian-shaped profiles near the GaN/AlN junction was observed using Secondary Ion Mass Spectroscopy (SIMS) in [Paper D] (Figure 3.2.6a-b), but has also been reported elsewhere in the literature. Chaudhuri et al. found that both oxygen and silicon tend to cluster around GaN/AlN interfaces with negative polarization charges, which consequently lowered 2DHG density and reduced hole mobility [107]. They showed that the impurity concentrations were substantial near the MOCVD-grown AlN layer, but could be reduced by incorporating MBE-grown impurity blocking layers, resulting in a higher 2DHG density near the GaN/AlN interfaces.

Donor-like defects may have a lower formation energy due to the presence of the negative polarization charges, which would explain the clustering of oxygen and silicon. Carbon tends to form acceptor-like impurities when incorporated into a bulk

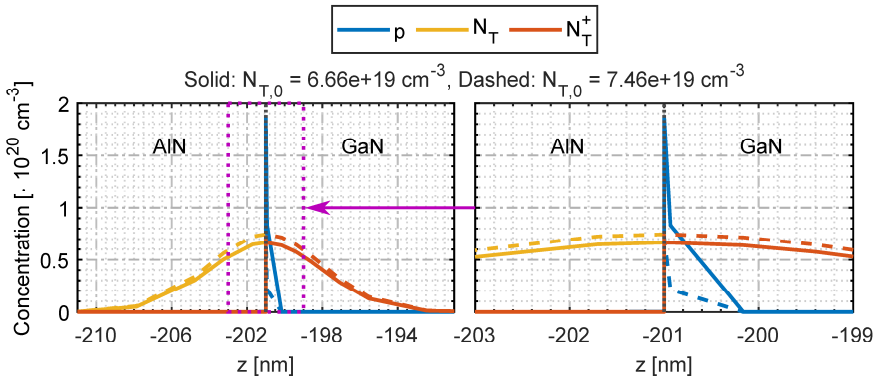


**Figure 3.2.5.** Simulated hole concentration (p), total trap concentration ($N_T$), and positively ionized trap concentration ($N_T^+$) near the GaN/AlN interface. A Gaussian-shaped trap profile ($N_T = N_{T,0}e^{-(z-z_0)^2/2\sigma_z^2}$) was assumed. Only donors on the GaN side of the interface were considered in this example.

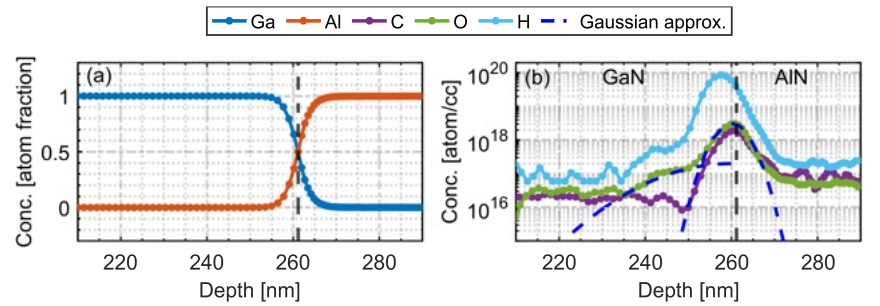


**Figure 3.2.6.** SIMS data showing (a) Ga and Al fraction content, and (b) Common unintentionally introduced impurities near the GaN/AlN interface, including hydrogen, oxygen, and carbon.

GaN crystal. However, it is not clear whether acceptor-like impurities from C would have a lower formation energy compared to donor-like states (e.g., $C_{Ga}$) near the GaN/AlN interface specifically. Modeling using density functional theory would give an idea of the types of impurities likely to form around the GaN/AlN interface.

### 3.2.3 Proposed Model for Transient and Breakdown Characteristics

Based on the arguments given above, donor states are needed to reduce the 2DHG concentration so that the system does not enter a metastable state after being subjected to high off-state conditions. However, due to the proximity of the AlN nucleation layer to the 2DEG in the buffer-free heterostructures, excessive electron capture by these highly-ionized donor states may pose a problem for the on-state performance in HEMTs fabricated on this heterostructure, particularly when the thickness of the GaN layer is reduced. A model describing the influence of these trap states during and after high voltage conditions is currently not fully understood. This section will explore different competing models, which will be compared with electrical measurements.

In [Paper D], the DCIT characteristics of MISHEMTs on two different types of buffer-free epis are presented (Figure 3.2.7a). One exhibits an excessive drain-source

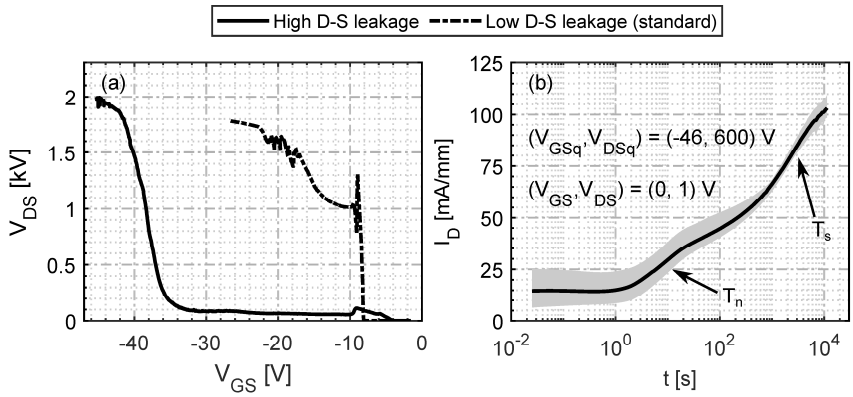


**Figure 3.2.7.** Measured (a) DCIT characteristics with 1 µA/mm injection current, and (b) DCT characteristics of buffer-free GaN MISHEMTs with two different epitaxial heterostructures. The shaded area in (b) indicates the spread between different devices. The stress time used in (b) is 100 s.

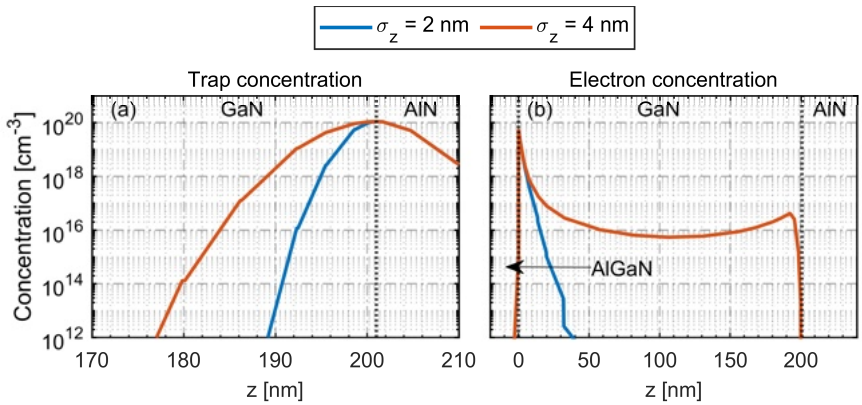


**Figure 3.2.8.** Zero-bias simulation showing (a) two Gaussian-shaped trap profiles with different spatial standard deviations ($\sigma_z$) along the c-axis in a buffer-free heterostructure, and (b) the resulting electron concentration.

(D-S) leakage current, resulting in a large negative $V_{th}$. In contrast, the other — a standard buffer-free material — displays a $V_{th}$ in the -8 to -10 V range. The reason for the large negative threshold voltage in the former case is due to an excessively high electron concentration in the GaN layer. In the previous section (3.2.2), it was argued that the presence of donors near the AlN layer would result in a large ionized concentration and, therefore, a low electron concentration. However, the overall number of mobile electrons being generated is dependent on the shallowness of the donor level, the peak concentration in the Gaussian-shaped impurity distribution, and the spatial standard deviation of the impurity distribution. Profiles with longer tails will tend to degrade electron confinement and result in overall higher mobile electron concentrations in the GaN layer (Figure 3.2.8a-b). Additionally, more shallow traps in the tail end of the distribution will result in a higher mobile electron concentration.

The energetic location of the hypothesized donor state(s) is not immediately apparent from the DCIT characteristics in Figure 3.2.7a alone. In [Paper D], it is demonstrated that the devices with high D-S leakage current display an $I_D$ recovery behavior characteristic of two trap states (Figure 3.2.7b). These two trap states will be referred to as $T_n$ and $T_s$ for consistency with [Paper D]. Additionally, using DCTS, it is shown

**Table 3.1.** Device parameters of the simulated device.

| Device structure parameter | Description | Value used |
|---|---|---|
| $h_{AlN}$ | AlN thickness | 60 nm |
| $h_{GaN}$ | GaN thickness | 201 nm |
| $h_{AlGaN}$ | AlGaN barrier thickness | 20 nm |
| $h_{Cap}$ | GaN cap thickness | 2.1 nm |
| $h_{GD}$ | Gate dielectric thickness | 40 nm |
| $h_{Pass}$ | Passivation layer thickness | 60 nm |
| $h_{SiOx}$ | Second dielectric thickness | 600 nm |
| $x_{AlGaN}$ | Al mole fraction in AlGaN | 24.7% |
| $L_{GS}$ | Gate-source length | 2 µm |
| $L_G$ | Gate length | 2 µm |
| $L_{GD}$ | Gate-drain length | 20 µm |
| $L_{GFP}$ | Gate field plate length | 0.75 µm |
| $L_{SFP}$ | Source field plate length | 0 µm |

that $T_n$ exhibits an activation energy and cross section of 0.19 eV and a cross section of $1.06 \cdot 10^{-23}$ $cm^2$, while $T_s$ displays an activation energy of 0.61 eV and a cross section of $1.14 \cdot 10^{-18}$ $cm^2$. These are distinctly different from the trap in the GaN-on-Si reference sample used in [Paper D], which rules out bulk traps in the dielectric as an origin for $T_n$ and $T_s$.

Based on the two characteristics in Figure 3.2.7 and the extracted activation energies and cross sections, it is not possible to discern the spatial location and distributions of the trap states in the heterostructure, and the mechanism that gives rise to the current recovery behavior. However, since the unintentionally introduced impurity concentrations (e.g., oxygen and carbon) inside the GaN and AlGaN layers—away from the GaN/AlN interface—are typically in the order of $1\text{-}5 \cdot 10^{16}$ $cm^{-3}$, their overall impact on the DCT characteristics is negligible [108]. Therefore, in the following analysis, the trap states inside the bulk GaN will be ignored, and only trap states near the AlN layer and at the surface of the GaN cap layer will be considered.

In trying to understand the trap and de-trapping process, two different cases were analyzed and compared to the measured characteristics in Figure 3.2.7. The devices with a high D-S leakage current were used for calibrating the model. Dimensions and chemical compositions of the simulated devices are outlined in Table 3.1. The two cases that will be discussed are the following,

1. **Non-conductive dielectrics**
   The electron and hole continuity equations are not solved inside the $Si_3N_4$ dielectrics. As a result, electrons cannot flow from the gate metal to the available (ionized) donor surface states in the access regions. Likewise, holes cannot flow into the gate metal from the semiconductor regions.
2. **Leaky dielectrics with acceptor and donor concentrations**
   The $Si_3N_4$ dielectrics are treated as semiconductor materials. Consequently, the electron and hole continuity equations are solved. Tunneling is activated to/from the gate metal and the $Si_3N_4$/GaN interfaces. Deep donor-like and acceptor-like states are incorporated into the dielectrics.

The two alternatives will primarily be evaluated based on their impact on the DCIT characteristics. These characteristics are chosen because they are particularly effective in falsifying different models, as the parameters under investigation strongly influence both the $V_{th}$ behavior and the electric field distribution between the gate and drain.

## Case 1: Non-Conductive Dielectrics

Since electron and hole conduction are ignored, electron trapping to surface states is negligible. Consequently, the two traps observed in Figure 3.2.7b should be located at, or near, the GaN/AlN interface (since the impact of traps in the bulk GaN away from the interface is assumed to be small). In this scenario, two Gaussian-shaped spatial trap distributions consisting of donors with energy levels of 0.6 eV and 0.2 eV from the conduction band minimum were introduced. The energy levels were chosen to match the traps extracted from DCTS in [Paper D]. The spatial standard deviations were tuned to give a similar $V_{th}$ as the high D-S leakage sample in Figure 3.2.7a (Figure 3.2.9a). The maximum off-state voltage in the DCIT in the simulations is significantly lower than the measurements (approximately 2 kV). Even if the impact ionization parameter for electrons ($a_n$ in Equation A.1) is reduced to increase the max $V_{DS}$, the MISHEMT is not capable of reaching more than a few hundred volts. Moreover, an excessive drain-source leakage current cannot itself explain the low max off-state voltages seen in Figure 3.2.9a. Instead, it is a consequence of three interacting mechanisms (Figure 3.2.9b), namely,

- A high electric field peak near the edge of the gate field plate edge that initiates impact ionization,
- Holes generated by impact ionization accumulate near the GaN/$Si_3N_4$ interface under the gate metal (Figure 3.2.10a), resulting in a large potential across the gate dielectric, and an increase of the potential inside the III-nitride layers (Figure 3.2.10b),

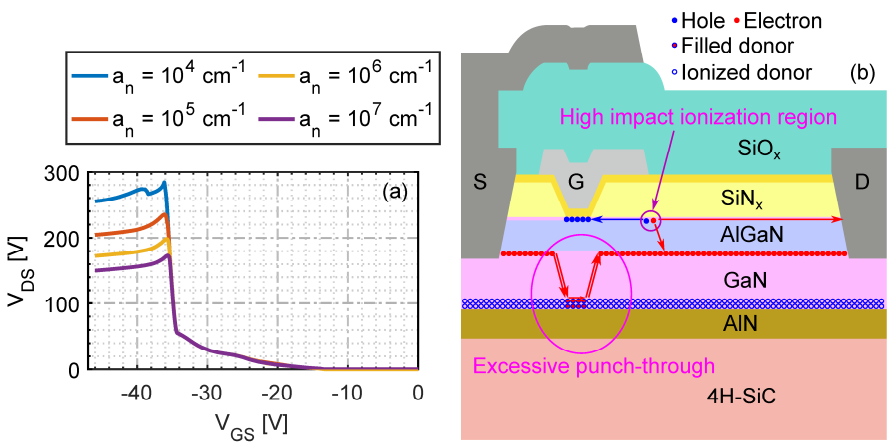


**Figure 3.2.9.** Simulations of a buffer-free MISHEMT with a non-conductive gate dielectric with two near-interfacial donor-like trap states, where (a) is the simulated DCIT characteristics with different impact ionization parameters $a_n$, (b) is a schematic showing the process that results in the low max off-state voltages.

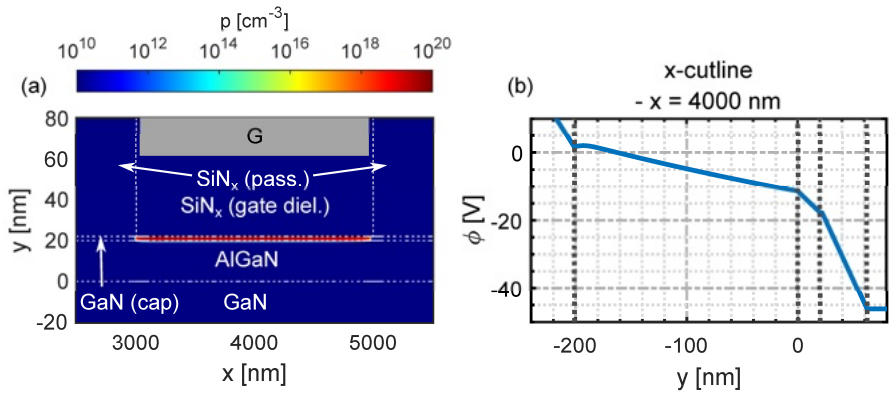


**Figure 3.2.10.** Simulated (a) top-view surface plot of the hole concentration near the gate recess, and (b) x-cutline plot of electrostatic potential in the gate region. The data was extracted at $V_{GS}$ = -46 V in the DCIT characteristics.

- Excessive drain-source punch-through current due to hole screening at the GaN/$Si_3N_4$ interface.

Furthermore, these three mechanisms can create a positive feedback loop, where the hole accumulation under the gate metal exacerbates the punch-through current. This, in turn, amplifies the impact of the ionization rate $g_{ii}$ (Equation A.2) which generates more holes. In a real device, the high electric field across the dielectric under the gate metal would likely lead to a premature, irreversible dielectric breakdown. Because of these effects, a model that assumes no conduction through the dielectrics cannot reproduce the observed DCIT characteristics. Therefore, it is more likely that conduction through the dielectrics is involved during high-voltage off-state conditions. To prevent the situation in Figure 3.2.9–3.2.10 from occurring, holes generated by impact ionization have to be able to exit through the gate terminal.

## Case 2: Leaky Dielectrics

Charge carrier transport and trap analysis in amorphous $Si_3N_4$ dielectrics have been the subject of intense research since the mid-1980s, due to their favorable properties for use in non-volatile flash memory devices [109]. The deep acceptor and donor traps can be utilized for charge storage with exceedingly long lifetimes. These deep-level traps are also likely to influence the I-V characteristics in GaN MISHEMTs, particularly during and after high-voltage conditions. In the buffer-free devices, the acceptor trap is of primary interest because of the way that it affects the lateral field distribution in the gate-drain access region. The donor-like states are also going to affect the gate terminal's ability to sink the holes generated by the impact ionization process, assuming that trap-assisted tunneling is accounted for. Enabling the gate to absorb the holes from impact ionization means that the feedback process described in Case 1 is avoided, which, in turn, allows for higher off-state voltages.

Similar to Case 1, two donor-like Gaussian-shaped trap distributions were introduced on the GaN side of the GaN/AlN interface to prevent the current collapse phenomena presented in section 3.2.1. In the following simulations, the two traps introduced near

the AlN layer are both shallow, similar to trap $T_n$ in [Paper D]. The reason for choosing shallow traps will become clearer later.

Adjusting the acceptor trap concentration ($N_{T,A}$) in the dielectrics can change the maximum off-state $V_{DS}$ by a factor of 4 (Figure 3.2.11a). High acceptor concentrations tend to produce a significant charge build-up in the dielectrics due to electron tunneling from the gate metal, which leads to a pronounced spike in the channel electric field near the gate field plate (Figure 3.2.11b). As a result, the majority of the potential change occurs within 4 µm of the gate field plate edge towards the drain terminal. Conversely, when the acceptor concentration is reduced, the charged acceptor concentration in the dielectric is reduced as well. The injected electrons are capable of filling the positively charged surface donors along the gate-drain access region (Figure 3.2.11c), resulting in a greater depletion of the channel electron concentration (Figure 3.2.11d) and a flatter electric field profile (Figure 3.2.11b). With high acceptor concentrations, the electron trap occupation in the surface donor is lower, and only a portion of the channel access region is depleted of electrons.

Studies determining the energetic position of the acceptor state vary widely. Shallow acceptor states of 0.38 eV (relative to the conduction band minimum) to deep acceptor states at 1.6 eV have been reported using optical and electrical methods

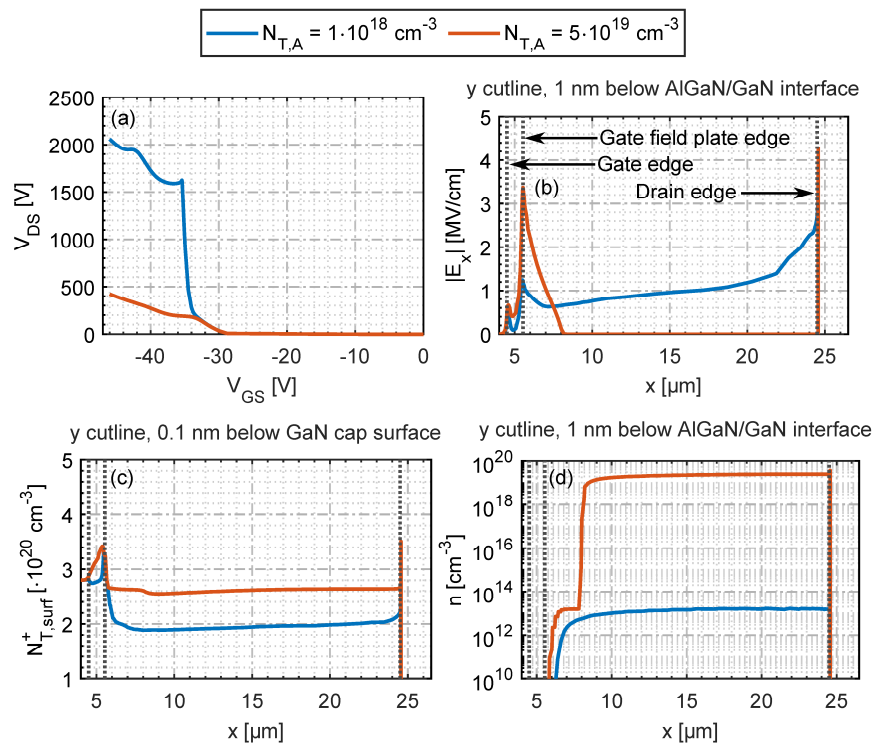


**Figure 3.2.11.** Simulations of a buffer-free MISHEMT with leaky $Si_3N_4$ layers and different acceptor trap concentrations, where (a) is DCIT characteristics, (b) is the lateral electric field near the AlGaN/GaN interface, (c) is the electron concentration near the AlGaN/GaN interface, and (d) is the concentration of trapped holes (ionized donors) near the GaN cap surface. Cutlines extracted at $V_{GS}$ = -46 V.

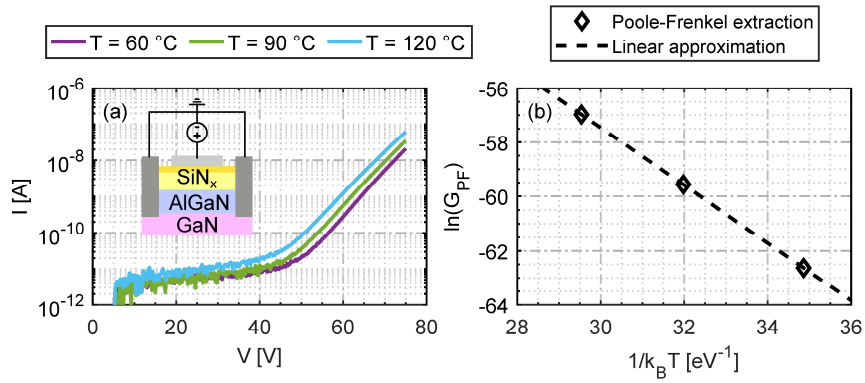


**Figure 3.2.12.** Electrical measurements on a MIS-cap structure, where (a) is the I-V characteristics of $Si_3N_4$ gate dielectric/passivation stack (with the same stoichiometry) measured at varying chuck temperatures, and (b) is the Arrhenius plot of the PF conductance. The symbols represent an average conductance of 6 devices.

(Table B3). The highly-insulating $Si_3N_4$ used in [Paper A-D] exhibits a PF behavior at high voltages (Figure 3.2.12a), i.e.

$$I \approx G_{PF} \cdot V = G_{PF,0} e^{\beta\sqrt{V} - \frac{E_0}{kT}}, \tag{3.8}$$

where $G_{PF,0}$ is a conductance pre-factor term, $\beta$ is the PF barrier lowering proportionality factor, and $E_0$ is the activation energy of the dominant defect at zero electric field.

By fitting the model parameters in Equation 3.8 to the measured I-V characteristics of the dielectrics at several temperatures, it is possible to estimate $E_0$ from the Arrhenius plot of $\ln(G_{PF})$ (Figure 3.2.12b). Using this method, an energy level of 1.06 eV was obtained. Moreover, since the dominant charge carriers are electrons, the activation energy is likely located 1.06 eV relative to the conduction band minimum. Based on reported values from the literature and the extracted trap state from the Arrhenius plot, an acceptor-type state located 1 eV below the conduction band minimum was used in the simulations. The acceptor concentrations cannot be straightforwardly extracted from the simple PF expression in Equation 3.8. Therefore, reported values from the literature (Table B3), as well as TCAD simulation tests, were used to obtain a good agreement between the measured and simulated DCT and DCIT characteristics.

As was demonstrated in Figure 3.2.11, allowing the dielectric to conduct electrons injected from the gate metal is necessary to prevent unrealistically low max off-state voltages in the buffer-free devices. However, filling the surface donors also entails a significant $I_D$ collapse after stressing at high $V_{DS}$ (Figure 3.2.13a). Notably, the surface traps will result in the largest $\partial I_D / \partial \log_{10} t$ amplitudes (Figure 3.2.13b). This strongly suggests that the 0.61 eV trap ($T_s$) extracted from DCTS in [Paper D] is surface-related. Reducing the activation energy so that the surface trap (in the simulation) is similar to the 0.19 eV trap ($T_n$) will produce a simulated DCT characteristic that does not agree with the measured characteristic in Figure 3.2.7b, since the most significant current increase would occur between 1 and 10 s instead of

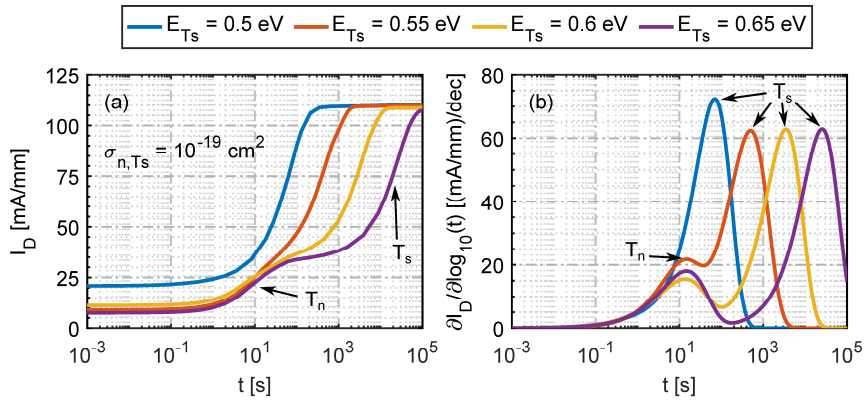


**Figure 3.2.13.** Simulated (a) DCT characteristics, and (b) the resulting log-time derivative of the DCT characteristics. The stress (filling) time, stress voltages, and on-state voltages were set to 100 s, ($V_{GSq}$,$V_{DSq}$) = (-46, 600) V, and ($V_{GS}$,$V_{DS}$) = (0, 1) V, respectively.

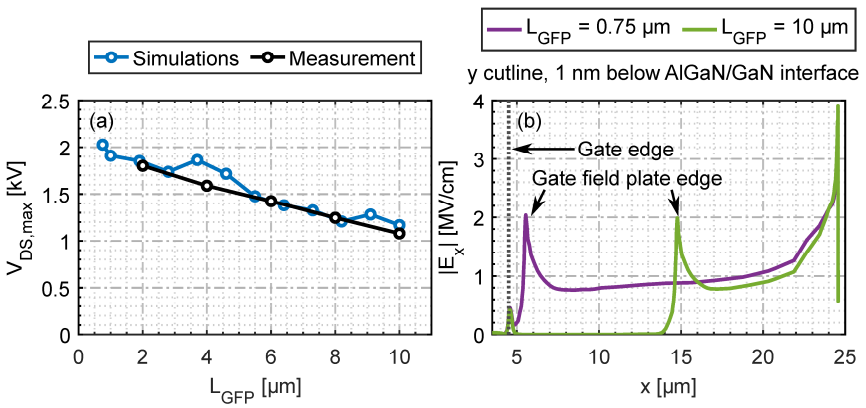


**Figure 3.2.14.** (a) Simulated and measured max $V_{DS}$ from the DCIT characteristics in buffer-free MISHEMTs with varying gate field plate lengths. (b) Lateral electric field profile in the channel for two gate field plate lengths.

the $10^3$ to $10^4$ s. It is therefore more likely that $T_s$ is surface-related and $T_n$ interface-related.

Furthermore, the model also predicts a reduction in max $V_{DS}$ with respect to $L_{GFP}$ (Figure 3.2.14a), which agrees with the measured trend in the buffer-free devices, as was also presented in Figure 2.3.9. The lateral electric field profile for a device with a long field plate ($L_{GFP}$ = 10 µm) and a short field plate ($L_{GFP}$ = 0.75 µm) is relatively similar between the gate field plate edge and the drain contact (Figure 3.2.14b). However, since the field plate edge is closer to the drain contact, the region in the access region being depleted of electrons becomes smaller due to the filling of surface states. Consequently, the region with a gradually increasing electric field profile shrinks, resulting in a lower maximum off-state voltage.

Effect of Trap $T_n$ Distribution and Concentration

By introducing two spatial donor trap distributions, $N_{Tn1}$ and $N_{Tn2}$ on the GaN side of the GaN/AlN interface, it was possible to reproduce the DCIT characteristics that were observed for the leaky sample (Figure 3.7a). The large $V_{th}$ shift is thought to be related to a relatively large spatial standard deviation for both $T_{n1}$ and $T_{n2}$ distributions (Figure 3.2.15a-b). Additionally, $T_{n1}$ and $T_{n2}$ are expected to have different spatial standard deviations, where $T_{n2}$ extends further into the GaN layer compared to $T_{n1}$. This is also similar to the SIMS profile for oxygen and hydrogen (Figure 3.2.6b), which exhibits a "double bump" similar to two Gaussian-shaped profiles. The best agreement with the measured DCIT and DCT characteristics was achieved when the two distributions had slightly different energy levels and trap cross sections. In [Paper D], the energy level (cross-section) for $T_{n1}$ was set to 0.18 eV ($5{\cdot}10^{-24}$ cm$^2$) and 0.3 eV ($5{\cdot}10^{-23}$ cm$^2$) for $T_{n2}$. These values are similar to the activation energy and cross section obtained for the $T_n$ trap from DCTS.

Making the spatial trap profile narrower around the GaN/AlN interface (Figure 3.2.15c) will result in a $V_{th}$ shift toward more positive values (Figure 3.2.15d). This could explain why the standard (low leakage) device in Figure 3.2.7a exhibits more normal DCIT characteristics. The models of the dielectric conductive properties and the interfacial donor-state energy level, concentration, and spatial spread could be further optimized to obtain better agreement with the standard device.

If the peak donor concentration at the GaN/AlN interface is reduced from $3.7{\cdot}10^{19}$ cm$^{-3}$ (Profile 1), to $3.5{\cdot}10^{19}$ cm$^{-3}$ (Profile 2), to $3.4{\cdot}10^{19}$ cm$^{-3}$ (Profile 3) (Figure 3.2.16a), a significant current collapse in the saturated $I_D$ is observed in the

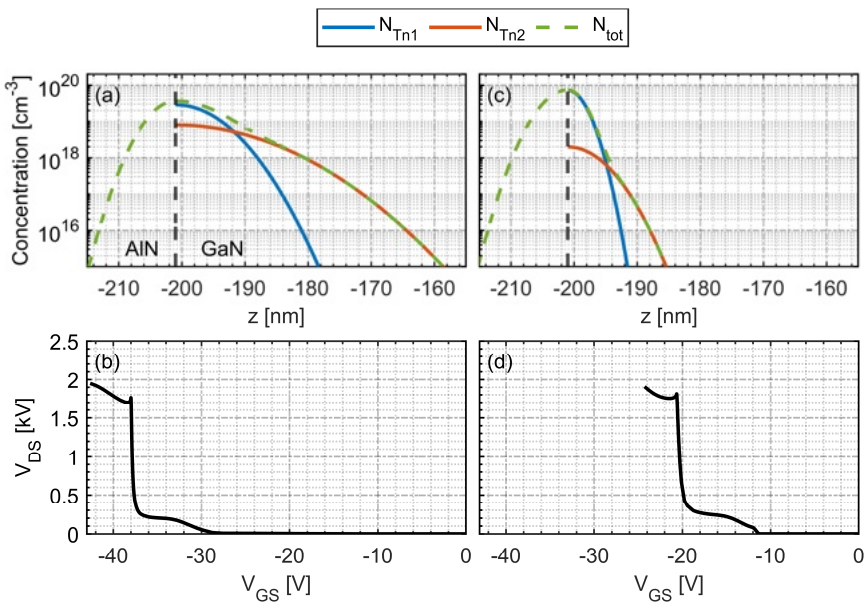


**Figure 3.2.15.** Simulations of a buffer-free MISHEMT with (a) a wide interfacial trap profile, and (c) a narrow interfacial trap profile. The resulting simulated DCIT characteristics of the wide profile and narrow profile are shown in (b) and (c), respectively.

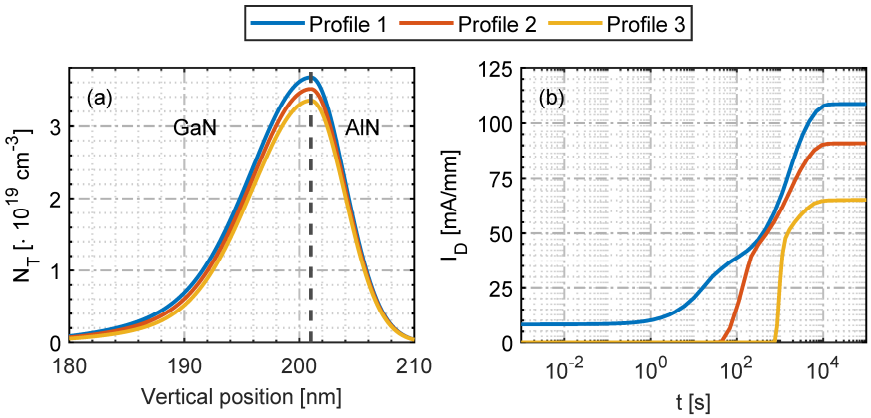


**Figure 3.2.16.** Predicted behavior of buffer-free HEMTs after reducing the donor concentration at the GaN/AlN interface, where (a) shows three donor profiles with different peak concentrations, (b) the resulting DCT characteristics.

simulated DCT characteristics (Figure 3.2.16b). By lowering the peak donor concentration, the hole concentration increases near the GaN/AlN interface (Figure 3.2.5), which, in turn, increases the *np*-product when a high $V_{DS}$ is applied in the off-state. Consequently, a larger recombination in the gate-source region, as well as the gate region, should be expected. Additionally, the outflow of holes through the gate terminal, similar to the case in Figure 3.2.3b, is also expected to increase when the donor concentration is reduced. Based on this model, a certain donor concentration is needed to prevent a current collapse of the saturated $I_D$.

## 3.3 Chapter Summary

A physics-based TCAD model was presented to explain the mechanisms responsible for the DCT and DCIT characteristics of a buffer-free GaN MISHEMT with excessive drain-source leakage. The recovery behavior seen in the DCT characteristics is indicative of two dominant traps. After comparing two different model alternatives, it was argued that a surface trap is likely responsible for the majority of the current reduction. However, the other trap seen in the DCT characteristics is thought to be related to defects and impurities near the GaN/AlN interface. These defects/impurities produce a high concentration of ionized donor states that screen the interface polarization charges. The ionized donors can, in turn, act as traps for electrons that get funneled into the region during high-voltage off-state conditions. Additionally, it is demonstrated that variations in the spatial distribution of the donor-like impurities can have a substantial impact on the $V_{th}$. A semipermanent reduction of the maximum off-state current is predicted if the donor concentration is reduced sufficiently. Therefore, a relatively high concentration of donor states is needed to prevent the current collapse from occurring.

# Chapter 4

# Characterization of Breakdown and Short-Channel Effects

In addition to vertical downscaling, reducing the lateral dimensions is of interest for power amplifier applications, and possibly more important for low-voltage classes in power electronic converters. In microwave GaN HEMTs, the current gain and power gain cut-off frequency are inversely proportional to the gate length, making it one of the most important device design parameters. In power GaN HEMTs, reducing the gate length leads to a reduction of the gate component of the total on-state resistance. Minimizing this component in fin-HEMTs [110] and fully recessed gate designs [111] is necessary to improve the PFOM (Equation 2.2). However, reducing the gate length entails more pronounced short-channel effects (SCEs), which lead to a reduction in gain and efficiency for power amplifiers, and higher off-state leakage currents for power switching devices. This effect is most commonly observed in the transistor's transfer characteristics, where it manifests as a negative shift in the $V_{th}$ at high $V_{DS}$. A new method that allows for a faster way to characterize this $V_{th}$ shift is presented and discussed in this chapter.

## 4.1 Short-Channel Effects and Drain-Induced Barrier Lowering

When a negative voltage is applied to the gate terminal in a GaN HEMT, the boundary conditions imposed by the gate result in a band bending underneath the gate, which shifts the electron quasi-Fermi level ($E_{Fn}$) away from the conduction band minimum ($E_C$) and into the band gap. If the applied gate voltage is below $V_{th}$, then the 2DEG underneath becomes depleted, and a shift of the electron concentration that originated in the gate region occurs sideways. The gate boundary conditions not only affect the band diagram in the barrier layer and near the 2DEG, but also deeper into the GaN layer. However, when applying a high positive voltage on the drain terminal, the boundary conditions imposed by the drain will start to affect the band diagram under the gate terminal (Figure 4.1.1), particularly further away from the AlGaN/GaN interface (downwards). For a long gate length device, the gate is capable

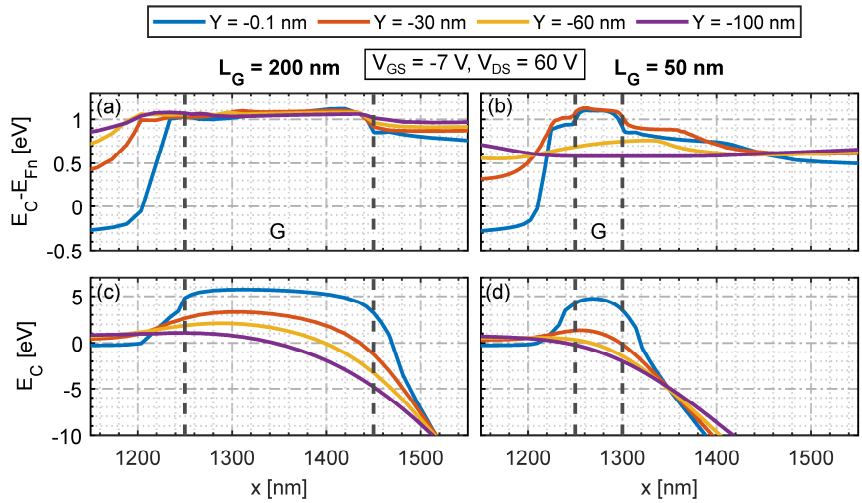


**Figure 4.1.1.** Lateral variation of the band energy levels at different y-cutlines below the AlGaN/GaN interface of a GaN HEMT with a gate length of (a,c) 200 nm and (b,d) 50 nm. The two simulated devices are biased in the off-state. The figures in the top row displays the position of $E_{Fn}$ relative to $E_C$, whereas the figures in the bottom row shows the variation of the $E_C$. The gate region is defined between dashed lines.

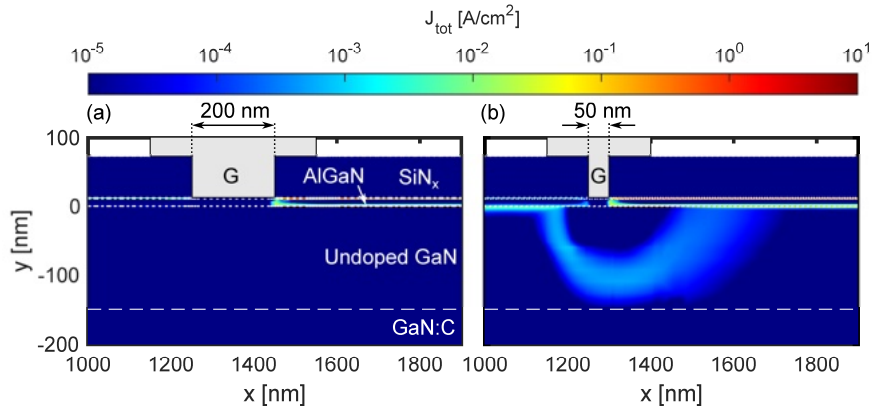


**Figure 4.1.2.** Top-view surface plots of the total conduction current density in an AlGaN/GaN with a gate length of (a) 200 nm, and (b) 50 nm.

of maintaining a relatively constant $E_{Fn}$ laterally across the gate region, and vertically into the GaN region (Figure 4.1.1a), even though $E_C$ may change significantly with respect to depth (Figure 4.1.1c). Consequently, the conduction current density underneath the gate is negligible (Figure 4.1.2a). By contrast, when the gate length is reduced, the ability of the gate terminal to pin $E_{Fn}$ deep into the band gap can become substantially degraded, particularly inside the GaN layer (Figure 4.1.1b). At the same time, a sharp decrease in $E_C$ occurs across the gate region (Figure 4.1.1d). This leads to an increase in the conduction current density between drain and source inside the GaN layer (Figure 4.1.2b).

The weakened gate modulation due to high drain voltages is considered an SCE, and typically becomes a problem for GaN HEMTs with gate lengths below 100 nm. However, GaN HEMTs with longer gate lengths may show pronounced SCEs at

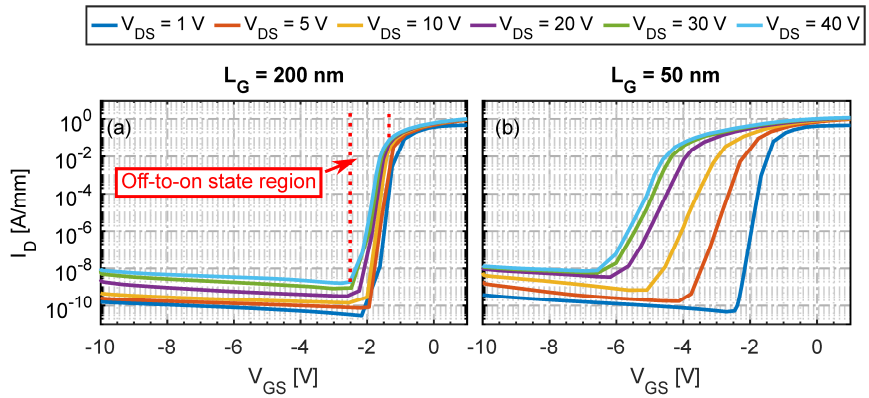


**Figure 4.1.3.** Simulated transfer characteristics of an AlGaN/GaN HEMT with a C-doped buffer and with (a) $L_G$ = 200 nm, and (b) $L_G$ = 50 nm.

voltages near the breakdown voltage. The excessive drain-source current that occurs as a result of SCEs may also reduce the breakdown voltage, since higher current densities tend to exacerbate the impact ionization rate.

Short-channel effects affect not only the drain–source buffer leakage current but also the $V_{th}$ and the saturation current in the output characteristics.. In GaN HEMT with long gate lengths, the $V_{DS}$-induced shift of the whole off-to-on state region is modest (Figure 4.1.3a). However, as the gate length of the device is reduced, the shift becomes much more pronounced (Figure 4.1.3b). The change in $V_{th}$ will be significant as well, since $V_{th}$ is defined in the off-to-on state region. The magnitude of the $V_{th}$ shifts with respect to a change in $V_{DS}$ is determined by the DIBL, which is a numerical estimate and a figure of merit for short-channel FETs. In the following sections, the definition of DIBL and the methods used to extract $V_{th}$ will be compared and discussed.

## 4.2 The Conventional DIBL Characterization Method

One of the most widely used techniques for characterizing $V_{th}$ shifts and DIBL involves the use of repeated transfer characteristics (Figure 4.2.1a-b) and can be summarized in the following four steps.

1. Establish a drain threshold current ($I_{D,th}$) at which $V_{th}$ is defined. This can be defined as a fixed current/current density, or as a percentage of the maximum drain current/current density.
2. Obtain the transistor's transfer characteristics at several $V_{DS}$.
3. Extract $V_{th}$ for all of the measured transfer, where $V_{th} = V_{GS}(I_{D,th}, V_{DS})$ (Figure 4.2.1b).
4. Calculate DIBL using

$$\sigma = -\frac{V_{th,high} - V_{th,low}}{V_{DS,high} - V_{DS,low}}, \tag{4.1}$$

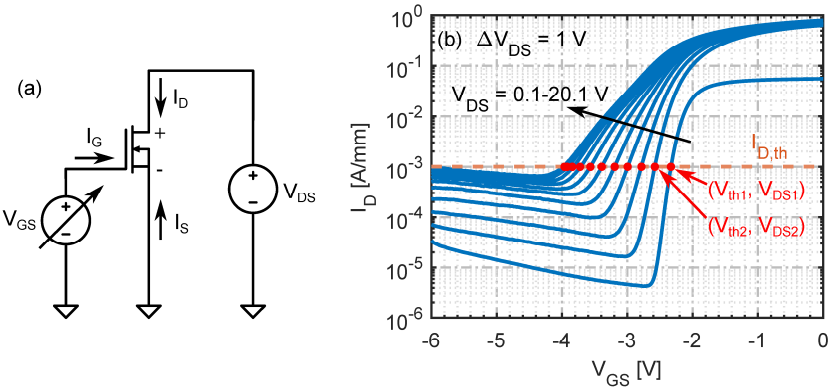


**Figure 4.2.1.** The conventional DIBL characterization technique, where (a) is the circuit diagram, and (b) is an example showing the measured transfer characteristics of a short-channel HEMT with increasing $V_{DS}$.

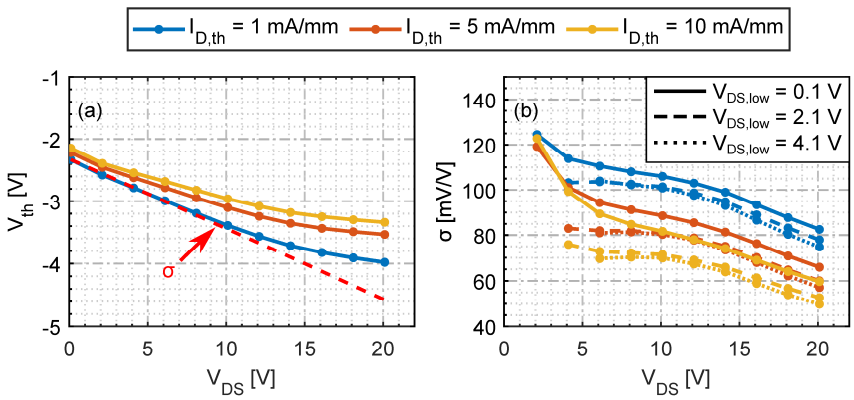


**Figure 4.2.2.** Example of the variation in (a) $V_{th}$, and (b) the DIBL with respect to $V_{DS}$ at different threshold currents of a GaN-based HEMT. All $V_{th}$ are extracted from the transfer characteristics of a short-channel HEMT. The red dashed line in (a) exhibits a linear approximation using a low-voltage reference $V_{DS}$.

where $V_{DS,low}$ is a low, pre-defined reference drain-source voltage and $V_{th,low}$ its corresponding threshold voltage, while $V_{DS,high}$ is a drain-source voltage higher than $V_{DS,low}$, with its corresponding $V_{th,high}$ that shifts towards more negative values due to SCEs.

The threshold voltage may not necessarily decrease linearly with respect to $V_{DS}$, but instead has regions where it saturates. In these cases, the original DIBL definition will not accurately capture the saturation effect, since it fundamentally expresses a linear change close to the chosen reference voltage (Figure 4.2.2a), i.e.

$$V_{th} = V_{th,low} - \sigma \cdot (V_{DS} - V_{DS,low}). \tag{4.2}$$

Therefore, using Equation 4.1 for high $V_{DS}$ deep into the saturated region will express the linear rate-of-change between $V_{th,low}$, and the saturated $V_{th}$ region, which does not necessarily reflect the actual $V_{th}$-$V_{DS}$ relationship between, or above, the two chosen $V_{DS}$ values. To account for non-linear effects, σ would itself need to be expressed using a set of empirical parameters and higher-order $V_{DS}$ terms. Alternatively, when comparing DIBL between different technologies, several DIBL values can be

**Table 4.1.** An overview of $I_{D,th}$, $V_{DS}$ values, and the corresponding σ reported in the literature for different III-nitride HEMT technologies.

| $I_{D,th}$ | $V_{DS,low}$ | $V_{DS,high}$ | σ | Epi | Reference |
|---|---|---|---|---|---|
| 10 mA/mm | 1 V | 3 V | 63 mV/V | AlGaN/GaN | [112] |
| 0.42 mA/mm | 0.5 | 50 V | 209 mV/V | AlGaN/GaN | [113] |
| N/A | 0.5 V | 10 V | 28 mV/V | InAlN/GaN | [114] |
| 10 mA/mm | 3 V | 7 V | 50-60 mV/V | InAlN/GaN | [115] |
| 1 mA/mm | 1 V | 16 V | 40 mV/V | InAlGaN/GaN | [116] |
| N/A | 1 V | 5 V | 9 mV/V | InAlN/GaN | [117] |
| 10 mA/mm | 1 V | 10 V | 57 mV/V | InAlN/GaN | [118] |
| 1 mA/mm | 5 V | 25 V | 1.15 mV/V | AlN/GaN | [119] |
| 1 mA/mm | 2 V | 10 V | 5.2 mV/V | InAlN/GaN | [120] |

presented, each expressing the $V_{th}$ shift in a specific region. However, this would also require a large set of $I_D$-$V_{GS}$ sweeps to sufficiently capture regions where $V_{th}$ changes rapidly or where it starts to saturate.

The DIBL and the $V_{th}$ shift may vary depending on the choice of $I_{D,th}$ (Figure 4.2.2a-b), especially in devices where the subthreshold swing (SS) is large and increases with respect to $V_{DS,}$ as in Figure 4.2.1b. In the literature, the choice of $I_{D,th}$ is normally set to 1 mA/mm or 10 mA/mm (Table 4.1). In this current range, the spread in DIBL may be as high as 20-25% (Figure 4.2.2b). Another source of variation is the choice of in $V_{DS,low}$, which can vary between 0.5 V and 5 V (Table 4.1). Normally, a $V_{DS}$ value in the resistive region is selected. For GaN HEMTs, these values range from 0.5 V to 2 V. Changing the $V_{DS,low}$ in this range, may also lead to a ~20 % variation (Figure 4.2.2b). Taken together, DIBL can either be 100-115 mV/V if ($I_{D,th}$, $V_{DS,low}$) is (1 mA/mm, 0.1 V), or 75-80 mV/V if ($I_{D,th}$, $V_{DS,low}$) is (10 mA/mm, 2.1 V). Therefore, using a single measure of DIBL with a somewhat arbitrarily chosen ($I_{D,th}$,$V_{DS,low}$)-pair can complicate comparisons between different device technologies.

## 4.3 Drain Current Injection Technique

The drain current injection technique (DCIT) was initially meant for analyzing different breakdown processes in FETs [121]. In conventional breakdown measurement techniques, $V_{GS}$ is held at a constant value below $V_{th}$, while the $V_{DS}$ or $I_D$ is increased. In the DCIT, a constant $I_D$ is applied while the $V_{GS}$ is reduced from an “open channel condition”, in which the transistor is biased above its threshold region, to a “depleted channel condition”, where the transistor is considered to be in the off-state (Figure 4.3.1a-b). At the same time, the $V_{DS}$ is monitored, resulting in a sharp increase in the $V_{DS}$ when the device transitions from the on-state (open channel) to the off-state (depleted channel) (Figure 4.3.1b). The $V_{DS}$ will eventually plateau, followed by a gradual increase or decrease in $V_{DS}$ as the $V_{GS}$ decreases. By simultaneously measuring $I_G$, it is possible to discern which mechanism is limiting the off-state $V_{DS}$. Consequently, one can determine whether the limiting factor is caused by a high off-state gate leakage current, avalanche current between drain and gate, or avalanche current between drain and source. However, it will only capture

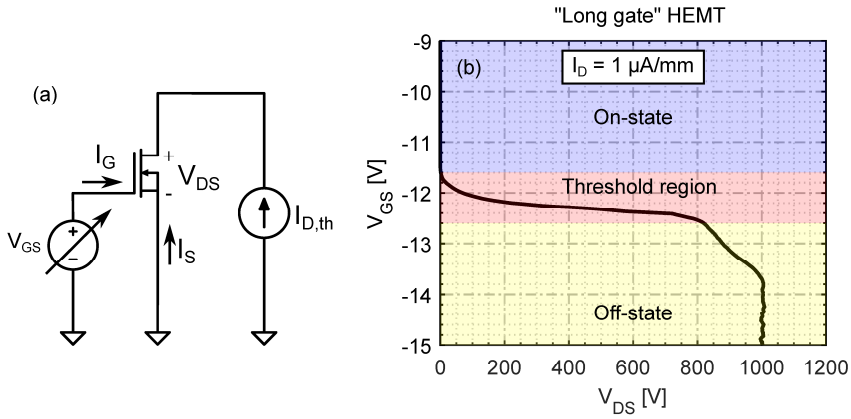


**Figure 4.3.1.** (a) Circuit diagram showing the DCIT setup, and (b) the $V_{GS}$-$V_{DS}$ characteristics of a MISHEMT with a $L_G$ = 2 µm and $L_{GD}$ = 10 µm.

$V_{GS}$-$V_{DS}$ data points for a single $I_D$, which may or may not result in the highest off-state voltage of the device. The advantage of this method is the ability to obtain data for an appropriate off-state $V_{GS}$ that can later be used when employing the conventional $V_{DS}$ or $I_D$ ramping method.

In [Paper E], it is argued that the DCIT can have a dual use, since it also provides information about the region between the on-state and off-state (Figure 4.3.1b). In this region, the $V_{GS}$ can be interpreted as the $V_{th}$ (at the specified injection current criterion, $I_{D,th}$) of the transistor. In contrast to the conventional method, the DCIT facilitates the extraction of a large set of $V_{th}$-$V_{DS}$ values in one measurement, as long as $V_{th}$ is defined in terms of a fixed $I_{D,th}$.

Additionally, the DCIT allows for the calculation of DIBL as the numerical derivative of $V_{th}$ with respect to $V_{DS}$, i.e.

$$\sigma_{DCIT} = -\frac{\Delta V_{th}}{\Delta V_{DS}}\Big|_{I_D = I_{D,th}}, \tag{4.3}$$

where $\Delta V_{th}$ and $\Delta V_{DS}$ are the incremental differences between two neighboring $V_{th}$ and $V_{DS}$, respectively. By combining the DCIT with the new definition in (Equation 4.3), a large variation in DIBL within a small $V_{DS}$ interval can more easily be observed compared to the conventional method (Figure 4.3.2a-b). The new method is therefore primarily meant to be used to compare $V_{th}$ and DIBL characteristics between different device technologies (e.g., epitaxial or gate design), as opposed to the conventional technique, where $V_{th}$ shifts and σ are extracted from two $I_D$-$V_{GS}$ sweep measurements. However, it is possible to use the new method to calculate a single figure of merit that will give an estimate of the amount of DIBL to be expected in a given operating range. The new figure of merit,

$$\tilde{\sigma}_{DCIT} = \frac{1}{V_2 - V_1}\int_{V_1}^{V_2} \sigma_{DCIT}\,(V_{DS})\, dV_{DS}, \tag{4.4}$$

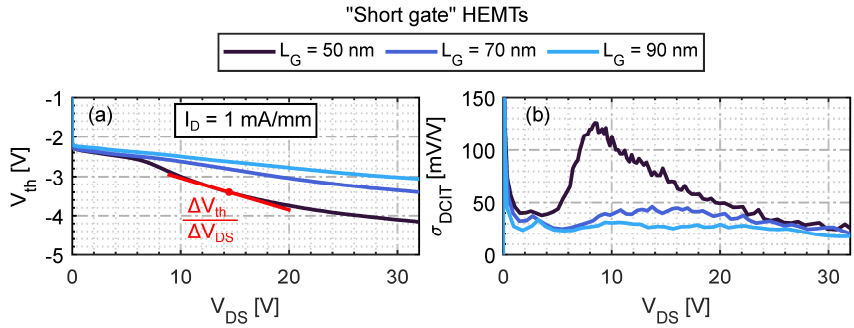


**Figure 4.3.2.** Example of (a) the $V_{th}$ characteristics, and (b) the DIBL characteristics of a HEMT with a Schottky gate with different gate lengths using the DCIT.

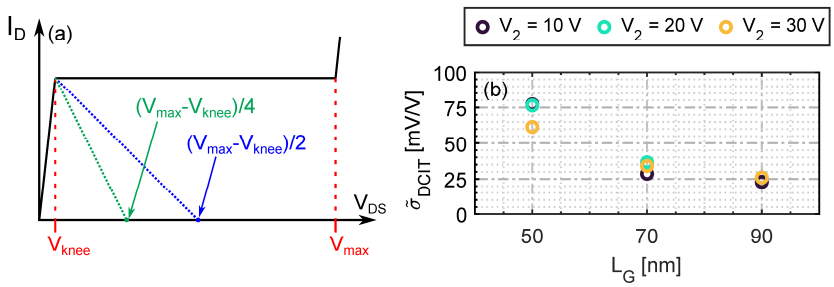


**Figure 4.3.3.** The schematic of an output characteristics in (a) demonstrates relevant voltage ranges for the calculation of $\tilde{\sigma}_{DCIT}$. The $\tilde{\sigma}_{DCIT}$ of the GaN HEMTs in Figure 4.3.2 at different upper boundaries of the $V_{DS}$ ($V_2$) ranges is shown in (d). The lower boundary ($V_1$) is set to 3 V.

expresses an average of all of the incremental $V_{th}$ shifts between two $V_{DS}$ points. For power amplifier applications, the knee voltage ($V_{DS,knee}$) is an appropriate lower end in Equation 4.4, whereas $V_2$ could be adjusted to mimic the maximum voltage in different amplifier classes (Figure 4.3.3a). The HEMTs in Figure 4.3.2a-b display a larger variation in $\tilde{\sigma}_{DCIT}$ between different $V_2$ when $L_G$ is 50 nm compared to 70 or 90 nm (Figure 4.3.3b), since the cumulative $V_{th}$ shifts are greater closer to the knee voltage.

## 4.3.1 Memory Effects and Threshold Voltage Stability

In the conventional method, the measurement equipment implements a primary ($V_{GS}$) and secondary ($V_{DS}$) voltage sweep, where the primary sweep either starts in a deep off-state and ends in an on-state (off-to-on sweep) or starts in an on-state and ends in an off-state (on-to-off sweep). The primary sweep step length is typically kept small in order to capture a sufficient number of points in the off-to-on state region, resulting in a period where the device is subjected to an off-state (or on-state) stress before $V_{th}$ is extracted. In GaN HEMTs, off-state stress—particularly at high $V_{DS}$—can force the device into a meta-stable state due to the filling of deep-level traps. Consequently, $V_{th}$ extracted from one secondary sweep will not only be affected by the pre-stressing within the same primary sweep, but also by the cumulative stresses from all previous secondary sweeps. Moreover, since $V_{th}$ shifts towards more negative voltages, the

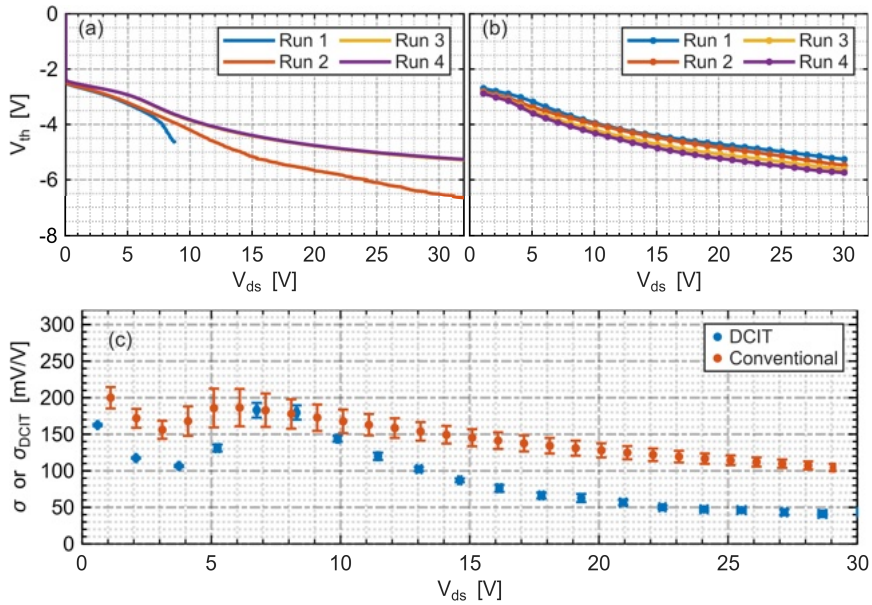


**Figure 4.3.4.** Repeated $V_{th}$ measurements using (a) the DCIT, and (b) repeated transfer characteristics. The results from the first four runs are shown. In (c), between-run variations in DIBL using the DCIT and the conventional method are shown for a post-stressed HEMT.

time spent in the off-state differs for each secondary sweep. Using repeated transfer characteristics will therefore provide a post-stressed estimate of $V_{th}$.

In [Paper E], it is shown that the DCIT reduces the pre-stressing effects, making it possible to observe the $V_{th}$ stability and estimate how much DIBL is expected in a device which starts from an equilibrium state, and how much it varies from one DCIT measurement to the next (Figure 4.3.4a). In some instances, the $V_{th}$ between first, second, and third DCIT sweeps can vary by 1-1.4 V between measurement runs before the device has reached a metastable state. By contrast, the $V_{th}$-$V_{DS}$ characteristics using the repeated transfer characteristics will not reveal the same type of run-to-run variations, since $V_{th}$ is extracted for a post-stressed device state (Figure 4.3.4b). It is also shown that the spread in DIBL between measurement runs in a post-stressed HEMT tends to be smaller when employing the DCIT compared to the conventional method (Figure 4.3.4c), further showcasing the advantages of the new method.

## 4.3.2 Impact of Heterostructure Design

The gate length is not the only aspect of the device design that affects the SCEs in GaN HEMTs. The ability to confine the electron density near the AlGaN/GaN interface through appropriate buffer design can significantly improve the gate modulation by pinning the quasi-Fermi level deep into the III-nitride layer stack through doping or incorporating an Al(Ga)N layer below the 2DEG. The improved electron confinement allows for a reduction of the gate length without suffering from severe SCEs. In this section, the impact of different heterostructure designs on $V_{th}$ and DIBL will be demonstrated.

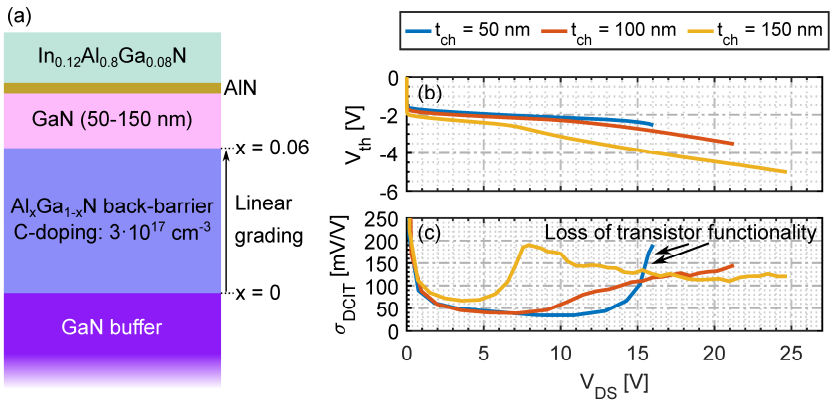


**Figure 4.3.5.** (a) Schematic of an InAlGaN/GaN heterostructure with a graded AlGaN back-barrier. The impact of the channel thickness ($t_{ch}$) on $V_{th}$ and $\sigma_{DCIT}$ is shown in (a) and (b), respectively.

Employing an AlGaN back barrier can be used to lower the requirements for effective suppression of SCEs. The larger band gap and smaller electron affinity relative to GaN can be utilized to engineer the band diagram so that the 2DEG becomes more tightly confined to the barrier/GaN interface. Due to unintentional incorporation of n-type impurities during the growth process, a certain acceptor-type compensational doping is required for the design to have the intended effect of reducing SCEs. Malmros et al. demonstrated that InAlGaN/GaN heterostructures with a graded AlGaN back-barrier and varying UID GaN channel layer thicknesses ($t_{ch}$) could be utilized to reduce the gate length from 100 nm to 50 nm while maintaining a similar DIBL and improving $f_T$ and $f_{max}$ [116]. The same type of epitaxial design was used in [Paper E] (Figure 4.3.5a), where it was shown that a $t_{ch}$ of 50 nm exhibits flatter $V_{th}$-$V_{DS}$ characteristics (i.e., a lower $\sigma_{DCIT}$) up until the transistor functionality is lost (Figure 4.3.5b-c). By contrast, thicker channel layers tend to show a large increase in $\sigma_{DCIT}$, starting in the 5-10 V range, and which is kept high up to 25 V (Figure 4.3.4c).

The thickness of the GaN channel layer in the buffer-free design can also be reduced to mitigate SCEs. Simulated $V_{th}$-$V_{DS}$ characteristics indicate that it is possible to significantly reduce the amount of DIBL by reducing the UID GaN channel thickness layer below 100 nm, thereby allowing for a sub-50 nm gate length (Figure 4.3.6a)[6]. Indeed, a HEMT with a 50 nm channel thickness and a 20 nm gate length displays lower DIBL than a HEMT with a 100 nm channel thickness and a 50 nm gate length (Figure 4.3.6b).

Chen et al. showed that DIBL could be reduced by up to a factor of 3.1 at an $L_G$ of 40 nm by growing a 150 nm layer instead of 250 nm, without seriously degrading the mobility or the sheet carrier concentration [122]. However, it remains to be seen whether a sub-100 nm GaN layer can be grown on an AlN nucleation layer without adversely affecting the crystal quality, while maintaining minimal current collapse or

[6] The simulated characteristics have not been calibrated with respect to a real buffer-free device, but serves to show the effect of reducing the GaN layer thickness.

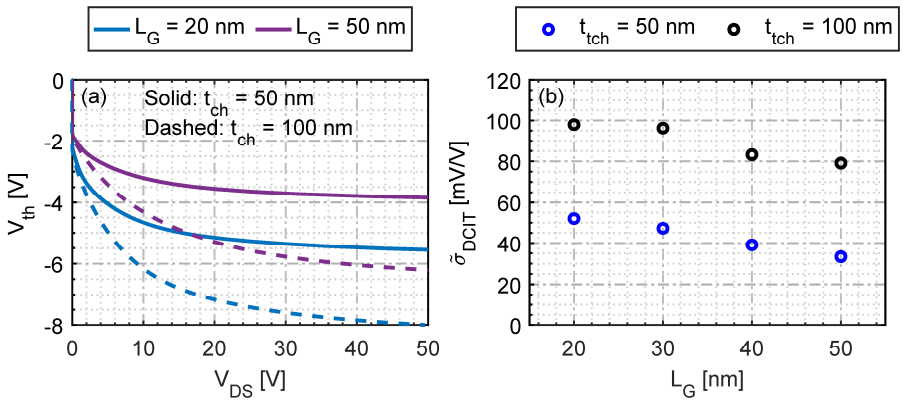


**Figure 4.3.6.** Simulated buffer-free HEMT (a) $V_{th}$-$V_{DS}$ characteristics with different channel layer thicknesses and gate lengths, and (b) the corresponding figure of merit $\tilde{\sigma}_{DCIT}$. The integral limits $V_1$ and $V_2$ used for calculating $\tilde{\sigma}_{DCIT}$ was set to 1 V and 50 V, respectively.

$R_{on,dyn}$. Nevertheless, Figure 4.3.6 demonstrates the strength of utilizing the AlN layer to improve the gate modulation of the 2DEG.

## 4.3.3 TCAD Model Parameter Optimization

In addition to the advantages of the DCIT presented so far, TCAD model parameter extraction is another area in which DCIT could excel. It is well-established that the $V_{th}$ is sensitive to process- and material-related parameters, including fluorine-based plasmas [123], oxygen-based plasmas [124], gate insulator material (for MISHEMTs) [125], gate metal [126], or channel layer thickness [122]. Furthermore, the underlying mechanisms that give rise to significant $V_{th}$ variations during high-voltage off-state conditions are, in general, complex and difficult to predict. A TCAD software facilitates testing of process and material-related parameters, and enables the analysis of the device in terms of its band structure, space charge distribution, electric field, and trap occupations.

In [Paper E], it is argued that the DCIT can significantly reduce the overall simulation time compared to the use of repeated transfer characteristics in TCAD (Figure 4.3.7a). The reduced simulation time makes it easier to test $V_{th}$-sensitive process or material-related parameters, which can be used—assuming that the model is correctly calibrated—to make predictions. Additionally, the DCIT can be implemented in an optimization algorithm to find an appropriate parameter set that results in $V_{th}$-$V_{DS}$ characteristics that agree with the measurements, while reducing the objective function evaluation time. With the DCIT, the measured and modeled $\sigma_{DCIT}$ can also be straightforwardly implemented into the objective function ($F$), e.g.,

$$F(\boldsymbol{P}) = (\boldsymbol{\Delta V_{th}}(\boldsymbol{P}))^T W(\boldsymbol{\Delta V_{th}}(\boldsymbol{P})) + (\boldsymbol{\Delta \sigma_{DCIT}}(\boldsymbol{P}))^T W(\boldsymbol{\Delta \sigma_{DCIT}}(\boldsymbol{P})), \qquad (4.5)$$

where $\boldsymbol{P}$ is the optimization parameter set, $\boldsymbol{\Delta V_{th}}$ is a vector consisting of the differences between modeled and measured $V_{th}$, $\boldsymbol{\Delta \sigma_{DCIT}}$ is a vector consisting of the differences between modeled and measured $\sigma_{DCIT}$, and $W$ is a weighting matrix. The

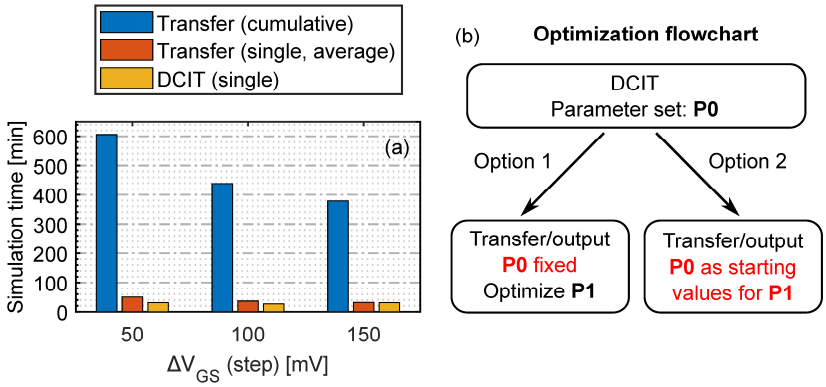


**Figure 4.3.7.** (a) A comparison of the TCAD simulation time between repeated transfer characteristics and the DCIT. In the simulations of the transfer characteristics, the $V_{DS}$ was varied between 0.1 V and 22.1 V in steps ($\Delta V_{DS}$) of 2 V. (b) Suggested optimization strategies using the DCIT.

optimized parameter set can then either be fixed or used as starting values for subsequent optimization of the transfer and output characteristics (Figure 4.3.7b).

## 4.4 Chapter Summary

Minimizing SCEs and DIBL is essential to realize high-frequency operation in laterally downscaled GaN HEMTs. Normally, DIBL is calculated through the use of repeated transfer characteristics with increasing $V_{DS}$. In [Paper D], the DCIT is instead suggested as a method to measure $V_{th}$ over a wide $V_{DS}$ range, which, in turn, can be used to calculate DIBL. In addition, the DCIT facilitates the calculation of DIBL in terms of the numerical derivative of $V_{th}$ with respect to $V_{DS}$. The method was demonstrated on different GaN HEMT technologies, including AlGaN/GaN HEMTs with an Fe-doped buffer, and InAlGaN/GaN HEMTs with a C-doped AlGaN back-barrier and different GaN channel thicknesses. Moreover, it was shown in TCAD that buffer-free GaN HEMTs with reduced channel thicknesses allowed for a reduction in gate length due to the high electron confinement in the GaN layer. Lastly, the new method allows for more efficient testing of $V_{th}$-sensitive device design parameters in TCAD, which may be useful for constructing more realistic physics-based models.

# Chapter 5

# Conclusions and Future Work

Downscaling of the III-nitride layers and the gate length are effective approaches for improving GaN HEMT performance in microwave and power electronic applications. Conventional epitaxial designs rely on the use of complex growth schemes to meet the high device performance requirements. This involves the use of superlattices, stepped Al(Ga)N layers, and compensation-doped buffer layers. By contrast, growing high-quality AlGaN/GaN heterostructures without the use of extra interlayers would reduce complexity and growth time. Additionally, utilizing the high electron confinement induced by the AlN nucleation layer allows for the simultaneous downscaling of the GaN layer and the gate length. It is in this context that the thin-channel AlGaN/GaN/AlN heterostructures have emerged as a viable alternative to the conventional epitaxial designs.

In [Paper A-B], high-voltage GaN MISHEMTs fabricated on the buffer-free epitaxial design QuanFINE® are demonstrated. In this design, the AlGaN/GaN heterostructure is grown directly on the AlN nucleation layer, without the need for extra interlayers. Furthermore, the III-nitride layers are grown on a semi-insulating 4H-SiC substrate as opposed to Si, allowing for reduced vertical leakage currents. Using highly-insulating gate dielectric and passivation layers, a sub-100 nA/mm drain-source leakage (punch-through) current at 1600 V for devices with an $L_{GD}$ of 20 µm was demonstrated. Additionally, by further improving the lateral isolation and field plate design, $V_{DS,max}$ of 1930-2000 V could be realized. Both stoichiometric gate dielectric and passivation could be employed to suppress gate leakage current without adversely affecting $R_{on,dyn}$ up to quiescent voltages of 240 V. In Chapter 2, it was also shown that increased $L_{SFP}$, $L_{GFP}$, and $L_{DFP}$ either reduced or had a negligible impact on $V_{DS,max}$. In [Paper C], it is suggested that device failure is initiated by the formation of a vertical percolation path in the $Si_3N_4$ layers directly underneath the gate field plate edge. The hypothesis is corroborated using TEM, SEM, EDS, optical microscopy, and TCAD simulations. The reduced $V_{DS,max}$ with respect to $L_{GFP}$ may therefore be related to an excessive electric field peak underneath the gate field plate edge. In order to further improve the off-state device performance, the dielectric thicknesses and field plate lengths could be further optimized. Based on the results presented in Chapter 2, a thicker $Si_3N_4$ passivation layer and a thinner $SiO_x$ 2nd dielectric should be employed. Alternatively, a slanted field plate design without

source-connected field plates could be implemented to create a more evenly distributed electric field profile in the gate-drain access region.

In [Paper D], a hypothesis is presented for the mechanism that is partially responsible for the $I_D$ collapse after stressing buffer-free MISHEMTs at high off-state voltages. It is suggested that highly ionized donor-like states near the GaN/AlN interface can capture electrons caused by a large punch-through current. Moreover, the donor-like states are also thought to be distributed spatially, which can give rise to an excessive leakage current if the tail-end of the distribution extends too deep into the GaN layer. In Chapter 3, different model alternatives were compared to the measured DCT and DCIT characteristics. Leakage from the gate metal was necessary to fill the surface donor states to prevent unrealistically low off-state breakdown voltages, and to explain the dominant emission process in the DCT characteristics. Shallow donor states with unusually low electron cross-sections are hypothesized to exist near the nucleation layer to compensate for the 2DHG that would naturally form there. The model facilitates the investigation of critical dopant parameters (e.g., peak concentration and standard deviation) and their impact on the device characteristics. Future work should be focused on exploring methods to mitigate the electron trapping of the surface states while maintaining an evenly distributed electric field profile between the gate and drain. This can involve introducing non-Ohmic vertical conduction channels along the gate-drain access region [50] or by depositing a p-type cap layer near the drain [127].

In [Paper E], the DCIT was suggested as a technique for characterizing $V_{th}$ shifts and DIBL in GaN HEMTs. The new method allows for $V_{th}$-$V_{DS}$ data acquisition over a large $V_{DS}$ range in a single measurement. By contrast, the conventional method requires a large set of $I_D$-$V_{GS}$ measurements to obtain the same results. Additionally, calculation of DIBL in terms of the derivative of $V_{th}$ with respect to $V_{DS}$ is facilitated using the DCIT as opposed to the conventional technique. A new figure of merit was also proposed using the new DIBL definition. SCEs and DIBL have traditionally been used when characterizing GaN HEMTs with gate lengths below 100 nm, since SCEs are more pronounced at low voltages in these types of devices. However, with the new technique, it is easier to estimate the amount of DIBL in HEMTs with longer gate length since the DCIT is capable of acquiring data from a few volts to thousands of volts in the same measurement. The ability to estimate DIBL in power electronic HEMTs may become more relevant when optimizing device performance through simultaneous downscaling of the gate length and the UID GaN layer thickness in double heterostructure AlGaN/GaN/AlN HEMTs. Furthermore, the DCIT can also be employed when balancing the on-state resistance and SCEs in fin-HEMTs through variation in fin length/width, or in HEMTs with recess-etched gates through variation in gate lengths. Testing the effectiveness with which different device design parameters can suppress SCEs can also be performed in a TCAD software with reduced simulation time. In conclusion, the DCIT can be used to quickly obtain information about the off-state performance, the $V_{th}$ variation, and the DIBL in GaN HEMTs.

# Appendix A

# Simulation Model Assumptions

The TCAD model used to explain the off-state and drain current recovery characteristics of the buffer-free heterostructures is based on a set of assumptions concerning initial conditions, electron transport, boundary conditions, and the selection of relevant physical models. While key assumptions are described here, not all underlying model details are explicitly stated. Relevant model parameter values used in the simulations are summarized in the tables of Appendix B.

## General assumptions

- The device is assumed to be in thermal equilibrium (constant Fermi level throughout the system) in its initial state.
- Charge carrier transport during non-equilibrium states is modeled using drift-diffusion.
- Transitions between III-nitride materials of different Al compositions are abrupt.
- Transient simulations are employed for all simulation steps (ramping and constant voltage).
- The following generation-recombination models are implemented
    - Impact ionization using Chynoweth's law [128],

$$\alpha_{n/p} = a_{n/p} e^{-\frac{b_{n/p}}{F}}, \tag{A.1}$$

which describes the number of electron-hole pairs generated over a unit length (typically in $cm^{-1}$). The parameters $a_{n/p}$ and $b_{n/p}$ are empirically-derived impact ionization parameters for electrons (n) and holes (p). The term $F$ is the driving force, which can either be equal to the electric field or the gradient of the quasi-Fermi level. For numerical stability reasons, the latter option was used in the simulations of [Paper D]. Equation A.1 is implemented into the impact ionization generation term in the continuity equations, i.e.

$$g_{ii} = \frac{1}{q}\left(\alpha_n |\boldsymbol{J_n}| + \alpha_p |\boldsymbol{J_p}|\right), \tag{A.2}$$

where $q$ is the elementary charge, and $\boldsymbol{J_{n/p}}$ is the current density for electrons (n) and holes (p). Notably, the $\alpha_{n/p}$ terms in A.1 acts as field-dependent scaling factors for the current densities.

- Shockley-Read-Hall,

$$R_{SRH} = \frac{np - n_{i,eff}^2}{\tau_p\left(n + n_{i,eff}e^{E_{trap}/k_BT}\right) + \tau_n\left(p + n_{i,eff}e^{-E_{trap}/k_BT}\right)}, \quad (A.3)$$

where $\tau_p$ is the hole lifetime, $\tau_n$ is the electron lifetime, and $E_{trap}$ is the trap energy level relative to the intrinsic Fermi level.

- Radiative (band-to-band),

$$R_{rad} = C_{rad} \cdot \left(np - n_{i,eff}^2\right), \quad (A.4)$$

where $C_{rad}$ is a proportionality factor in the order of $10^{-10}$ cm$^3$/s, and $n_{i,eff}$ is the effective intrinsic density.

- Both low-field and high-field mobility models are included.
  - Arora low-field doping-dependent mobility model [129],

$$\mu_{low} = \mu_{min} + \frac{\mu_d}{1 + \left(\frac{N_{tot}}{N_0}\right)^{\alpha}}, \quad (A.5)$$

where $N_{tot}$ is the total doping/trap concentration and $\mu_{min}$, $\mu_d$, $N_0$ and $\alpha$ are empirically-derived model parameters.

  - Caughey-Thomas high-field mobility model [130],

$$\mu(F) = \frac{\mu_{low}}{\left(1 + \left(\frac{\mu_{low}F}{v_{sat}}\right)^{\beta}\right)^{1/\beta}}, \quad (A.6)$$

where $F$ is the driving force, $v_{sat}$ is the saturation velocity, and $\beta$ is an empirical model parameter.

## Electrical contacts

- All contacts are modeled as Schottky contacts with an associated work function.
- Tunneling to/from the semiconductor regions out of/into the electrical contacts is assumed.
- The Wentzel-Kramers-Brillouin (WKB) approximation is used to model tunneling of electrons (drain, source, gate) and holes (gate) to/from the contacts. Each contact has an associated tunneling mass for electrons and holes.

## Charge carrier transport in the dielectrics

- The $Si_3N_4$ dielectrics (passivation and gate dielectric) are treated as semiconductor materials. The reason for making this assumption is twofold:
  i. To be able to conduct holes generated by impact ionization in the GaN and AlGaN layers.
  ii. To be able to conduct gate-injected electrons, which can fill surface trap states at the III-nitride/$Si_3N_4$ interface.

- Tunneling through the $Si_3N_4$/GaN interface is activated.
- Tunneling from the gate metal to the $Si_3N_4$ is activated.

These assumptions are only made in the simulations of [Paper D]. An in-depth discussion on the impact of the dielectric properties on the device characteristics is presented in Chapter 3.

## Polarization

- All III-nitride layers exhibit spontaneous polarization ($\boldsymbol{P_{sp}}$).
- The AlGaN barrier layer is assumed to be strained, resulting in a piezoelectric polarization component ($\boldsymbol{P_{pz}}$) in addition to the spontaneous polarization.
- The polarization vectors are pointing downwards relative to the surface (Ga/Al polarity). Therefore, only the z-component (along the c-axis) is non-zero,

$$\boldsymbol{P_{sp}} = \left(0,0,P_{z,sp}\right), \tag{A.7}$$

$$\boldsymbol{P_{pz}} = \left(0,0,P_{z,pz}\right). \tag{A.8}$$

- The spontaneous polarization of $Al_xGa_{1-x}N$ is calculated using

$$P_{z,sp,AlGaN}(x) = P_{sp,AlN}x + P_{sp,GaN}(1-x), \tag{A.9}$$

  where $x$ is the Al mole fraction.

- The formula presented in [131] (p. 49) was used for the calculation of the piezoelectric polarization in AlGaN, i.e.

$$P_{z,pz,AlGaN}(x) = 2d_{31}\varepsilon_1\left(c_{11} + c_{12} - 2\frac{c_{13}^2}{c_{33}}\right), \tag{A.10}$$

  where $c_{ij}$ are the elastic constants, $d_{31}$ is the piezoelectric moduli, $\varepsilon_1$ is the relative change of the relaxed and the strained in-plane lattice constants, $a_0$ and $a$, respectively. The parameters on the right-hand side of Equation A.10 are calculated using a linear interpolation between the parameter values of AlN and GaN, i.e.,

$$A_{AlGaN}(x) = A_{AlN}x + A_{GaN}(1-x), \tag{A.11}$$

  where $A$ is replaced with the parameters on the right-hand side of Equation A.10.

- A polarization calibration parameter ($\alpha_P$) was used to adjust the magnitude of the charges at the boundaries of the barrier layer using the following equation

$$\rho_P = -\alpha_P(\nabla \cdot \boldsymbol{P}). \tag{A.12}$$

  This was implemented in order to obtain a more realistic 2DEG sheet carrier concentration ($n_s$). The polarization charge was varied within 10% of the nominal values.

## Band gap and electron affinity

The electron affinity ($\chi$) and band gap ($E_g$) of the $Al_xGa_{1-x}N$ layers are calculated assuming a non-linear interpolation with a bowing factor, i.e.

$$E_{g,AlGaN}(x) = E_{g,AlN}x + E_{g,GaN}(1-x) - b_{E_g}(1-x)x, \quad (A.13)$$

$$\chi_{AlGaN}(x) = \chi_{AlN}x + \chi_{GaN}(1-x) - b_{\chi}(1-x)x, \quad (A.14)$$

where $E_g$ is the band gap energy, $b_{E_g}$ is the band gap bowing factor, $\chi$ is the electron affinity, and $b_{\chi}$ is the electron affinity bowing factor.

## Trap dynamics

The electron and hole capture rates are determined by the V-model [132], i.e.

$$c_n = \sigma_n v_{th,n} n, \quad (A.15)$$

$$c_p = \sigma_p v_{th,p} p, \quad (A.16)$$

$$e_n = \sigma_n v_{th,n} N_C e^{-\frac{(E_C - E_T)}{k_B T}}, \quad (A.17)$$

$$e_p = \sigma_p v_{th,p} N_V e^{-\frac{(E_T - E_V)}{k_B T}}, \quad (A.18)$$

where $c_{n/p}$, $e_{n/p}$, $\sigma_{n/p}$, $v_{th,n/p}$ are the local capture rate, local emission rate, capture cross section, and thermal velocity of electrons/holes ($n/p$), respectively. $E_C$ is the energy at the edge of the conduction band, $E_V$ is the energy at the edge of the valence band, $N_C$ is the effective density of states in the conduction band, $N_V$ is the effective density of states in the valence band, and $E_T$ is the energy of the trap level. The capture and emission rates are incorporated into the differential equations determining the trap occupancy ($f_{n/p}$) of electrons and holes,

$$\frac{\partial f_n}{\partial t} = c_n(1 - f_n) - e_n f_n \ \ (electrons), \quad (A.19)$$

$$\frac{\partial f_p}{\partial t} = c_p\big(1 - f_p\big) - e_p f_p \ \ (holes). \quad (A.20)$$

Equations A.19 and A.20 are, in turn, included in the continuity equations,

$$\nabla \cdot \boldsymbol{J_n} = q\frac{\partial n}{\partial t} + qN_{T,A}\frac{\partial f_n}{\partial t} + R, \quad (A.21)$$

$$-\nabla \cdot \boldsymbol{J_p} = q\frac{\partial p}{\partial t} + qN_{T,D}\frac{\partial f_p}{\partial t} + R, \quad (A.22)$$

where $N_{T,A}$, $N_{T,D}$, $R$ is the acceptor concentration, donor concentration, and remaining recombination mechanisms (e.g., impact ionization), respectively.

## Surface states

Trap states at the $Si_3N_4$/GaN cap interface are assumed. A single discrete donor state at 0.3 eV [Paper E], and 0.6 eV [Paper D] is used. Surface donor states are necessary to include in order to reproduce the measured $n_s$, as has been described by Ibbetson et al. [133]. A summary of surface donor energy levels reported in the literature can be found in Table B4. The surface donor concentration and polarization calibration parameter in Equation A. 12 were tuned to give an $n_s$ similar to the values measured in the real heterostructures. The $n_s$ was calculated by integrating the electron bulk concentration along the c-axis (z direction), i.e.

$$n_s = \int n \, dz \,. \qquad (A.23)$$

Additionally, a surface state continuum with a model similar to what is presented by Miczek et al. [134] was included in the simulations for [Paper D].

# Appendix B

# Simulation Model Parameters

Key model parameters for GaN, AlGaN, AlN, and $Si_3N_4$ that are used in the TCAD simulations are presented in the tables below. References to reported experimental and calculated values are provided. Several of the parameters listed below were also varied to test their impact on device characteristics.

**Table B1.** Model parameters of GaN.

| Parameter | Description | Reported values | Values used | References |
|---|---|---|---|---|
| $P_{sp,z,GaN}$ | Spontaneous polarization (SP)[a] | -3.4 to -2.9 μC/cm$^2$ | -2.9 μC/cm$^2$ | [135] [136] |
| $d_{31}$ | Piezoelectric moduli | -1.25·10$^{-10}$ cm/V, -1.6·10$^{-10}$ cm/V[d] | -1.5·10$^{-10}$ cm/V | [136] |
| $c_{11}$ | Elastic coefficients | 374 GPa[b] 367 GPa[c] | 367 GPa | [137][b] [138][c] |
| $c_{12}$ | | 106 GPa[b] 135 GPa[c] | 135 GPa | |
| $c_{13}$ | | 70 GPa[b] 103 GPa[c] | 103 GPa | |
| $c_{33}$ | | 379 GPa[b] 405 GPa[c] | 405 GPa | |
| $\chi_{GaN}$ | Electron affinity | 2.7 to 3.3 eV | 3.2 eV | [139]–[142] |
| $E_{g,GaN}$ | Band gap energy | 3.41 to 3.47 eV | 3.42 eV | [143] [144] [145] |
| $a_n$ | Impact ionization parameters for electrons | 2.69·10$^7$ to 4.48·10$^8$ cm$^{-1}$ [b] 2.81·10$^8$ cm$^{-1}$ [c] | 2.8·10$^8$ cm$^{-1}$ | [146][b] [147][b] [148][b] [149][c] |
| $b_n$ | | 2.27·10$^7$ to 3.4·10$^7$ V/cm[b] 3.43·10$^7$ V/cm[c] | 3.43·10$^7$ V/cm | |
| $a_p$ | Impact ionization parameters for holes | 4.32·10$^6$ to 7.13·10$^6$ cm$^{-1}$ [b] 5.41·10$^6$ cm$^{-1}$ [c] | 5.4·10$^6$ cm$^{-1}$ | [147][b] [148][b] [149][c] |
| $b_p$ | | 1.31·10$^7$ to 1.46·10$^7$ V/cm 1.96·10$^7$ V/cm | 1.96·10$^7$ V/cm | |

[a] Along c-axis [b] Experimental data [c] Calculations [d] Sentaurus TCAD default value

**Table B2.** Model parameters of AlN and $Al_xGa_{1-x}N$.

| Parameter | Description | Reported values | Values used | References |
|---|---|---|---|---|
| $P_{sp,z,AlN}$ | Spontaneous polarization (SP)[a] | -10 to -8.1 µC/cm$^2$ | -8.1 µC/cm$^2$ | [135] [136] |
| $d_{31}$ (AlN) | Piezoelectric moduli | $-2.65\cdot10^{-10}$ to $-2.3\cdot10^{-10}$·cm/V, $-2.1\cdot10^{-10}$ cm/V[e] | $-2.2\cdot10^{-10}$ cm/V | [136] [150][c] |
| $c_{11}$ (AlN) | Elastic coefficients | 345 GPa[c] 396 GPa[d] | 396 GPa | [150][c] [138][d] |
| $c_{12}$ (AlN) | | 125 GPa[c] 137 GPa[d] | 137 GPa | |
| $c_{13}$ (AlN) | | 120 GPa[c] 108 GPa[d] | 108 GPa | |
| $c_{33}$ (AlN) | | 395 GPa[c] 373 GPa[d] | 373 GPa | |
| $\chi_{AlN}$ | Electron affinity | 0.25 to 1.2 eV | 0.6 eV | [140] [139] [142] |
| $b_\chi$ | $\chi_{AlGaN}$ bowing parameter | -1 to 0 eV | -1 eV | [140] [139] [151] |
| $E_{g,AlN}$ | Band gap energy | 5.85 to 6.21 eV | 6.28 eV | [140] [152] [153] [145] |
| $b_{E_g}$ | $E_{g,AlGaN}$ bowing parameter | 1 to 1.45 eV | 1.3 eV | [140] [143] [144] [145] |

[a] Along c-axis [b] No bowing parameter assumed [c] Experimental data [d] Calculations
[e] Sentaurus TCAD default value

**Table B3.** Amorphous $Si_3N_4$ parameters.

| Parameter | Description | Reported values | Values used | References |
|---|---|---|---|---|
| $E_{g,Si3N4}$ | Band gap energy | 4.5 to 5.3 eV | 5.3 eV | [109] [154]–[156] |
| $\chi_{Si3N4}$ | Electron affinity | 1.95 to 2.15 eV[a]<br>1.35 to 2.43 eV[b] | 2 eV | [109][a] [157][a]<br>[158][b] [159][b] |
| $E_{T,A}$ | Acceptor trap level in Si3N4 below conduction band minimum | 0.38 to 1.6 eV | 1 eV | [160]–[163] |
| $N_{T,A}$ | Acceptor trap concentration in Si3N4 | $2{\cdot}10^{18}$ to $3{\cdot}10^{19}$ $cm^{-3}$ | $2{\cdot}10^{18}$ $cm^{-3}$ | |
| $E_{T,D}$ | Donor trap level in Si3N4 above valence band maximum | 0.5 to 1.8 eV | 0.5 eV | [160] [162] [164] |
| $N_{T,D}$ | Donor trap concentration in Si3N4 | $1.3{\cdot}10^{17}$ to $3{\cdot}10^{19}$ $cm^{-3}$ | $2.5{\cdot}10^{18}$ $cm^{-3}$ | [160] [162] [164] |
| $m_{t,e}$ ($\cdot m_0$) | Electron tunneling mass | 0.79 | 1 | [165] |

[a] estimated based on the valence band offset with respect to silicon
[b] estimated using a band gap of 4.5-5.3 eV and default silicon band structure properties

**Table B4.** Possible surface donor trap energy level relative to the conduction band minimum.

| Reported values | Extraction method | Distribution/discrete trap | References |
|---|---|---|---|
| 0.37 eV | DCTS, XPS | Gaussian-like distribution, peak energy position | [166] |
| 0.2 eV | TCAD fit to measurements | Discrete level | [167] |
| 0.34 eV | DLTS | N/A | [168] |
| 0.68 eV | | N/A | |
| 0.57 eV | $CI_D$-DLTS/DLOS | N/A | [169] |
| 0.6 eV | TCAD fit to measurements | Discrete level | [170] |
| 1.65 eV | Calculation and Hall measurements | Discrete level | [133] |

XPS: x-ray photoelectron spectroscopy
DLTS: deep level transient spectroscopy
$CI_D$-DLTS/DLOS: drain current deep level optical/transient spectroscopy

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