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#### **RESEARCH ARTICLE**

# **Gap Waveguide-Based MMIC Packaging Solutions for Compact RF Front-End Modules at 100 GHz**

JUAN-LUIS ALBADALEJO LIJARCIO<sup>®1,2</sup>, ABBAS VOSOOGH<sup>®1</sup>, THOMAS EMANUELSSON<sup>3</sup>, JIAN YANG<sup>®2</sup>, (Senior Member, IEEE), AND ASHRAF UZ ZAMAN<sup>®2</sup>, (Senior Member, IEEE)

Gapwaves AB, 412 63 Gothenburg, Sweden

Corresponding author: Juan-Luis Albadalejo Lijarcio (juanluis.albadalejo@gapwaves.com)

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ABSTRACT This paper presents two innovative packaging techniques for Monolithic Microwave Integrated Circuits (MMICs) designed for multilayer waveguide-based antennas operating near 100 GHz. The first technique involves a transition from a high-permittivity Gallium Arsenide (GaAs) MMIC to a rectangular waveguide using conventional bondwires as the coupling structure within the W-band. This approach enables seamless integration of any off-the-shelf RF chip into waveguide antenna modules without modifying the ground-signal-ground (GSG) pads or adding passive transition substrates. An electromagnetic bandgap (EBG) structure, implemented using metallic pins, effectively suppresses unwanted field propagation. Measurements of a back-to-back (B2B) prototype indicate a reflection coefficient below -10 dB and an average insertion loss of 0.12 dB for a single transition across a bandwidth from 90 to 97 GHz (10.5% relative bandwidth). The second technique introduces a contactless vertical transition from a high-permittivity Alumina (Al<sub>2</sub>O<sub>3</sub>) based microstrip line to a waveguide, targeting F-band applications. This proposed concept employs a patch-shaped probe placed on the substrate to couple electromagnetic waves to an H-shaped waveguide aperture positioned above the probe. Experimental results demonstrate a reflection coefficient below -10 dB and an average insertion loss of 0.17 dB over a frequency range of 102 to 120 GHz (15.3% relative bandwidth). In addition, the impact of manufacturing and assembly tolerances on the performance of both transitions is analyzed.

**INDEX TERMS** Alumina, bondwire, contactless, F-band, GaAs, gap waveguide, integration, mmWave, monolithic microwave integrated circuit (MMIC), packaging, transition, W-band, waveguide.

#### I. INTRODUCTION

The need for higher data rates has increased interest in higher frequencies, such as the sub-THz range, where larger portions of the EM spectrum are available for future wireless applications. As frequency increases, traditional PCB-based array antennas suffer from lower efficiency as a result of the high losses in the dielectric substrate. Waveguide-based antennas have emerged as an effective low-loss

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solution for higher mmWave frequency bands [1], [2]. However, active microwave circuits are typically fabricated using planar semiconductor technologies such as SiGe, GaAs, or GaN, which complicates their integration with waveguide structures. As a result, low-loss interconnection concepts are needed for MMIC to waveguide-based antenna integration.

Extensive research on microstrip-to-waveguide transitions has resulted in various designs reported in the literature. These transitions can be broadly categorized into three main configurations: on-board, on-chip, and substrate-less.

<sup>&</sup>lt;sup>2</sup>Department of Electrical Engineering, Chalmers University of Technology, 412 96 Gothenburg, Sweden

<sup>&</sup>lt;sup>3</sup>Ericsson AB, 417 56 Gothenburg, Sweden



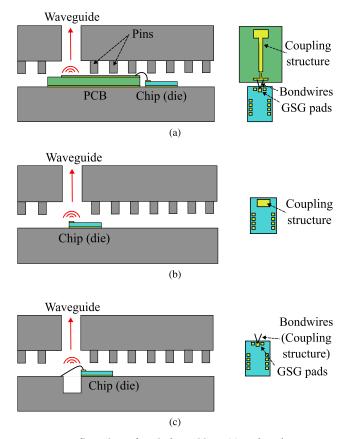


FIGURE 1. Configurations of vertical transitions: (a) On-board, (b) on-chip, and (c) substrate-less.

To illustrate these configurations, simplified examples are presented in Fig. 1. This paper reviews and analyzes representative examples from each category.

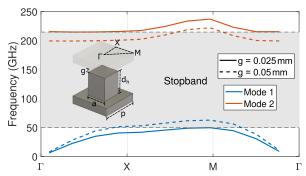
On-board transitions, also known as launcher on-board (LoB), refer to transitions where the chip is connected to an additional substrate, typically a low-permittivity material, using bondwires. A coupling structure is implemented on this additional substrate to facilitate field coupling to the waveguide. For instance, a microstrip line to ridge gap waveguide (RGW) transition using a defected ground slot at the Ku-band is presented in [3]. At the W-band, a groove gap waveguide (GGW) to microstrip line transition is demonstrated in [4], while another W-band microstrip to GGW transition employing a Chebyshev transformer is shown in [5]. Additionally, a Ka-band transition from an integrated-on-lid microstrip to RGW is detailed in [6]. These approaches are categorized as inline transitions, as the fields are coupled to a waveguide in the same plane as the chip. Despite their utility, inline transitions are less suited for integrating RF circuits into multi-layer waveguide antenna arrays due to the complexities they introduce in routing. They reduce available space for critical functions, such as biasing, Local Oscillator (LO) distribution, and Intermediate Frequency (IF) signal routing on the carrier board. To address these limitations, vertical transitions have also been explored. Examples include a Ka-band microstrip to RGW transition using a patch-shaped probe [7] and two microstrip to RGW transitions at the E-band [8]. On-board transitions offer the key advantage of requiring no modifications to the original chip. However, the inclusion of an additional substrate in these transitions can result in increased losses at higher frequencies and reduce the compactness of the transition design.

On-chip transitions are distinguished by the absence of an additional substrate, with the coupling structure directly implemented on the high-permittivity substrate to facilitate field coupling to the waveguide. Various inline implementations of this approach have been documented in the literature. For instance, two transitions from chip to GGW and RGW are described in [9]. A microstrip line to waveguide transition using an intermediate substrate integrated waveguide (SIW) at W-band is presented in [10], while a chip-to-silicon micromachined waveguide transition at D-band is detailed in [11]. Additionally, a silicon-based chip-to-RGW transition at E-band is reported in [12], and a chip-to-RGW transition at W-band is introduced in [13]. This approach offers the distinct advantage of minimizing losses by avoiding the additional propagation through an external substrate. However, it also poses significant challenges. Modifying the chip to include the transition removes the GSG pads, complicating probe-based testing due to the absence of standard test interfaces. Furthermore, on-chip transitions necessitate the co-design of the chip and waveguide package, which may not always be practical. This method also substantially increases the chip size, leading to higher manufacturing costs.

Substrate-less transitions, as described in prior literature, directly connect the chip to the waveguide structure using bondwires. All documented implementations follow the inline approach. For example, a transition at Ka-band is demonstrated in [14], while another at Ku-band is presented in [15]. A D-band transition is introduced in [16]. This method offers several advantages, including the elimination of chip modifications, which reduces both manufacturing costs and co-design time. However, it also has notable limitations. The highly inductive behavior of bondwires at very high frequencies often results in a narrow operational bandwidth. Furthermore, the performance of these transitions is susceptible to assembly precision, making them less robust for practical deployment.

This work presents two distinct variations of transitions suitable for applications around 100 GHz. The first approach employs a vertical substrate-less transition based on a bondwire technique for a GaAs substrate ( $\epsilon_r=12.94$ ). This method is advantageous for the direct integration of off-the-shelf RF chips. The second approach introduces an on-chip vertical transition from a high-permittivity Alumina substrate ( $\epsilon_r=9.9$ ) to a waveguide without galvanic contact. This transition utilizes an on-chip patch-shaped probe to vertically couple the fields to a waveguide placed above. To the best of the authors' knowledge, these are the first vertical





**FIGURE 2.** Pin-shaped EBG unit cell overlaid on the dispersion diagram of the infinite periodic structure. (p=1 mm; a=0.5 mm;  $d_h=0.6$  mm).

transitions reported on the literature for each mechanism. Both transitions are designed to achieve very low insertion loss within the frequency band of interest. B2B prototypes for both designs have been manufactured and experimentally verified. Additionally, the impact of manufacturing and assembly tolerances on the performance of both transitions has been thoroughly analyzed.

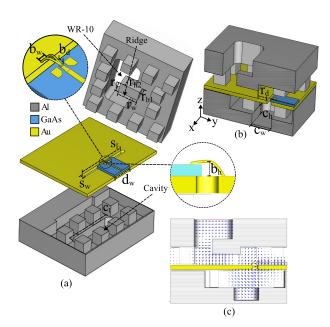
The organization of this article is as follows: Section II introduces the proposed substrate-less bondwire transition, providing an overview of the design methodology and presenting the simulation and measurement results. Section III focuses on the on-chip vertical transition, accompanied by detailed simulation and measurement analyses. Section IV compares the performance of both transitions with previous work. Finally, Section V concludes the article, summarizing the main contributions.

### II. TRANSITION A: SUBSTRATE-LESS BONDWIRE TRANSITION

#### A. EBG UNIT CELL

The design of the Electromagnetic Band Gap (EBG) unit cell is a fundamental step in developing gap waveguide technology devices. The use of pins for the packaging of microstrip circuits has been extensively documented [17], [18] and proven effective in suppressing cavity modes. The core working principle relies on the fact that no mode can propagate between a Perfect Electric Conductor (PEC) and a Perfect Magnetic Conductor (PMC) as long as the gap between them is smaller than a quarter wavelength. Various methods can be used to realize the PMC, one of the most common being the use of pins, often referred to as a "bed of nails", as employed in this paper. The primary role of the unit cell is to suppress unwanted modes and create a stopband, allowing only the desired electromagnetic waves to propagate. The proposed transition is designed to operate around 100 GHz, making the proper configuration of the EBG unit cell essential to ensure efficient wave propagation

The pin-shaped EBG unit cell considered in this design is illustrated in Fig. 2. Its dispersion characteristics are calculated using the Eigenmode Solver in CST Microwave Studio. The resulting dispersion diagram, shown in the



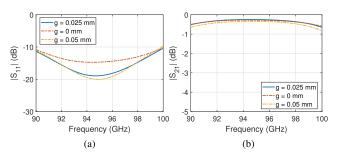
**FIGURE 3.** Proposed substrate-less vertical chip to waveguide transition. (a) Exploded view, (b) side cross-section, and (c) cross-sectional view of electric field at 95 GHz. ( $c_W = 0.85 \text{ mm}$ ;  $c_h = 0.45 \text{ mm}$ ;  $c_l = 2.5 \text{ mm}$ ;  $s_W = 0.2 \text{ mm}$ ;  $s_l = 2.7 \text{ mm}$ ;  $r_W = 0.93 \text{ mm}$ ;  $r_{h1} = 0.28 \text{ mm}$ ;  $r_{h2} = 0.56 \text{ mm}$ ;  $r_{l1} = 0.52 \text{ mm}$ ;  $r_{l2} = 0.38 \text{ mm}$ ;  $b_W = 0.05 \text{ mm}$ ;  $b_d = 0.06 \text{ mm}$ ;  $d_w = 1 \text{ mm}$ ).

same figure, indicates that no electromagnetic mode can propagate between approximately 50 and 220 GHz for a 25  $\mu \rm m$  nominal gap. This stopband behavior demonstrates the effectiveness of the proposed unit cell structure in achieving a wide operating band. Increasing the air gap to 50  $\mu \rm m$  slightly narrows the stop-band bandwidth. Unless stated otherwise, a 25  $\mu \rm m$  gap will be used in all subsequent simulations and design evaluations presented in this work.

#### **B. DESIGN OF THE TRANSITION**

The proposed transition establishes a direct connection between the chip and the metal layer using bondwires, as depicted in the exploded view in Fig. 3. This transition was first introduced in [19], where only simulation results of the initial design were presented. This design employs a GaAs substrate characterized by a relative permittivity of  $\epsilon_r=12.94$  and a thickness of  $100~\mu m$ , combined with gold bondwires measuring  $25~\mu m$  in diameter. Due to the significant inductive behavior of bondwires at high frequencies, minimizing their length is critical to maintaining a wide bandwidth. To address this challenge, a narrow etched slot is incorporated into an intermediate gold-coated brass layer to enhance bondwire attachability. This slot facilitates efficient energy coupling into the cavity below while reducing the length of the wire.

The bondwires are arranged in a V-shape to reduce overall inductance, aiding relatively wideband impedance matching. The electromagnetic energy is coupled into a  $\lambda/4$  cavity placed underneath which returns the downward-propagating fields in phase, reinforcing the upward radiation from the



**FIGURE 4.** Simulations of the proposed substrate-less bondwire transition for different gap variations. (a) Reflection coefficient, and (b) Insertion loss.

coupling slot. A ridge is introduced to improve the reflection coefficient and coupling to the vertical waveguide.

To mitigate electromagnetic field leakage through small air gaps between the top and bottom metal layers, arrays of metallic pins are integrated into both layers. Additional pins are strategically placed above the chip to suppress the propagation of undesired modes within the waveguide structure. Some prior studies have addressed mode suppression by using chips with lateral dimensions below the subcritical width [20], effectively preventing the propagation of higher-order modes. However, this method is not always practical, particularly when working with commercially available chips, where dimensional modifications are not feasible.

#### C. SIMULATION RESULTS

The simulation results of the proposed transition are shown in Fig. 4. It can be seen that the reflection coefficient remains lower than -10 dB in the frequency range of around 90 to 100 GHz (10.5% relative bandwidth). The losses are on average smaller than 0.5 dB in this band of interest. The simulation results highlight the expected variations in the gap, showing that the impact on field leakage remains negligible.

#### D. MANUFACTURING AND MEASUREMENTS

After confirming the proper performance of the proposed transition through simulations, a B2B prototype, shown in Fig. 5, was developed to evaluate its performance experimentally. While the transition design is suitable for mass production, rapid prototyping techniques such as CNC milling were used to fabricate the top and bottom layers. The thin middle layer was produced via chemical etching on a brass metal plate, followed by gold plating. The chip was placed manually and attached to the middle gold layer by using silver epoxy before wirebonding. The mechanical model incorporates both alignment pins and screws to enhance tolerance and minimize any potential misalignment. These features ensure precise positioning and secure assembly, thereby improving overall accuracy and reliability.

Due to the close spacing of the waveguide holes, an additional adapter plate was designed to fan out the ports, facilitating connection to the WR-10 flanges of the W-band

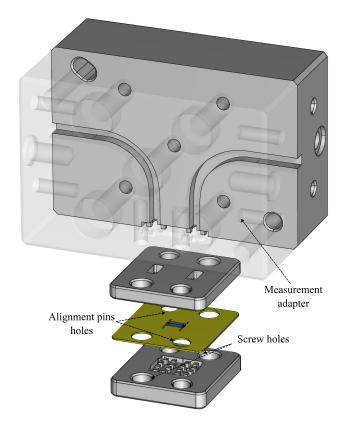


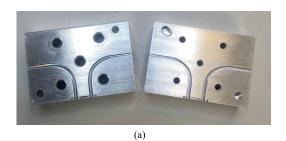
FIGURE 5. Mechanical model of the B2B prototype, illustrating the substrate-less bondwire packaging concept and the measurement adapter.

frequency extenders connected to the VNA. The adapter features a two-layer structure, split along the waveguide E-plane, ensuring minimal leakage even in the presence of minor gaps. In addition, pins have been incorporated to prevent potential leakage at the interface with the transition. Images of the fabricated components are shown in Fig. 6.

The comparison between the simulation and measurement results is shown in Fig. 7. The overall behavior aligns closely, though minor discrepancies are noticeable, particularly in the higher frequency range. The measured return loss is better than 10 dB from 90 to 97 GHz, and the insertion loss averages around 1 dB. It is important to note that this insertion loss value also includes contributions from the measurement adapter and the 1.9 mm microstrip line on the GaAs substrate. Based on additional simulations, the loss in the measurement adapter is estimated to be around 0.15 dB, while the microstrip line accounts for approximately 0.6 dB. Considering these factors, the estimated loss of a single transition is approximately 0.12 dB.

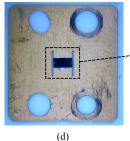
Upon closer examination of the manufactured prototype, it was found that the bondwire geometry deviates from the original design. This is evident in Fig. 6(e), where the original design is overlaid on the image of the assembled prototype. In particular, the width of the V-shape  $b_w$  and the initial location of the bond  $b_d$  are significantly larger than specified in the original design. These deviations,

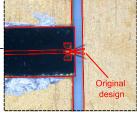










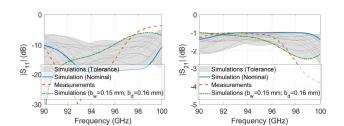


(e)



FIGURE 6. Manufactured parts of the B2B bondwire transition prototype.
(a) Measurement adapter, (b) top layer, (c) bottom layer, (d) chip

(b)



assembled on middle layer, (e) comparison of assembled prototype and

original design, and (f) assembled prototype.

FIGURE 7. Measurement results of the proposed substrate-less bondwire transition. (a) Reflection coefficient, and (b) Insertion loss.

as previously explained, substantially increase the inductance of the bondwires and negatively impact the performance. The green dashed-dotted line in Fig. 7 shows a new

**TABLE 1.** Tolerance analysis of Transition A.

Parameter	Value			
$b_w$	0.05 + 0.1 mm			
$b_d$	0.06 + 0.1 mm			
$b_h$	0.1 + 0.02 mm			
g	$0.025 \pm 0.025 \text{ mm}$			

simulation that incorporates these measured imperfections. This result aligns much more closely with the measurements, particularly at higher frequencies, which confirm that the observed geometric deviations are the primary source of the performance degradation.

Furthermore, a tolerance analysis was performed by incorporating deviations in the most critical parameters, as summarized in Table 1. The tolerance limits are derived from practical experience gained during prior assembly and prototyping activities. They represent reasonable estimates that account for typical variations introduced by manufacturing processes and manual assembly. The results, illustrated by the shaded grey area in the figure, provide a clearer understanding of the performance variability introduced by manufacturing and assembly imperfections.

#### **III. TRANSITION B: ON-CHIP VERTICAL TRANSITION**

#### A. DESIGN OF THE TRANSITION

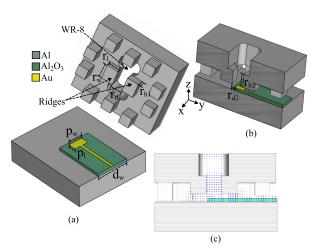
The proposed transition is illustrated in Fig. 8. This design relies on electromagnetic coupling from the probe, positioned on an Alumina substrate, which serves as a representative material for the chip's bulk substrate environment in this study. Alumina was selected for its high permittivity  $(\epsilon_r = 9.9)$ , comparable to various semiconductor materials used in MMICs. The substrate, with a thickness of 125  $\mu m$ , includes a ground plane on its backside, and the probe couples to a waveguide placed above it. The length of the probe  $l_2$  is approximately  $\lambda/2\sqrt{\epsilon_e}$ , where  $\lambda$  is the freespace wavelength, and  $\epsilon_e$  is the effective dielectric constant. To enhance the bandwidth of the transition, a stepped dual-ridge section has been incorporated. Additionally, the transition is surrounded by metallic pins, which prevent electromagnetic fields from leaking in undesired directions and suppress the propagation of unwanted modes within the waveguide. Since the EBG unit cell designed for the previous transition also covers the F-band, the same pin dimensions are utilized in this transition.

#### **B. SIMULATION RESULTS**

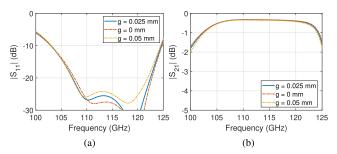
The simulation results of the proposed transition are shown in Fig. 9. It can be seen that the reflection coefficient remains lower than -10 dB in the frequency range of around 103 to 124.5 GHz (19.3% relative bandwidth). The losses are on average smaller than 0.5 dB in this band of interest.

#### C. MANUFACTURING AND MEASUREMENTS

Once the correct performance of the single transition was confirmed in the simulations, a B2B prototype, shown in



**FIGURE 8.** Proposed on-chip vertical waveguide transition. (a) Exploded view, (b) side cross-section, and (c) cross-sectional view of electric field at 110 GHz. ( $p_W=0.67~\text{mm};\ p_I=0.38~\text{mm};\ r_I=0.55~\text{mm};\ r_W=0.71~\text{mm};\ r_{d1}=0.5~\text{mm};\ r_{d2}=0.15~\text{mm};\ r_{h1}=0.38~\text{mm};\ r_{h2}=0.61~\text{mm};\ d_W=1.5~\text{mm}.$ 



**FIGURE 9.** Simulations of the proposed on-chip transition for different gap variations. (a) Reflection coefficient and (b) Insertion loss.

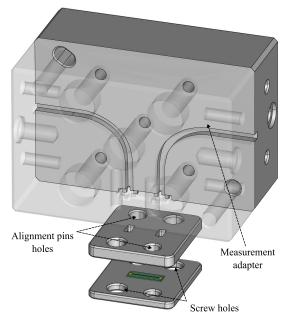
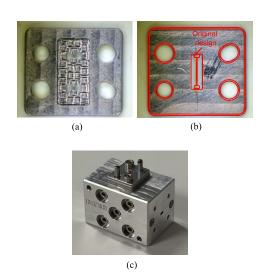


FIGURE 10. Mechanical model of the B2B prototype, illustrating the on-chip vertical transition concept and the measurement adapter.

Fig. 10 was designed and manufactured. The metal layers were manufactured by using CNC milling in Aluminum.



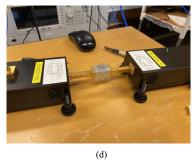


FIGURE 11. Mechanical model of the B2B prototype, illustrating the substrate-less bondwire packaging concept and the measurement adapter. (a) Top layer, (b) comparison of bottom layer with mounted chip and original design, (c) assembled prototype, and (d) measurement set-up.

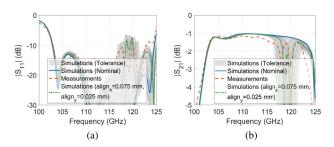


FIGURE 12. Measurement results of the proposed on-chip transition. (a) Reflection coefficient, and (b) Insertion loss.

**TABLE 2.** Tolerance analysis of Transition B.

Parameter	Value			
$align_x$	$\pm$ 0.05 mm			
aligny	$\pm$ 0.1 mm			
g	$0.025 \pm 0.025 \text{ mm}$			

The chip was manually aligned and glued on the bottom metal layer under a microscope. Some images of the fabricated parts are presented in Fig. 11. Similar to the previous transition, an adapter plate was employed to facilitate connection to the WR-8 flanges of the F-band frequency extenders connected to the VNA.



TABLE 3. Performance comparison between the proposed transitions and previous work.

Topology	Orientation	Transition	Substrate $(\epsilon_r)$	Frequency [GHz] <sup>a</sup>	Bandwidth [%]	Insertion loss [dB] b
On-board	Inline	[3]	RT-Duroid 5880 (2.2)	11.8-18.8	45	0.25
		[4]	Quartz (3.8)	90-100	10.5	1.75-3
		[5]	CuClad 233 (2.34)	85-104	20	1
		[6]	RT-Duroid 5880 (2.2)	26.9-38.3 (RL>15dB)	35	0.31-0.83
	Vertical	[7] °	RO4350B (3.66)	Type 1: 25-31.7 Type 2: 25.3-30.7 Type 3: 24.5-30.3	24 19.2 21.2	<0.62 <0.6 <0.49
		[8]	RO3003 (3)	A: 75-83 B: 69-86	10.1 21.9	A: 1.5 B: 1.5
On-chip	Inline	[9]	Alumina (9.9) d	54.2-71.6	27.75	0.5
		[10]	Alumina (9.9) d	72-95.5	28	0.7
		[11]	SiGe (4)	135-160 (RL>5dB)	17	4.2-5.5
		[12]	SiGe (4.1)	69-90	26.4	1.55-1.9
		[13]	GaAs (12.94)	85-105	21	0.5-0.75
	Vertical	Transition B	Alumina (9.9) d	102-120	15.3	0.17
Substrate-less	Inline	[14]	RO4003 (3.55)	33.3-36.7	9.5	0.8
		[15]	Alumina (9.9) d	11-14.5	27	0.75
		[16]	GaAs (12.94)	149-170	13	0.8
	Vertical	Transition A	GaAs (12.94)	90-97	10.5	0.12

<sup>&</sup>lt;sup>a</sup> Reported operating frequency band for a return loss better than 10 dB unless otherwise specified.

The measured S-parameters are presented in Fig. 12. It is evident that some resonances appear in the measurements, significantly narrowing the bandwidth. Upon closer inspection of the manufactured components, it was determined that the chip was not properly aligned during manual assembly, clearly seen in Fig. 11(b). When these misalignments were included in the model, the updated simulations plotted as the green dash-dotted line exhibited the same resonant peaks seen in the measurements. These resonances were attributed to an unwanted resonant mode between the ridges of the top plate and the bottom plate, with the loading effect of the Alumina dielectric in between. This issue can be easily addressed by reducing the width of the ridge, which would shift the resonant frequencies outside the desired frequency band. Despite this, the reflection coefficient remains below  $-10 \, dB$ , and the average insertion loss remains below 1.25 dB across the 103-120 GHz band (15.3% relative bandwidth). As with the previous transition, the insertion loss value also includes contributions from the measurement adapter and the 3.75 mm microstrip line on the Alumina substrate. Additional simulations estimate the loss in the measurement adapter to be around 0.2 dB, while the microstrip line contributes approximately 0.7 dB. Taking these factors into account, the estimated loss for a single transition is around 0.17 dB.

Moreover, a tolerance analysis was carried out by including the most critical deviations listed in Table 2. The resulting performance envelope, shown as the shaded gray region in Fig. 12, highlights the range of variation that manufacturing and assembly imperfections can introduce.

#### IV. COMPARISON TO STATE-OF-THE-ART

To evaluate the performance of the proposed transitions, Transition A and Transition B are compared against previously reported designs summarized in Table 3. The comparison focuses on parameters such as operating frequency range, bandwidth, and insertion loss.

Transition A, a vertical substrate-less design based on GaAs, operates within a frequency range of 90-97 GHz, achieving a bandwidth of 10.5% and an exceptionally low insertion loss of 0.12 dB. Compared to other substrate-less vertical transitions, Transition A offers superior performance in terms of insertion loss. Although its bandwidth is slightly narrower than that of previously reported designs, this work represents the first implementation of a vertical transition using the substrate-less approach.

Transition B, an on-chip vertical transition using Alumina, operates within the 102-120 GHz frequency range, achieving a bandwidth of 15.3% and an insertion loss of 0.17 dB. This result surpasses other on-chip designs in terms of insertion loss while maintaining a relatively wide bandwidth.

These improvements highlight the effectiveness of the proposed designs for high-frequency applications and their potential for integrating RF chips into waveguide-based antennas.

#### **V. CONCLUSION**

This work presents two innovative packaging techniques for integrating MMICs designed for high-frequency waveguide antenna systems around 100 GHz. The first technique employs a bondwire-based transition from a high-permittivity

<sup>&</sup>lt;sup>b</sup> Insertion loss for a single transition.

<sup>&</sup>lt;sup>c</sup> Only simulation results are provided.

<sup>&</sup>lt;sup>d</sup> Representing chip's bulk substrate.



GaAs MMIC to a rectangular waveguide for W-band applications. It achieves a reflection coefficient below -10 dB and an average insertion loss of approximately 0.12 dB across a 10.5% relative bandwidth (90-97 GHz). This method is well-suited for integrating any off-the-shelf RF chips without modification, thereby reducing both manufacturing costs and co-design time. The second technique introduces a contactless vertical transition from an Alumina-based microstrip line to a waveguide for F-band applications. It achieves a reflection coefficient below -10 dB and an average insertion loss of 0.17 dB across a 15.3% relative bandwidth (102-120 GHz). Although this method requires modifications to the chip, it achieves a higher bandwidth while maintaining very low loss performance. The experimental results for both techniques, designed for multilayer waveguide applications, demonstrate their effectiveness in achieving low reflection and insertion loss, while also accounting for manufacturing and assembly tolerances.

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JUAN-LUIS ALBADALEJO LIJARCIO was born in Spain. He received the B.Sc. degree in telecommunications technology engineering from the University of Jaen, Spain, in 2016, and the M.Sc. degree in electrical engineering from the KTH Royal Institute of Technology, Sweden, and the Polytechnic University of Catalonia, Spain, in 2020. He is currently pursuing the Ph.D. degree with the Chalmers University of Technology. He is an Antenna Engineer with Gapwaves AB.



**ABBAS VOSOOGH** received the M.Sc. degree from the K. N. Toosi University of Technology, Tehran, Iran, in 2011, and the Ph.D. degree from the Chalmers University of Technology, Gothenburg, Sweden, in 2018. He is currently the Director of technology and innovation with Gapwaves AB, Sweden. His current research interests include system integration and packaging for millimeter- and submillimeter-wave applications, metasurfaces, passive components, and planar

array antenna design. He was a recipient of the Best Student Paper Award from the 2015 International Symposium on Antennas and Propagation, TAS, Australia, the CST University Publication Award, in 2016, the Best Paper Award and the Best Student Paper Award from the 2016 International Symposium on Antennas and Propagation, Okinawa, Japan, the First Prize Student Award from the 2017 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting, San Diego, CA, USA, and the 2019 EurAAP Kildal Award for Best Ph.D. in Antenna and Propagation.





**THOMAS EMANUELSSON** received the Master of Science degree in electronic engineering from the Chalmers University of Technology, Gothenburg, Sweden, in 1984. He is currently holding a position as a Senior Expert of microwave and sub-THz technology with Ericsson AB, Gothenburg, and also a position as an Adjunct Professor with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University of

Technology. He has extensive background in mmWave radio communication, radar phased array systems, and monolithic microwave integrated circuit (MMIC) technology.

the Department of Signals and Systems, Chalmers University of Technology. In 2010, 2016, and 2020, he was an Associate Professor, a Professor, and a Full Professor, respectively, with the Department of Electrical Engineering, Chalmers University of Technology. He has authored more than 100 journal articles and about 200 peer-reviewed conference papers (H-index: 35 and i10-index: 107). His research interests include ultra-wideband antennas and UWB feeds for reflector antennas, mmWave antennas, mmWave multilayer phased array antennas, mmWave sheet waveguide element (SWE) antennas, gap waveguide antennas, UWB radar systems, UWB antennas in near-field sensing applications, hat-fed antennas, reflector antennas, radome design, and computational electromagnetics.



JIAN YANG (Senior Member, IEEE) received the B.S. degree in electrical engineering from Nanjing University of Science and Technology, Nanjing, China, in 1982, the M.S. degree in electrical engineering from Nanjing Research Center of Electronic Engineering, Nanjing, in 1985, and the Swedish Licentiate and Ph.D. degrees from the Chalmers University of Technology, Gothenburg, Sweden, in 1998 and 2001, respectively. From 1985 to 1996, he was a Senior

Engineer with Nanjing Research Institute of Electronics Technology, Nanjing. From 1999 to 2005, he was a Research Engineer with the Department of Electromagnetics, Chalmers University of Technology. From 2005 to 2006, he was a Senior Engineer with COMHAT AB, DSML, Sweden. From 2006 to 2010, he was an Assistant Professor with



ASHRAF UZ ZAMAN (Senior Member, IEEE) was born in Chittagong, Bangladesh. He received the B.Sc. degree in electrical and electronics engineering from Chittagong University of Engineering and Technology, Chittagong, in 2001, and the M.Sc. and Ph.D. degrees from the Chalmers University of Technology, Gothenburg, Sweden, in 2007 and 2013, respectively. He is currently an Associate Professor with the Communication and Antenna Systems Division, Chalmers University

of Technology. His current research interests include high-gain millimeterwave planar antennas, gap waveguide technology, frequency-selective surfaces, microwave passive components, RF packaging techniques, and low-loss integration of MMICs with the antennas.

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