Thesis for The Degree of Licentiate of Engineering

Analog Linearization of Highly Efficient Supply-Modulated Power Amplifiers

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To my dear father Paul, who sadly passed away on the 23rd of November 2024, who has been my inspiration to pursue a degree in Electrical Engineering, giving his enduring support through thick and thin.

"We're lost in a cloud
With too much rain
We're trapped in a world
That's troubled with pain
But as long as a man
Has the strength to dream
He can redeem his soul and fly."
– Elvis Presley

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Abstract

The increasing demand in the global wireless data traffic imposes a set of new requirements and challenges for the development of the wireless communication infrastructure. At microwave frequencies the Power Amplifier (PA) tends to suffer from increased Radio Frequency (RF) losses and a reduction in output power levels, effectively yielding reduced energy efficiency. Thus, it is crucial to investigate efficiency enhancement techniques to improve the back-off efficiency.

In the first part of this thesis the concept of supply modulation is introduced. An analysis of the benefits and drawbacks of various supply modulator topologies is discussed. Based on this analysis two reconfigurable laboratory-grade supply modulator implementations are presented. The first design employs a push-pull output stage, while the second design exhibits a parallel load-sharing output stage topology. The manufactured Printed Circuit Boards (PCBs) achieve a high half-power (3-dB) bandwidth of 130 MHz with a maximum linear output current exceeding 2.5 A.

The second part of this thesis discusses a novel analog phase correction method for a K-band (18 – 27 GHz) 4 W PA in a 150 nm GaN-on-SiC technology, implemented with a custom tuneable phase modulator Monolithic Microwave Integrated Circuit (MMIC) directly in the PA RF input path. The phase modulator exhibits an inverse response compared to the PA for linearization. Modulated measurements are performed with a 33.75 MHz 16-QAM input signal with 6 dB Peak-to-Average Power Ratio (PAPR) at a frequency of 20.5 GHz. With supply modulation the average Power-Added Efficiency (PAE) is improved by 6.5 – 9.5 percentage points (pp) for a variety of tracking functions. The PA output phase variation is reduced from 30° to 14° with phase correction. Simultaneously, the Adjacent Channel Power Ratio (ACPR) improves by 2 – 5 dB, resulting in similar or even better linearity performance compared to a static 20 V bias, while a significantly higher average PAE is achieved.

Overall, this thesis provides a comprehensive overview of the benefits and drawbacks of supply modulation for energy efficiency enhancement. The main findings contribute to the development of highly efficient and linear RF transmitters for future wireless communication systems.

Keywords

Energy Efficiency, Monolithic Microwave Integrated Circuits, Non-Linear Distortion, Phase Shifter, Power Amplifiers, Pre-Distortion, Supply Modulation

List of Publications

Appended Publications

This thesis is based on the following publications:

[**A**] **R. Vissers**, C. Fager, M. R. Duffy, Z. Popović, G. Lasser, "Tuneable Analog Phase Correction for Drain-Modulated Power Amplifiers," Submitted to *IEEE Trans. Microw. Theory Techn.*, Jul. 2025.

[**B**] **R. Vissers**, C. Fager, G. Lasser, "VNA-Based Large-Signal Drain-Modulated Power Amplifier Measurement Setup With Digital Pre-Distortion," in *Proc. 101st ARFTG Microw. Meas. Conf.*, San Diego, CA, USA, 2023, pp. 1–4.

Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

[**a**] Z. Liu, G. Kaval, **R. Vissers**, G. Lasser, "An 8-Way E-Band GaAs Power Amplifier Utilizing Shared-Ground Vias," Accepted for *IEEE Topical Conf. Power Amplifiers Wireless Radio Appl. (PAWR)*, Los Angeles, CA, USA, 2026.

[**b**] H. Zaheri, **R. Vissers**, H. Zhou, G. Lasser, "A 10 W GaN/Si Doherty Power Amplifier Designed for 15 GHz 6G Band With 8 dB Backoff Efficiency," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millimetre-wave Circuits (INMMiC)*, Torino, Italy, 2025, pp. 1–4.

[**c**] **R. Vissers**, C. Fager, G. Lasser, "K/Ka-Band Eight-Way Power-Combined Power Amplifier in 180 nm E-Mode GaAs," in *Proc. IEEE Topical Conf. Power Amplifiers Wireless Radio Appl. (PAWR)*, San Juan, PR, USA, 2025, pp. 26–28.

[**d**] Z. Liu, **R. Vissers**, G. Lasser, "A 15 GHz Stacked GaAs Power Amplifier for Potential 6G Application," in *Proc. IEEE Topical Conf. Power Amplifiers Wireless Radio Appl. (PAWR)*, San Juan, PR, USA, 2025, pp. 23–25.

[**e**] **R. Vissers**, H. Zirath, G. Lasser, "High-Efficiency Ka-Band Active Frequency Doubler MMIC in 150 nm GaN/SiC HEMT Technology," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millimetre-wave Circuits (INMMiC)*, Aveiro, Portugal, 2023, pp. 1–3.

[**f**] G. Lasser, **R. Vissers**, "A Push-Pull 6 – 12 GHz GaN Dual-Stage MMIC PA With Capacitive Cross-Coupling Neutralization for Increased Gain," in *Proc. 18th Eur. Microw. Integr. Circuit Conf. (EuMIC)*, Berlin, Germany, 2023, pp. 76–79.

Acronyms

ACPR – Adjacent Channel Power Ratio
AM – Amplitude Modulation
APD – Analog Pre-Distortion
AWG – Arbitrary Waveform Generator
BEOL – Back End-of-Line
BJT – Bipolar Junction Transistor
CMOS – Complementary Metal-Oxide-Semiconductor
CW – Continuous Wave
DAC – Digital-to-Analog Converter
DFT – Discrete Fourier Transform
DPD – Digital Pre-Distortion
DR – Dynamic Range
EM – Electro-Magnetic
ET – Envelope Tracking
EVM – Error Vector Magnitude
FR3 – Frequency Range 3
FWA – Fixed Wireless Access
GaAs – Gallium Arsenide
GaN – Gallium Nitride
HEMT – High Electron Mobility Transistor
IF – Intermediate Frequency
IoT – Internet of Things
IQ – In-Phase/Quadrature
LMBA – Load-Modulated Balanced Amplifier
LO – Local Oscillator
MMIC – Monolithic Microwave Integrated Circuit
op-amp – Operational Amplifier
PA – Power Amplifier
PAE – Power-Added Efficiency
PAPR – Peak-to-Average Power Ratio
PCB – Printed Circuit Board
pp – Percentage Points
PSD – Power Spectral Density
PT – Power Tracking

PT2 – Second-Order Power Tracking
PT2R – Reduced Second-Order Power Tracking
PWM – Pulse-Width Modulation
QAM – Quadrature Amplitude Modulation
RF – Radio Frequency
RMS – Root Mean Square
SA – Spectrum Analysis
SATCOM – Satellite Communications
Si – Silicon
SiC – Silicon Carbide
SNR – Signal-to-Noise Ratio
SOLT – Short-Open-Load-Through
VCCS – Voltage-Controlled Current Source
VCVS – Voltage-Controlled Voltage Source
VISA – Virtual Instrument Software Architecture
VNA – Vector Network Analyzer

Contents

Chapter 1

Introduction

1.1 Motivation

The rapid growth of global mobile data traffic has revolutionized the wireless communications sector. Never has the world been so connected with applications spanning from video calling, text messaging, and social media to high-definition video streaming, remote computing, Internet of Things (IoT), and even Satellite Communications (SATCOM). A recent Statista review shows that in 2023 a grand total of 123 ZB of data was created and consumed worldwide [1]. The forecast shows that in the year 2028 there will be almost four times as much data being consumed. Constant development in the wireless sector ensures that the data throughput can meet these increasing demands. According to a report from Ericsson the global mobile network data traffic is currently dominated by the Fixed Wireless Access (FWA) 4G and 5G standards with 165 EB/month in 2024 [2], as presented in Fig. 1.1. Moreover, the projection shows an expected twofold increase in 2028 and the prediction exceeds 400 EB/month in 2030.

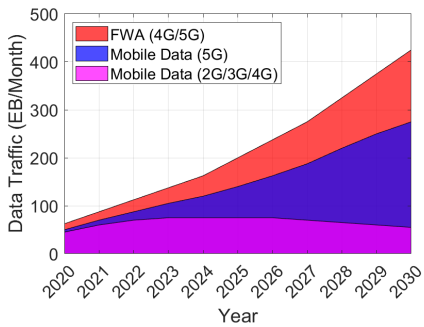


Figure 1.1: Projection of global mobile network data traffic over the years [2].

Consequently, development of wireless communication infrastructure is facing a variety of challenges to allow for high-speed and high-capacity throughput with low deployment costs [3], [4]. The main challenges to address are

bandwidth and efficiency. According to the famous Shannon equation [5], the channel capacity, C, is defined as

$$C = B \cdot \log_2 (1 + \text{SNR}), \tag{1.1}$$

where B is the bandwidth and SNR is the Signal-to-Noise Ratio. This equation shows how much information can be transmitted reliably through a channel for a specified bandwidth and SNR. Preferably, the bandwidth is a large as possible to obtain very high data rates. However, wideband modulated signals with a high Peak-to-Average Power Ratio (PAPR) have to adhere to stringent band requirements due to the spectrum scarcity at microwave frequencies, which requires careful frequency planning [6]. Any potential non-linearities will result in unwanted spectral regrowth and out-of-band emissions.

Efficient power handling is arguably the most important aspect of present-day handsets and cellular base stations [7], [8]. A high efficiency is desired to reduce heat generated in a transmitter, or else costly cooling equipment has to be employed. More than 50% of the power dissipated in a transmitter comes from the Power Amplifier (PA) [9]. This component is specifically designed to amplify signal power and exhibit a high output power over a broad frequency range, while maintaining as high as possible efficiency through efficiency enhancement techniques.

Commonly used efficiency enhancement techniques are load modulation and supply modulation. Active load modulation topologies employ multiple parallel PAs operating in different bias classes, where the outputs are connected through a combiner network to improve the back-off efficiency. Examples are the Doherty PA [10], [11], the outphasing PA [12], [13], and the Load-Modulated Balanced Amplifier (LMBA) [14], [15]. These architectures can achieve high efficiency at output back-off levels of 9 – 12 dB with increased design complexity.

An alternative to these implementations is supply modulation, which is often implemented as Envelope Tracking (ET) [16]. This method dynamically varies the supply voltage of the PA based on the Radio Frequency (RF) input power level, which in turn improves the back-off efficiency [17]. However, the main complexity is introduced by designing a high-speed and highly efficient supply modulator [18]. Another challenge to address is linearity, which is compromised as the gain and phase characteristics change when the supply voltage is varied [19], [20].

1.2 Thesis Scope and Outline

This thesis focuses on the theory, design, and validation of an analog phase linearization technique for highly efficient supply-modulated PAs. A theoretical background on supply modulation is provided, which is backed by a practical implementation with promising measurement results.

Chapter 2 gives an introduction on supply modulation, discussing the benefits and challenges that arise. A series of tracking functions are introduced to overcome bandwidth limitations imposed by the envelope. This chapter is

complemented with an overview of common semiconductor topologies, followed by the fundamentals of PA design.

In Chapter 3 the main design considerations for supply modulators are presented. A theoretical background is provided on four common supply modulator topologies, showing both discrete and continuous designs. Afterwards, these topologies are compared to each other.

Chapter 4 presents the design and characterization of two reconfigurable laboratory-grade continuous supply modulators. The first design employs a push-pull output stage for high output current handling [Paper B], while the second design combines multiple operational amplifiers (op-amps) in parallel to attain a high linear output current [Paper A].

In Chapter 5 the Vector Network Analyzer (VNA)-based modulated measurement setup with drain modulation capability is discussed [Paper A, B]. An in-depth explanation is given regarding coherence and calibration of the setup to allow for highly accurate measurements.

Chapter 6 presents the novel tuneable analog phase linearization method for supply-modulated PAs [Paper A]. The system level overview is discussed and all individual components of the manufactured amplifier are discussed in more detail. Both Continuous-Wave (CW) and modulated measurement results are given to validate the effectiveness of the phase correction.

Finally, Chapter 7 concludes the thesis, giving a summary of the key findings and providing a future outlook.

Chapter 2

Supply Modulation Theory and Challenges

This chapter will provide a theoretical background on supply modulation, as well as available semiconductor technologies and fundamentals of PA design. Section 2.1 gives a comparison of device characteristics for Gallium Nitride (GaN), Gallium Arsenide (GaAs), and Complementary Metal-Oxide-Semiconductor (CMOS) technologies. Section 2.2 provides the fundamentals of PA design, discussing the transistor operating classes and matching network design. In Section 2.3 the concept of supply modulation is introduced. Finally, Section 2.4 discusses tracking function synthesis for supply-modulated PAs.

2.1 Semiconductor Technologies

A variety of PAs with supply modulation utilizing different technologies have been reported in literature. Designs in CMOS allows for a high level of integration and more design freedom due to the availability of up to ten metal layers, which allows for more complex design structures [21]. Moreover, due to its mature Back End-of-Line (BEOL) processing it offers the possibility to add additional analog circuitry in the vicinity of the PA [22]. This makes this technology a potential contender for present-day mobile handsets [23]–[25]. Very high frequencies can be reached due to aggressive nanometer gate scaling. However, CMOS generally has a rather low available supply voltage, which makes it difficult to use for high-power applications. Furthermore, the initial cost is much higher than its III-V counterparts, but in high-volume markets, such as for mobile handsets, the cost could be significantly reduced [26].

The GaAs material employs a larger bandgap of approximately 1.4 eV compared to around 1.1 eV for the CMOS technology. A wider bandgap allows for enhanced efficiency, reliability, and power density. Its integration level is much lower as typically only two metal layers are available for the design. Better thermal dissipation is observed in comparison to the CMOS technology [26]. A moderate output power level can be achieved with good thermal stability [27].

Supply-modulated GaAs PAs are commonly used in commercial handsets due to the inherent resilience to gain and phase variations when the supply voltage is altered [19], [28], thus limited designs are published.

GaN High Electron Mobility Transistors (HEMTs) exhibit a wide bandgap of approximately 3.4 eV, making them suitable for high-power and high-efficiency applications. The high breakdown voltage of GaN HEMTs can support large voltage swings to achieve high RF output power and efficiency [10], [11], [13]. Often GaN is grown on Silicon Carbide (SiC) substrates as it can provide high thermal dissipation [29]. Recently, Silicon (Si) has been investigated as a substrate for GaN, having lower production costs at the cost of worse thermal behavior [30]. The maturity of GaN lags behind GaAs and CMOS processes [26]. Supply modulation is less common for GaN PAs since the gain and phase characteristics change significantly for a varying supply voltage [20], [31].

2.2 Power Amplifier Fundamentals

In general there are two common ways in which a transistor can be configured to amplify an RF input signal, which are the transconductance amplifier and switch-based configuration. Typically, a switch-mode amplifier can achieve higher efficiencies at the cost of increased design complexity, requiring accurate harmonic terminations and a high switching speed. These terminations can become increasingly bulky when lower frequencies are approached, e.g. the Frequency Rage 3 (FR3) band (7.125 – 24.25 GHz) for 5G and 6G communications or the K-band (18 – 27 GHz) for SATCOM applications. Furthermore, based on the termination order the design might exceed the operating frequency of the technology. An alternative is the transconductance amplifier, typically configured in a common source configuration to provide both voltage and current gain, which is depicted in Fig. 2.1. Transistor Q_1 is biased with a specified gate voltage, V_{GG}, and drain voltage, V_{DD}, which sets the quiescent drain current, I_{DD}. At both the RF input and output a dc blocking capacitor is added, which acts as an RF short circuit. Similarly, the gate and drain biases are provided through an inductor, which presents a high impedance for the RF signals, only allowing dc to flow through.

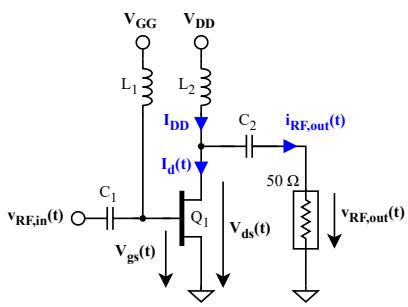


Figure 2.1: Simplified schematic of a common source transconductance amplifier.

The time-varying gate-source voltage, $V_{\mathrm{gs}}(t)$, is calculated as

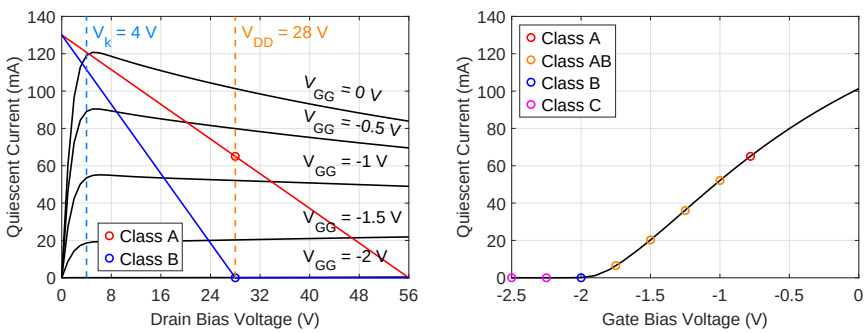
$$V_{\mathrm{gs}}(t) = V_{\mathrm{GG}} + v_{\mathrm{RF,in}}(t), \tag{2.1}$$

which is comprised of the dc gate bias and the RF input voltage, $v_{\mathrm{RF,in}}(t)$. The gate-source voltage modulates the drain current, $I_{\mathrm{d}}(t)$, which subsequently flows through dc blocking capacitor C_2 and yields an RF output current, $i_{\mathrm{RF,out}}(t)$. For a continuous wave sinusoidal input signal the real power delivered to the load, P_{out}, is computed as

$$P_{\mathrm{out}} = \frac{1}{T}\int_0^T v_{\mathrm{RF,out}}(t) \cdot i_{\mathrm{RF,out}}(t)\ \mathrm{d}t, \tag{2.2}$$

where $v_{\mathrm{RF,out}}(t)$ is the RF output voltage and T is the period of the sinusoid.

Based on the dc gate and drain bias the quiescent current of the transistor is set, which determines the operation class. Fig. 2.2 presents the simulated drain current versus the drain and gate bias voltages for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 120 nm depletion mode GaN-on-SiC HEMT technology. The maximum voltage swing is obtained for a class-A bias, which becomes evident from the class-A load line in Fig. 2.2a, having a voltage swing from the knee voltage, V_{k}, to the breakdown voltage, which is equal to two times V_{DD}. Simultaneously, the maximum current swing is achieved, thus yielding the highest linear output power. For the class-B bias a half-rectified current waveform is obtained. In class-C operation the conduction angle, θ_{c}, corresponding to the fraction when the transistor is conducting current, is further reduced.



(a) (b)

Figure 2.2: Simulation results of (a) drain current versus drain and gate bias voltage and (b) drain current versus gate bias voltage with $V_{\mathrm{DD}} = 28$ V for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 technology.

The conduction angle determines the dc power consumption, P_{dc}, which directly influences the PA drain efficiency, η, computed as

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}} = \frac{\theta_{\mathrm{c}} - \sin(\theta_{\mathrm{c}})}{4 \cdot \left(\sin\left(\frac{\theta_{\mathrm{c}}}{2}\right) - \frac{\theta_{\mathrm{c}}}{2}\cos\left(\frac{\theta_{\mathrm{c}}}{2}\right)\right)}, \tag{2.3}$$

where a reduced conduction angle yields a higher drain efficiency. However, this comes at the cost of a reduction in linearity and gain of the PA. In Table 2.1 the conduction angles and maximum attainable drain efficiencies are displayed. Different transistor classes may be utilized based on the design application [32].

	θ_c (rad)	Maximum η (%)
Class-A	2π	50%
Class-AB	$\pi < \theta_c < 2\pi$	$78.5\% < \eta < 50\%$
Class-B	π	78.5%
Class-C	$0 < \theta_c < \pi$	$100\% < \eta < 78.5\%$

Table 2.1: Maximum drain efficiency for different transistor classes.

Often the RF input power, P_{in}, is disregarded in the efficiency calculations, resulting in the Power-Added Efficiency (PAE), defined as

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{dc}}}, \tag{2.4}$$

which approaches the drain efficiency if the gain of the PA is sufficiently high.

Another important consideration when choosing the bias point is the transconductance, g_{m}, which is calculated as

$$g_{\text{m}} = \frac{\Delta I_{\text{DD}}}{\Delta V_{\text{GG}}}, \tag{2.5}$$

and shown in Fig. 2.3. It represents the change in the quiescent current with respect to the change in the gate bias voltage. At the maximum transconductance point of the bell-shaped curve the power amplification is the highest. A flat transconductance curve is desired to enhance linearity, but in reality the parasitic drain and source resistances, as well as device self-heating, will result in the bell-shaped characteristic [33].

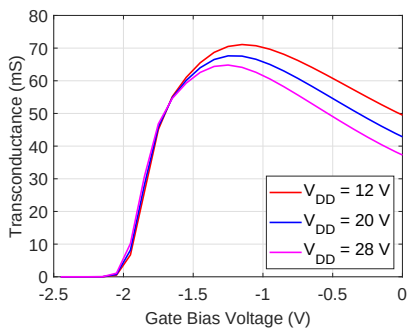


Figure 2.3: Simulation results of the transconductance versus gate and drain bias voltage for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 technology.

When the bias point has been chosen, the devices can be matched accordingly for gain, efficiency, and output power. A generic two-stage PA with matching networks is presented in Fig. 2.4. The PA is designed from the output to the input. Typically, the output stage has the largest transistor periphery compared to the driver stage to attain a higher available RF output power at the cost of decreased gain. It is not possible to infinitely increase the periphery, as heat dissipation becomes increasingly more difficult and large currents will start to flow through the ground vias. In this case it is better to combine multiple smaller devices, which in turn increases the design complexity.

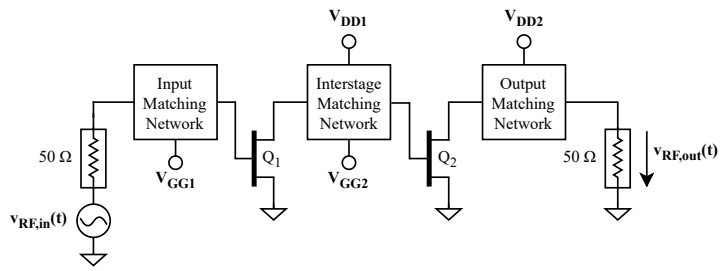


Figure 2.4: Simplified schematic of a generic two-stage PA.

Initially a load-pull analysis is performed on the output stage transistor. This empirical method revolves around presenting a multitude of load impedances to find the optimum impedance that yields either the highest output power or the maximum PAE. For higher frequencies the gain decreases and a similar optimum load impedance is found to achieve the highest output power or maximum PAE, as depicted in Fig. 2.5. It is crucial that a reliable large-signal model is available, which is often difficult due to convergence issues and increasing complexity. The interstage network usually employs a simultaneous conjugate match to boost the gain of the PA. Adding a matching network at the gate contact will directly influence the drain matching network due to parasitic coupling. Therefore, the circuit has to be carefully tuned by implementing the matching networks one by one.

Another important consideration is the stability of the PA to avoid unwanted oscillations. The magnitude of the reflection coefficients, S_{11} and S_{22}, should be below one, which alludes to unconditional stability. A common measure to evaluate unconditional stability is Rollett's stability factor [34], denoted as the K-factor, which is computed as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|}, \text{ with} \qquad \Delta = S_{11}S_{22} - S_{12}S_{21}, \tag{2.6}$$

where S_{21} is the forward transmission coefficient and S_{12} is the reverse transmission coefficient. Unconditional stability is achieved when $K > 1$ and $\Delta < 1$. The main limitation is that this stability metric only evaluates external stability of the entire PA, and therefore it is not practical for multistage PAs where

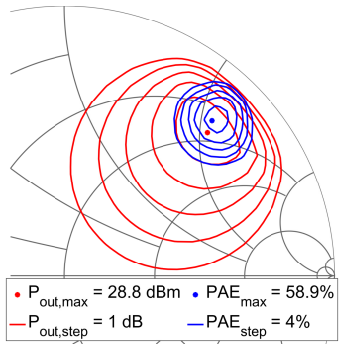


Figure 2.5: Load-pull simulation results for highest output power and maximum PAE at a frequency of 20.5 GHz for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 technology. The transistor is biased with a current density of 197 mA/mm at $V_{\mathrm{DD}} = 28$ V.

internal stability is of concern. A similar metric that evaluates external stability at the input and output of the PA is the Edwards-Sinsky stability criterion [35], known as the μ-factor, which is calculated as

$$\begin{aligned} \mu &= \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|}, \text{ and} \\ \mu' &= \frac{1-|S_{22}|^2}{|S_{11}-\Delta S_{22}^*|+|S_{12}S_{21}|}, \end{aligned} \tag{2.7}$$

which yields unconditional stability whenever either $\mu > 1$ or $\mu' > 1$. This method de-embeds the external stability to the input (μ) and output (μ') ports, respectively. More advanced methods are needed to assess internal stability, such as the Ohtomo stability criterion [36], where a multistage circuit is partitioned in smaller blocks of which the stability is individually investigated. This method can also assess large-signal stability, which is especially important for PA design [37].

The design complexity of supply-modulated PAs is higher than conventional class-AB or class-B PAs, since both the gain and phase linearity are compromised, as shown in Fig. 2.6. Effectively, this results in increased output distortion [38], [39]. The non-linear gain characteristics can be exploited to improve the amplitude linearity of the PA for a specified tracking function [40] and potential phase shifts can be mitigated with additional circuitry around the PA, such as a deliberate source and load mismatch [41]–[43] or compensating driver stage [44]. Moreover, the dc decoupling capacitance on the bias lines should be kept to a bare minimum to allow for large bandwidth signals. In turn, this may decrease the stability of the circuit, which should be resolved on-chip, usually at the transistor gates. Next to that, a varying supply voltage will introduce additional memory effects, which could push the PA into an unstable region due to self-biasing.

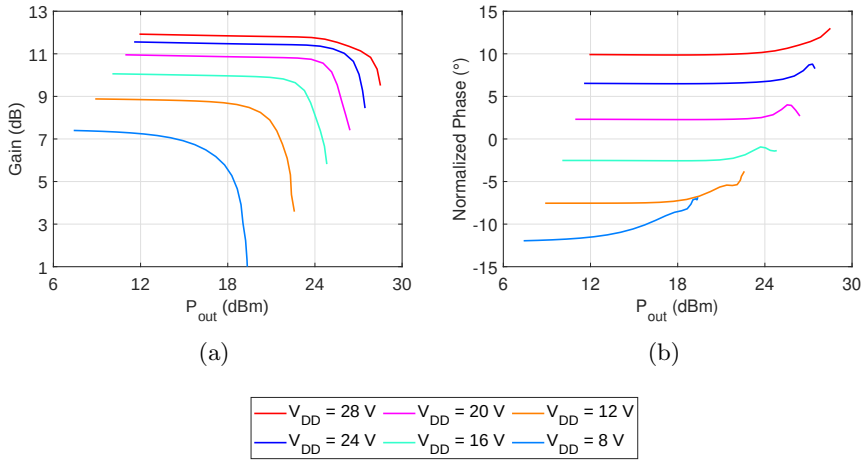


Figure 2.6: Simulation results of (a) gain versus output power and (b) normalized phase versus output power at a frequency of 20.5 GHz for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 technology. The transistor is biased with a current density of 197 mA/mm with varying drain supply voltages.

Fig. 2.7 presents the PAE curves under a variety of supply voltages for a 4×50 μm transistor using the WIN Semiconductors NP12-01 technology. Hence, for a static bias voltage of 28 V the maximum attainable PAE is 58.9%, which decreases to less than half when operated at a back-off level of 6 dB. With supply modulation it is possible to improve the back-off efficiency by dynamically varying the supply voltage based on the output power level.

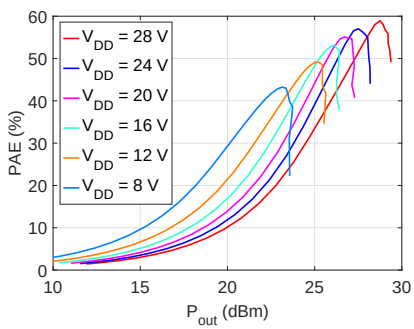


Figure 2.7: Simulation results of PAE versus output power at a frequency of 20.5 GHz for a 4×50 μm transistor utilizing the WIN Semiconductors NP12-01 technology. The transistor is biased with a current density of 197 mA/mm with varying drain supply voltages.

2.3 Introduction to Supply Modulation

For conventional class-AB or class-B operation of a PA it is generally difficult to maintain high efficiency in back-off for real-time communication signals with a high output PAPR. One effective method to overcome these limitations is supply modulation, often implemented in the form of ET [18]. ET was originally introduced by Saleh and Cox in 1983 [16] and revolves around dynamically varying the supply voltage based on the envelope of the instantaneous input signal. In turn, this yields more versatility and shifts the design complexity from the PA to the linear tracker. With gate or drain modulation it is possible to enhance the linearity or back-off efficiency of the PA [17], [45].

Fig. 2.8 depicts a simplified schematic of an ET PA, where the directional coupler feeds the RF input signal into the envelope detector to obtain the instantaneous envelope. Subsequently, the envelope is shaped according to a specified tracking trajectory, which the supply modulator then dynamically feeds to the PA, denoted by the modulation voltage, V_{mod}. This can be implemented in the form of gate modulation or drain modulation, each having its own benefits and drawbacks [46], [47]. Gate modulation is often used for PA linearization, which can slightly improve efficiency. This method is advantageous in terms of available bandwidth and decreased voltage swing [27], [48]. The slew rate, denoted by the rate of change at which the output voltage is able to change over time, is typically not a limiting factor for gate modulators, since the voltage swing is significantly smaller compared to drain modulators. With drain modulation the highest efficiency improvement is achieved by always keeping the PA near its saturation region, controlling the current flow more effectively. However, linearity tends to worsen significantly due to gain and phase variations that introduce distortion in the RF output signal [38], [39]. Furthermore, the design of a high-speed drain modulator is often challenging, since a large voltage swing is required, which can lead to slew-rate limitations. By combining both techniques simultaneously, back-off efficiency can be improved with drain modulation and non-linearities can be resolved with gate modulation [49], [50].

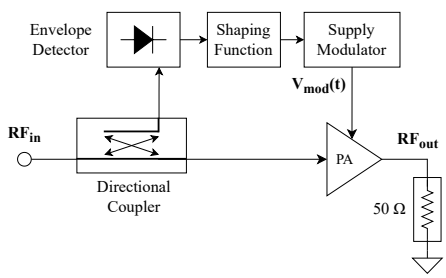


Figure 2.8: Simplified schematic of an ET PA.

To graphically illustrate the benefit of e.g. drain modulation, a comparison of the voltage overhead for a static bias and a dynamic drain-modulated ET bias is shown in Fig. 2.9. For a static bias it can be seen that the voltage

overhead increases significantly for lower output power levels, which decreases the back-off efficiency and generates unnecessary heat. Moreover, if the static supply were to be lowered to obtain better back-off efficiency, the peak output power cannot be achieved. Looking at the dynamic drain-modulated ET bias it is notable that the voltage overhead is kept to a bare minimum, thus limiting the power dissipation of the PA and improving the efficiency, especially in back-off.

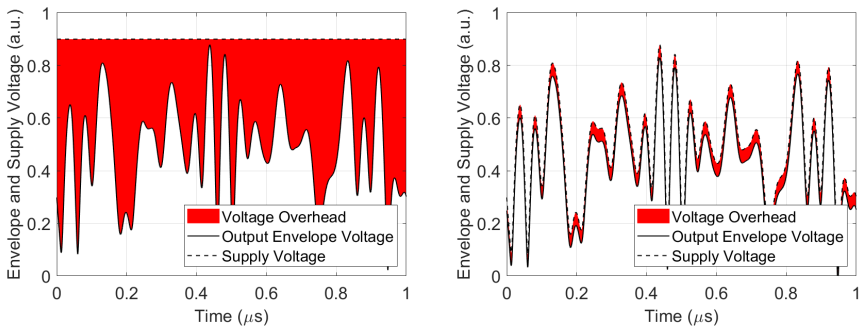


Figure 2.9: Voltage overhead for (a) a statically biased PA and (b) a drain-modulated ET PA.

However, the ET PA architecture introduces additional design complexity imposed by the supply modulator. It is important to consider the tracking accuracy, tracker efficiency, and slew-rate limitations for wideband supply modulation. Continuous supply modulators have the benefit to provide accurate tracking with limited envelope distortion, although these tend to be highly inefficient with limited available bandwidth [51]. Moreover, fast-switching and high slew-rate op-amps with sufficient voltage swing are required to make this work. Continuous supply modulators are effective tools for laboratory use, having the freedom to provide any desired output voltage. However, in a real communication system this implementation would decrease the overall efficiency of the system drastically, since the compound efficiency of the complete system, η_{syst}, is computed as

$$\eta_{\text{syst}} = \eta_{\text{SM}} \cdot \eta_{\text{PA}}, \tag{2.8}$$

where η_{SM} is the supply modulator efficiency and η_{PA} is the PA drain efficiency. Therefore, discrete supply modulation is mostly used in practice. In literature wide-bandwidth discrete supply modulators with >90% efficiency for high output power GaN PAs have been reported [52]–[54], being able to enhance the PA back-off efficiency by a factor of two [55]. This method can generally provide two to four different voltage levels, which would introduce unwanted envelope distortion due to fast switching transients.

Previously it was mentioned that the main challenges for supply-modulated PAs are the supply modulator design and interconnect, as well as the tracking function synthesis. The main design difficulties for active load-modulated

PAs, such as the Doherty PA, outphasing PA, or LMBA, are the design of the input and output combiner networks, frequency scaling, and back-off power level improvement. The combiner networks tend to get bulky at lower frequencies, since quarter-wavelength ($\lambda/4$) transmission lines are employed. Moreover, these combiner networks are often complemented with a Wilkinson splitter, which is typically tuned for a single center frequency. When deviating from the center frequency the port isolation of the splitter degrades, which limits the available fractional bandwidth. Next to that, the peak and back-off efficiency reduce when the PA is designed for increasingly higher output PAPR communication signals. Thus, it has been a constant research topic to try to overcome these limitations [56], [57].

2.4 Tracking Function Design

The shaping function block highlighted in Fig. 2.8 is defined by a specific tracking function. Here, the signal envelope is shaped to provide a desired supply voltage trajectory. Commonly known trajectories are maximum PAE tracking to obtain the highest efficiency or flat gain tracking to improve linearity. To synthesize a tracking function, the PA drain voltage, V_d, is mapped to its respective instantaneous RF input power level, P_in. This mapping can be computed from CW measurements of the PA under different static drain voltages. Another more advanced method involves prepulsing, where the PA is kept in a controlled trapping state to also include memory effects [58]. A trade-off has to be made between tracking accuracy and tracker efficiency, since fast-switching envelope signals degrade the efficiency of the linear tracker. Several works have investigated highly accurate ET without tracking signal bandwidth, B_track, minimization [59], [60]. Other works focus on limiting the slew-rate, and thus B_track, at the cost of tracking accuracy and increased envelope distortion [40], [61]–[63].

Mathematically speaking, the envelope, V_e, of an RF signal is computed as

$$V_\mathrm{e} = \sqrt{V_\mathrm{I}^2 + V_\mathrm{Q}^2}, \tag{2.9}$$

where V_I is the RF voltage of the in-phase component and V_Q is the RF voltage of the quadrature component. Due to the presence of the square root term in (2.9) for pure ET, B_track becomes infinite. This can be further explained by looking at the infinite Taylor series expansion of the square root term centered at 1, which is defined as

$$\sqrt{x} = 1 + \sum_{n=1}^{\infty} \frac{(-1)^{n-1}\,(x-1)^n\,(2n-2)!}{2^{2n-1}\,(n-1)!\;n!} \qquad \text{for } 0 \leq x \leq 2, \tag{2.10}$$

and can therefore be approximated as

$$\sqrt{x} \approx a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 + \cdots, \tag{2.11}$$

where a_0 – a_∞ are real-valued decimal numbers. Hence, the signal bandwidth is increased by a factor n when a signal is raised to the power of n. Consequently,

the square root approximation in (2.11) has infinite terms, thus yielding an infinite bandwidth expansion. However, in practice the higher order terms of (2.11) are generally sufficiently small to be neglected to create a truncated band-limited signal.

To overcome the slew-rate limitations of pure ET it is possible to use Power Tracking (PT) to create a band-limited even-order approximation of the Taylor series expansion, which in turn limits the tracking bandwidth to an integer multiple of the PT order [64], [65]. Solely even-order terms of the Taylor series expansion are used to obtain a $V_{\mathrm{d}}(P_{\mathrm{in}})$ trajectory that is proportional to the power of the input signal. For example, the first-order PT trajectory, V_{PT}, is written as

$$V_{\mathrm{PT}} = \alpha_0 + \alpha_2 \cdot V_{\mathrm{e}}^2, \tag{2.12}$$

where α_0 and α_2 are tracking coefficients. By exploiting PT the square root term in (2.9) is eliminated, thus limiting B_{track} to only the RF signal bandwidth, B_{RF}. As mentioned before, this method comes at the cost of reduced tracking accuracy compared to pure ET. Increasing the PT order to e.g. second-order PT (PT2) or reduced PT2 (PT2R) would result in more accurate tracking at the cost of increased envelope bandwidth expansion. The PT2 trajectory, V_{PT2}, is defined as

$$V_{\mathrm{PT2}} = \alpha_0 + \alpha_2 \cdot V_{\mathrm{e}}^2 + \alpha_4 \cdot V_{\mathrm{e}}^4, \tag{2.13}$$

where α_4 is an additional tracking coefficient. The higher-order terms extend B_{track} to two times B_{RF}. Similarly, the PT2R tracking function is given by

$$V_{\mathrm{PT2R}} = \alpha_0 + \alpha_4 \cdot V_{\mathrm{e}}^4, \tag{2.14}$$

expanding B_{track} to two times B_{RF}, which is identical to PT2.

The Power Spectral Density (PSD) for all aforementioned trajectories is presented in Fig. 2.10. This illustration clearly shows a reduction in the sidelobe level for the PT trajectory for frequencies larger than B_{RF} and similarly a reduction for the PT2 and PT2R trajectories for frequencies beyond $2 \cdot B_{\mathrm{RF}}$. The sidelobe level for pure ET has a less steep frequency roll-off due to the infinite terms in the Taylor series expansion for the square root function.

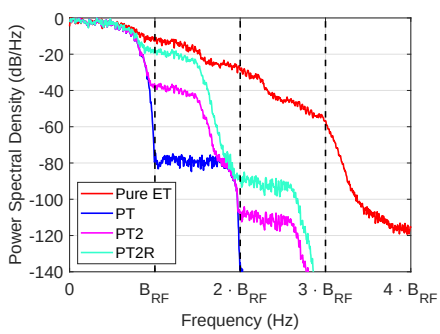


Figure 2.10: Normalized PSD for pure ET, PT, PT2, and PT2R, showing envelope bandwidth expansion.

Chapter 3

Supply Modulator Topologies

This chapter dives into supply modulator design considerations, as well as continuous and discrete supply modulator architectures. Section 3.1 discusses the most relevant design parameters in supply modulator design. Section 3.2 presents the linear regulator continuous supply modulator topology, which is typically based on linear op-amps. In Section 3.3 the switch-mode buck converter continuous supply modulator architecture is shown, employing fast-switching transistors. Section 3.4 discusses the hybrid continuous supply modulator design, combining the linear and buck converter topologies. Section 3.5 presents multi-level discrete supply modulator designs, where fast-switching transistors provide a limited number of supply voltages. Lastly, Section 3.6 provides a comparison of the aforementioned topologies.

3.1 Design Considerations

Supply modulator design requires careful consideration of a variety of properties. First of all, the efficiency of the supply modulator will directly influence the efficiency of the complete ET PA system, as shown in (2.8). The compound efficiency of the system is computed by multiplying the individual supply modulator and PA efficiencies, respectively.

Secondly, the supply modulator should demonstrate high speed to be able to handle fast envelope signals. The slew-rate determines the maximum rate of change of the op-amp or switching transistor output voltage, and the bandwidth directly influences how wideband RF input signals can be handled. As discussed in Section 2.4, envelope bandwidth reduction techniques can alleviate the supply modulator bandwidth requirement at the cost of tracking accuracy.

Thirdly, PA linearity implications are an important aspect in supply modulator design, which can be enforced by having a low output ripple. Assume an input RF signal, X_{in} defined as

$$X_{\text{in}} = V_{\text{in}} \cos\left(2\pi f_{\text{c}} t\right), \tag{3.1}$$

is being mixed together with a supply modulator ripple, X_{ripple}, of

$$X_{\text{ripple}} = V_{\text{ripple}} \cos\left(2\pi f_{\text{ripple}} t\right), \tag{3.2}$$

where V_{in} and V_{ripple} are the input voltage and ripple amplitudes, f_{c} and f_{ripple} are the RF carrier frequency and ripple frequency, and t is the time vector. Now, the output sideband amplitude, V_{out}, of the supply ripple is computed as

$$V_{\text{out}} = \sum_{i,j=0}^{\infty} a_{i,j} V_{\text{in}}^{i} V_{\text{ripple}}^{j}, \tag{3.3}$$

where $a_{i,j}$ are the intermodulation coefficients of the i-th order of the input voltage and the j-th order of the ripple amplitude. Hence, from (3.3) it can immediately be seen that additional unwanted intermodulation products occur, being directly influenced by the supply modulator ripple amplitude [22].

Finally, the supply modulator should ideally have a near-zero output impedance. The influence of a non-zero impedance on the drain of a PA has been evaluated with an envelope simulation testbench in the Keysight ADS software, using the schematic shown in Fig. 3.1. A modulated input signal is split into two paths, which are the envelope and RF path, respectively. In the envelope path the complex time-varying waveform is demodulated and the In-Phase (I) and Quadrature (Q) components are retrieved. The output current of the first Voltage-Controlled Current Source (VCCS), $I_1(t)$, is then computed as

$$I_1(t) = \frac{V_{\text{I}}^2(t) + V_{\text{Q}}^2(t)}{50}, \tag{3.4}$$

which is similar to the envelope calculation of (2.9) in Section 2.4. Subsequently, this current flows through resistor R_2 and yields a detected envelope voltage, $V_{\text{det}}(t)$. This voltage is converted to a detected power level, $P_{\text{det}}(t)$, as

$$P_{\text{det}}(t) = 10 \cdot \log_{10}\left(\frac{|V_{\text{det}}(t)|}{100}\right) + 30, \tag{3.5}$$

which will be compared to a pre-determined shaping table acquired from static simulations. The shaping table contains the desired drain voltage, $V_{\text{d,track}}$, for a desired input power level, $P_{\text{in,track}}$, for e.g. a flat gain or maximum PAE trajectory. Afterwards, the current of the second VCCS, $I_2(t)$, is calculated from the shaping table output drain voltage and an offset voltage, $V_{\text{d,offset}}$, as

$$I_2(t) = \frac{\Delta V_{\text{d}}(t)}{50} = \frac{V_{\text{d,track}}(t) - V_{\text{d,offset}}}{50}. \tag{3.6}$$

It should be noted that $V_{\text{d,offset}}$ is a static voltage, which is determined by the lower bound of the desired supply modulation voltage range. At the output of the second VCCS a time-varying drain voltage, $V_{\text{d}}(t)$, is obtained. To keep the drain impedance equal to zero, a Voltage-Controlled Voltage Source (VCVS) is used as a buffer between the drain modulator and the PA. To ensure that the correct supply voltage operating region is used, the time-varying drain voltage

is being superimposed with the static offset voltage at the VCVS output node. Through variable resistor R_{d} the output impedance of the drain modulator can be varied to evaluate the envelope distortion. The RF path only consists of a single VCVS with a voltage gain, G_{V}, of two to ensure that the correct input power level is presented to the PA.

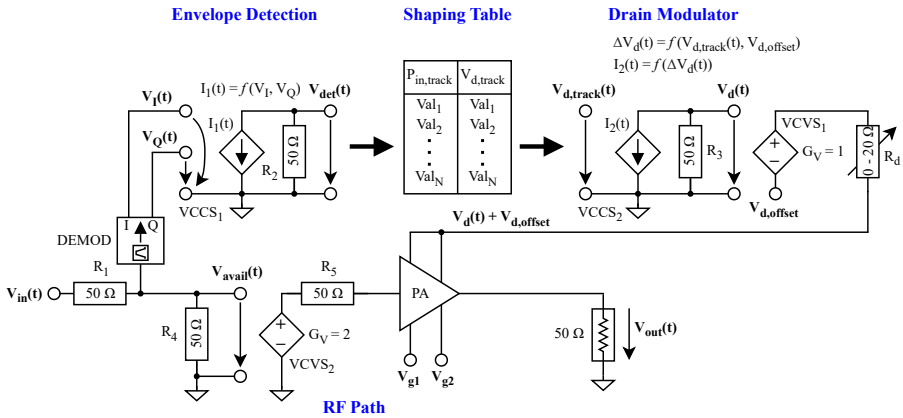


Figure 3.1: Schematic of envelope simulation testbench for a supply-modulated two-stage PA, highlighting the envelope signal path consisting of an envelope detector, shaping table, and drain modulator, as well as the RF signal path.

Simulations were performed on a supply-modulated two-stage driver amplifier operating at 20.5 GHz, which has a small-signal gain of 21.0 dB and a bandwidth spanning from 17.9 GHz up to 24.5 GHz, as discussed in detail in Section 6.2. A significant increase of the Root Mean Square (RMS) Error Vector Magnitude (EVM) for a higher supply modulator output impedance is observed, as presented in Fig. 3.2. This is mainly due to an additional voltage drop introduced at the supply node due to resistor R_{d}.

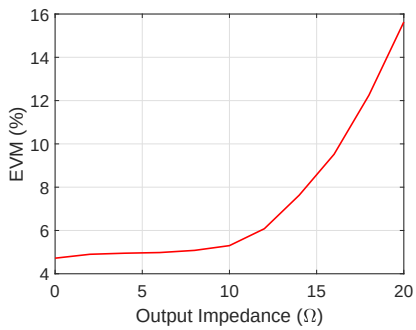


Figure 3.2: Simulated RMS EVM versus supply modulator output impedance for a supply-modulated two-stage PA operating at 20.5 GHz.

3.2 Linear Regulators

One possible topology for continuous supply modulation is the linear tracker, as shown in Fig. 3.3. This architecture typically consists of two linear amplifying stages, where the driver stage is a high-speed gain stage and the output stage is a low-speed power stage. In the non-inverting configuration the output impedance is inversely related to the open-loop gain and the feedback factor, where a larger feedback factor, defined by negative feedback resistor R_{fb2} and grounded resistor R_{s2}, yields a decreased output impedance. Therefore, the driver stage is designed for high gain such that the output stage gain can be lowered to reduce the output impedance of the tracker, which decreases the envelope distortion of the PA. The main difficulties arise from the lack of commercially available high-speed op-amps with significant current handling and large rail-to-rail supply voltages. Current feedback op-amps are most suitable, since the feedback resistor can be sized accordingly as a trade-off between high bandwidth or improved stability [66]. Linear trackers tend to be highly inefficient and thus also require careful thermal design. Therefore, the main application is for laboratory testing of supply-modulated systems. There seems to be a research gap regarding linear regulators, so only two published designs were chosen to be discussed in detail.

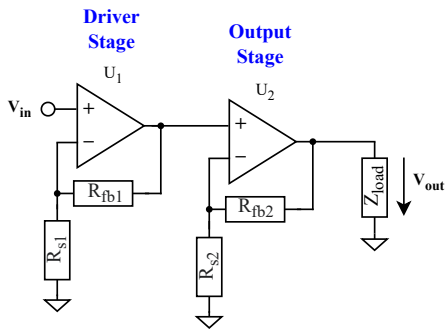


Figure 3.3: Simplified schematic of a linear tracker, highlighting the driver stage for gain and output stage for power handling.

The laboratory-grade continuous linear tracker published in [67] is presented in Fig. 3.4. This design revolves around the parallel configuration of 48 Texas Instruments LM7372 voltage feedback op-amps, having a gain-bandwidth product of 120 MHz, high slew-rate of 3000 V/μs, maximum supply voltage of 36 V, and an output current of 150 mA. The combined output yields a large voltage swing of 3 – 32 V with a maximum output current of 7 A. A bandwidth of 70 MHz is obtained by applying gain peaking of 8 dB, which results in an expanding gain characteristic. Afterwards, this is equalized to ensure a smooth flat response over frequency. The output combining network should be carefully designed to minimize the parasitic inductance, which in turn improves the available bandwidth. The driver consists of three voltage gain stages such that the output stage gain can be lowered to reduce the output impedance.

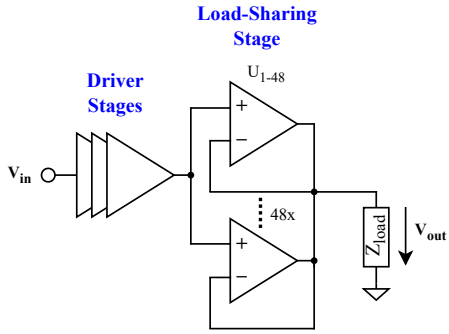


Figure 3.4: Simplified schematic of the laboratory-grade continuous linear regulator published in [67], highlighting the driver stages for gain and a load-sharing parallel op-amp configuration as output stage.

Another laboratory-grade continuous linear tracker published in [51] is depicted in Fig. 3.5. This supply modulator supports a high output current drive of 2 A and a large voltage swing of 6 – 28 V, together with a distortion-free tracking bandwidth of 18 MHz. The driver stage employs high-speed Texas Instruments THS3202 current feedback op-amps with a unity-gain bandwidth of 2 GHz, high slew-rate of 9000 V/μs, and a maximum supply voltage of 15 V in an instrumentation amplifier configuration. This configuration yields a differential to single-ended conversion while simultaneously boosting the gain of the tracker. The output stage uses two Analog Devices ADA4870 current feedback op-amps, having a bandwidth of 52 MHz, slew-rate of 2500 V/μs, a maximum supply voltage of 40 V, and a high output current drive of 1 A. Having two of these devices in parallel ensures that sufficient current can be supplied to the PA without distortion. Unfortunately, these op-amps are nowadays obsolete, but a potential alternative is presented in Section 4.2. Resistors R_{18} and R_{19} are added to counteract a slight gain mismatch between op-amps U_3 and U_4, as well as for stability purposes when a capacitive load is present. Lastly, the gain of the load-sharing output stage is deliberately kept low, which reduces the output impedance of the supply modulator.

3.3 Buck Converters

Another potential topology for a continuous supply modulator is the asynchronous buck converter [68], as presented in Fig. 3.6. This architecture is also widely known as a step-down DC-DC converter, where the output voltage will be equal to or lower than the static supply voltage, V_{DD}. Simultaneously, it can deliver high currents to the load with an increased efficiency compared to the linear regulator. Typically, this comes at the cost of higher design complexity.

Operation of the asynchronous buck converter revolves around transistor Q_1 acting as a controllable switch with a Pulse-Width Modulated (PWM) gate control signal, V_{hs}. When transistor Q_1 is turned on, diode D_1 gets an inverse

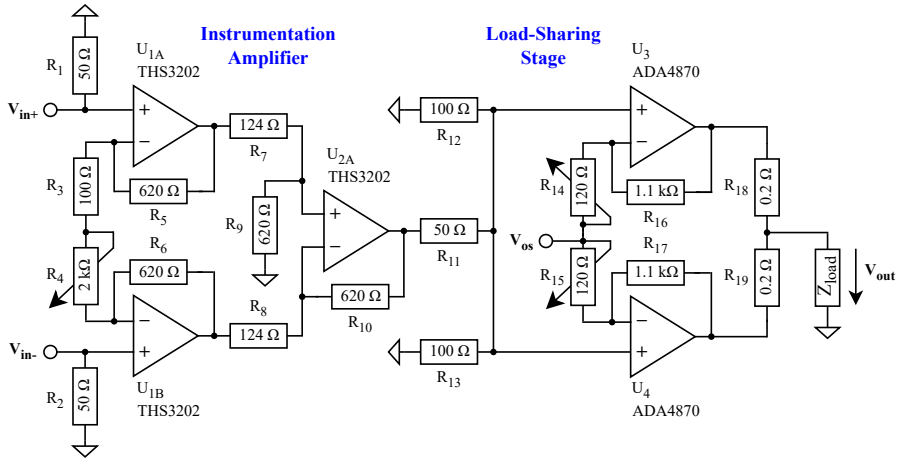


Figure 3.5: Simplified schematic of the laboratory-grade continuous linear regulator published in [51], highlighting the instrumentation amplifier as driver stage and load-sharing parallel op-amp configuration as output stage.

polarization from V_{DD}, effectively turning off the diode. This ensures that inductor L_1 will have a voltage potential of $V_{\mathrm{DD}} - V_{\mathrm{out}}$, which then provides a positive linear slope for the inductor current. Similarly, when transistor Q_1 is turned off, diode D_1 is reverse-biased and turns on shortly after, taking over the stored current of inductor L_1. Now, inductor L_1 will have a voltage potential of $-V_{\mathrm{out}}$ and supply a negative linear slope for the inductor current due to discharging. Based on the duty cycle, d, of the PWM gate control signal the average output voltage can be regulated accordingly. Capacitor C_1 is added to prevent unwanted voltage spikes due to fast on/off-switching of transistor Q_1.

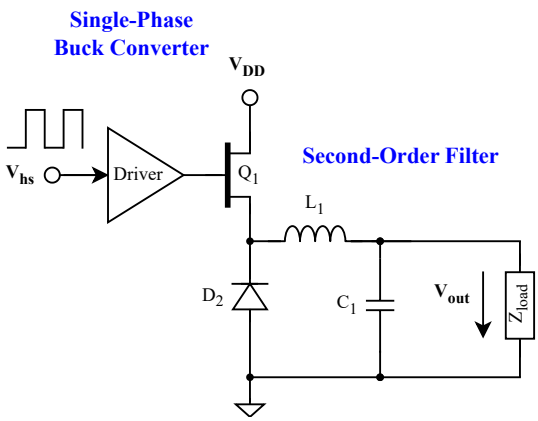


Figure 3.6: Simplified schematic of an asynchronous single-phase buck converter, highlighting the switching transistor with PWM input signals and second-order output filter.

The synchronous buck converter shown in Fig. 3.7 is a modified version of the asynchronous buck converter, replacing diode D_1 with another transistor Q_2. Circuit operation is similar to the asynchronous buck converter, now considering both transistor Q_1 and Q_2 acting as controllable switches with complementary PWM gate control signals, V_{hs} and V_{ls}. Typically, a higher efficiency can be achieved with a synchronous buck converter, while the cost and complexity increases. Specifically, for the asynchronous buck converter a power loss is introduced by the voltage drop over diode D_1, decreasing efficiency. By choosing a switching transistor Q_2 with sufficiently small drain-source on-resistance, $R_{\text{ds,on}}$, this power loss can be decreased, which in turn improves efficiency. However, complexity increases vastly due to the need of an additional complementary gate driver circuit. Furthermore, to prevent unwanted transient current spikes in the output load due to fast on- and off-switching, it is important to have a certain amount of dead time in between the switching operations, turning both transistors off.

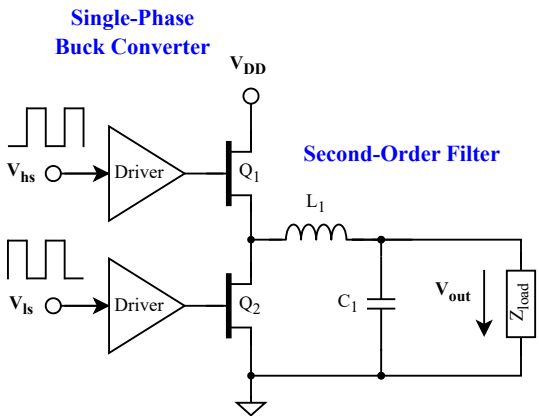


Figure 3.7: Simplified schematic of a synchronous single-phase buck converter, highlighting the switching transistors with PWM input signals and second-order output filter.

In practice, the efficiency of buck converters are severely influenced by the PWM duty cycle, where a smaller duty cycle introduces additional losses in diode D_1 or transistor Q_2 [69], [70]. Moreover, the switching frequency of the transistors has to be significantly higher than the RF modulation bandwidth to ensure that the spurious frequency components are filtered out by the LC-network [71], [72]. If pure ET is used, the transistor switching frequency should generally be ten times as large as the modulation bandwidth. With the envelope bandwidth reduction techniques presented in Section 2.4 this switching frequency requirement can be lowered. Packaged commercial high-power switching transistors often tend to have a smaller available switching speed, making this topology tricky to implement for wideband modulated signals. However, recent work shows a single-phase buck converter Monolithic Microwave Integrated Circuit (MMIC) handling RF modulation bandwidths

up to 80 MHz implemented in a 150 nm GaN HEMT process [45].

Moreover, multi-phase synchronous buck converters with higher-order output filters have been presented in [70], [73], [74], which could reach a modulation bandwidth of up to 20 MHz using commercially available switching transistors. This topology is depicted in Fig. 3.8, where N synchronous buck converter cells are used in parallel, together with a fourth-order output filter to ensure zero-voltage switching. For the multi-phase architecture the waveforms of each cell are interleaved, which reduces the power dissipation in the switching transistors by a factor of N. Next to that, the switching losses are reduced, which improves the overall efficiency [75]. The zero-voltage switching output filter is crucial to ensure inherent current phase balance in this design. A higher-order filter design can achieve sharper frequency selection, while simultaneously increasing the load sensitivity [73]. All in all, it can be seen that the efficiency can be further improved at the cost of growing complexity.

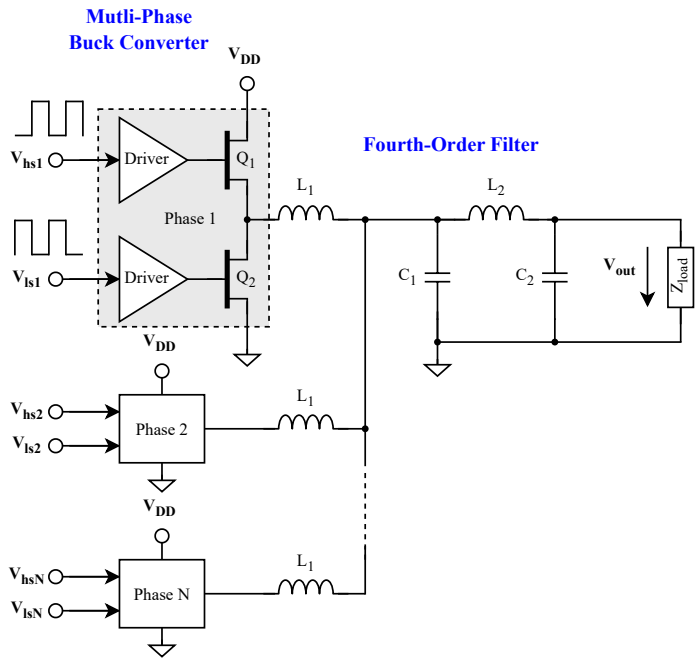


Figure 3.8: Simplified schematic of the N-phase synchronous buck converter published in [70], highlighting the N buck converter cells with PWM input signals and fourth-order output filter for zero-voltage switching.

3.4 Hybrid Implementations

A combination of the linear tracker of Section 3.2 together with the switch-mode synchronous buck converter of Section 3.3 results in a hybrid implementation [76], presented in Fig. 3.9. This continuous supply modulator topology employs

a linear amplifier as a high-speed low-efficiency voltage source and a composite switching amplifier as a low-speed high-efficiency current source. Specifically, the linear amplifier can reach an efficiency up to 50% in class-A bias, while the buck converter can reach efficiencies exceeding 90%.

In this topology, the linear amplifier is always on and the switch-mode buck converter is controlled by the output of the comparator. At the output of the linear amplifier the voltage drop over resistor R_{sense} is computed, which defines the polarity of the sensing current. In turn, this determines whether transistors Q_1 and Q_2 are turned on or off effectively. Moreover, the linear amplifier has to act as an active filter to reduce the output voltage ripple generated by the switching stage [77].

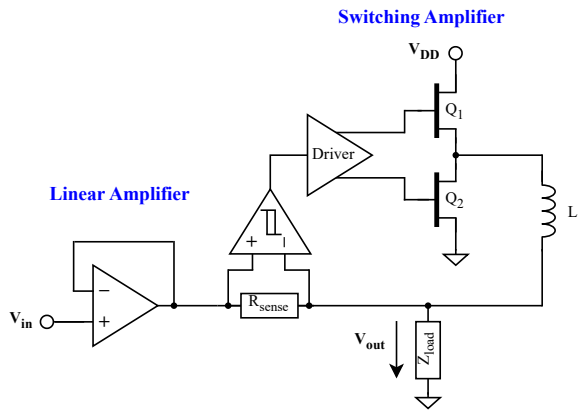


Figure 3.9: Simplified schematic of a hybrid supply modulator, highlighting the linear amplifier as a high-speed low-efficiency voltage source and switching amplifier as a low-speed high-efficiency current source.

This architecture solves the bandwidth limitation imposed by having solely a switch-mode buck converter as supply modulator. Simultaneously, it solves the efficiency issues imposed by the linear regulator. However, all of this comes at the cost of greatly increased design complexity and cost. On top of that, the interface between the linear and switching amplifier should be carefully designed to avoid any unwanted stability issues [78]. This topology is most commonly employed in CMOS technology due to the higher possible level of integration [79]–[82].

3.5 Multi-Level Discrete Supply Modulators

Discrete supply modulators can often reach higher efficiency and bandwidth compared to continuous supply modulators at the cost of having only a few available voltage levels. Class-G supply modulation is a commonly used architecture for discrete supply modulators [53], [55], [83], [84]. The core element of this architecture is a fast transistor acting as a switch to regulate

between different voltage levels. It employs a similar architecture compared to the buck modulator of Section 3.3 with the output LC-filter omitted.

A three-level discrete class-G supply modulator is depicted in Fig. 3.10, which can provide three distinct voltage levels, V_{DD1} – V_{DD3}, to the load [85]. The supply voltages are set as $V_{\mathrm{DD3}} > V_{\mathrm{DD2}} > V_{\mathrm{DD1}}$ to ensure correct operation. When transistor Q_1 is turned on and transistor Q_2 is turned off, diode D_2 is reverse-biased and thus V_{DD3} is applied to the load. Similarly, when transistor Q_1 is turned off and transistor Q_2 is turned on, diode D_2 is again reverse-biased to ensure that V_{DD2} is flowing into the load. When both transistors Q_1 and Q_2 are turned off, diode D_2 is forward-biased, thus supplying V_{DD3} to the load. Hence, the diodes D_1 and D_2 are necessary to block reverse drain-source voltages, since the transistors do not inherently have this capability. Significantly higher bandwidths up to a few hundreds of MHz can be achieved with this supply modulation method [86], [87], while maintaining efficiencies >90%. However, fidelity will degrade very rapidly with discrete supply modulation due to the limited available voltage levels. Other more advanced four-level switch-based discrete supply modulators employ multiple switches with self-biasing capabilities [88], a high-power 800 W multi-level converter [89], or a flying capacitor multi-level architecture [90]. An eight-level discrete supply modulator based on a 3-bit power-Digital-to-Analog Converter (DAC) is illustrated in [91].

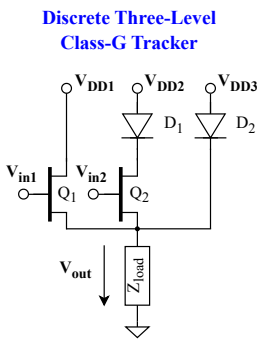


Figure 3.10: Simplified schematic of the three-level discrete class-G supply modulator published in [85].

3.6 Comparison of Topologies

Table 3.1 presents a summary of each implementation in terms of the design considerations mentioned in Section 3.1.

Bandwidth	
Linear Regulators	*High*; The bandwidth of a current feedback op-amp is dependent on the negative feedback resistor, where a lower value results in a higher bandwidth.
Buck Converters	*Low – Moderate*; Typically, the transistor switching speed has to be at least ten times faster than the envelope. This limitation can be mitigated with envelope bandwidth reduction techniques discussed in [40], [61]–[63]. Also, a higher order for the output *LC*-filter yields a sharper frequency selection.
Hybrid Implementations	*High*; The linear amplifier acts as a high-speed low-efficiency voltage source and the switching amplifier acts as a low-speed high-efficiency current source.
Discrete Supply Modulators	*High*; Switching is only performed between a limited amount of voltage levels, which allows for faster ET.
Efficiency	
Linear Regulators	*Low*; A linear amplifier is always on and thus has a maximum efficiency of 50% or lower.
Buck Converters	*High*; A switch-mode amplifier minimizes power loss by switching on and off, where the PWM duty cycle directly influences the efficiency.
Hybrid Implementations	*Moderate – High*; The switching amplifier delivers most of the power with high efficiency and the linear amplifier tracks the fast envelope in a linear fashion.
Discrete Supply Modulators	*High*; Transistors operate as switches between fixed voltage levels to minimize power dissipation.
Output Ripple	
Linear Regulators	*Low*; Linear amplification results in low output ripple.
Buck Converters	*Moderate – High*; Due to the switch-mode operation an output ripple is introduced, which can be minimized by carefully designing the output *LC*-filter.
Hybrid Implementations	*Moderate – High*; The switching amplifier introduces a ripple and the linear amplifier acts as an active filter to reduce this ripple.
Discrete Supply Modulators	*High*; Fast transistor switching results in an increased voltage ripple.

Output Impedance	
Linear Regulators	*Low*; The closed-loop output impedance has an inverse relationship to the open-loop gain and feedback factor, where a larger feedback factor will reduce the output impedance in a non-inverting configuration.
Buck Converters	*Low – Moderate*; Parasitics of the switching devices and *LC*-filter yield a non-zero output impedance, which is highly dependent on frequency.
Hybrid Implementations	*Low*; The near-zero output impedance of the linear amplifier dominates the overall output impedance, as it is in parallel with the switching amplifier output impedance.
Discrete Supply Modulators	*Low – Moderate*; Each voltage rail presents a different output impedance as device parasitics vary, especially at high output power levels.

Table 3.1: Comparison of supply modulator topologies.

Chapter 4

Laboratory-Grade Drain Modulator Design

This chapter presents two reconfigurable laboratory-grade continuous linear tracker designs employing high-speed current feedback op-amps. The designs support both GaN and GaAs devices with voltage swings between 10 – 20 V and 0 – 4 V, respectively. CW measurement results are shown to evaluate bandwidth, peaking behavior, and tracker output impedance. Section 4.1 discusses theory regarding the current feedback op-amp. Section 4.2 shows the first laboratory-grade continuous drain modulator with a push-pull output stage. Thereafter, Section 4.3 presents the second laboratory-grade continuous drain modulator with a load-sharing output stage.

4.1 Current Feedback Operational Amplifier

Current feedback op-amps are great contenders to be used for high-speed circuits such as the linear regulator design, generally exhibiting high unity-gain bandwidth, high slew-rates and low output impedance [92]. Fig. 4.1 depicts the model for a current feedback op-amp in non-inverting configuration with an external feedback network. The non-inverting input is connected to the inverting input through a unity gain buffer, which ensures that the non-inverting input has a high impedance and the inverting input has a low impedance. Due to the low impedance in the inverting path, the feedback network operates as a current source. The error current, i_{e}, is computed as the difference of the currents flowing at the inverting input, namely

$$i_{\mathrm{e}} = i_{\mathrm{s}} - i_{\mathrm{fb}}, \tag{4.1}$$

where i_{s} is the current through the grounded resistor, R_{s}, and i_{fb} is the current through the feedback resistor, R_{fb}. Subsequently, the error current is fed into the internal high-impedance stage, resulting in an output voltage, V_{out}, of

$$V_{\mathrm{out}} = i_{\mathrm{e}} \cdot Z_{\mathrm{T}}(f), \tag{4.2}$$

where $Z_{\mathrm{T}}(f)$ is the frequency-dependent transimpedance. Moreover, the transfer function of this idealized current feedback op-amp model is given by

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \left(1 + \frac{R_{\mathrm{fb}}}{R_{\mathrm{s}}}\right) \cdot \frac{1}{1 + \frac{R_{\mathrm{fb}}}{Z_{\mathrm{T}}(f)}} \approx 1 + \frac{R_{\mathrm{fb}}}{R_{\mathrm{s}}}. \tag{4.3}$$

The approximation in (4.3) comes from the assumption that the frequency-dependent transimpedance term is dominating, which is typically in the order of a few MΩ.

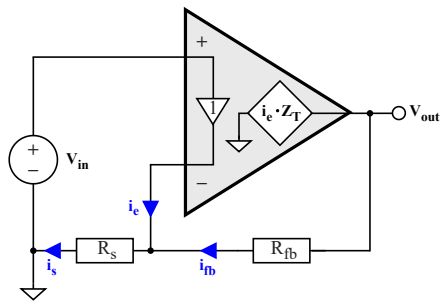


Figure 4.1: Ideal non-inverting current feedback op-amp model.

Loop gain analysis is a critical part of current feedback op-amps, as it defines the bandwidth and stability characteristics of the amplifier. The loop gain, G_{loop}, is defined as

$$G_{\mathrm{loop}} = A_{\mathrm{ol}} \cdot \beta = \frac{Z_{\mathrm{T}}(f)}{R_{\mathrm{fb}}}, \tag{4.4}$$

where A_{ol} is the open-loop gain and β is the feedback factor of the circuit. The point where the magnitude of the loop gain, $|G_{\mathrm{loop}}|$, equals one defines the bandwidth of the op-amps. Hence, the bandwidth is directly dependent on the feedback resistor value and not the gain setting. Therefore, a smaller feedback resistor yields a larger available bandwidth. However, setting this too small will result in unwanted oscillations, which can be investigated with an open-loop analysis. Often, recommended values for the feedback and grounded resistors are given in the datasheet of the component.

4.2 Push-Pull Drain Modulator Design

The first continuous linear regulator design is presented in Fig. 4.2, as published in [Paper B]. This design employs three Texas Instruments THS3491DDA high-speed current feedback op-amps distributed over two driver stages to boost the voltage gain, followed by two push-pull output stages with complementary Bipolar Junction Transistor (BJT) pairings to handle large load currents. This op-amp is favorable for the design due to its supply voltage of 32 V, high slew-rate of 8000 V/μs, a gain-bandwidth product of 900 MHz, and a linear output

current of 420 mA. The first driver stage yields a differential-to-single-ended conversion with most gain. Effectively twice the voltage swing is achieved by utilizing the complementary input voltage pair, $V_{\text{in}+}$ and $V_{\text{in}-}$, which results in a lower gain setting for the supply modulator. The second stage is a non-inverting single-ended gain stage that introduces a dc offset voltage, V_{os1}, to prevent voltage clipping at the rail and move the signal closer to the desired dc output voltage. The third stage comprises of a low-gain non-inverting op-amp configuration with a feedback loop connected over the final two push-pull stages, which decreases the output impedance. At the inverting input a second dc offset voltage, V_{os2}, is applied to allow for the desired output voltage swings. The push-pull stages have a unity voltage gain, while the current gain is defined by the BJTs. A driver push-pull stage with smaller complementary PNP and NPN devices is needed to avoid problems with the final push-pull complementary pair, since the output stage op-amp cannot supply sufficient current to the base in a linear fashion. Moreover, at the emitters of the transistors *RC*-networks have been added to improve thermal stability. Between the two push-pull stages an additional *RC*-network is added to improve stability.

At the output a dynamic current sensing circuit is added to accurately compute the dynamic current draw of the PA under supply modulation in order to calculate the real-time efficiency [51]. A differential probe is connected over the 0.2 Ω sensing resistor to compute the dynamic current over time, V_{I}, while simultaneously the average current is measured with a multimeter at the decoupled output, $\overline{V_{\text{I}}}$. This extraction procedure will be discussed in more detail in Section 5.3.

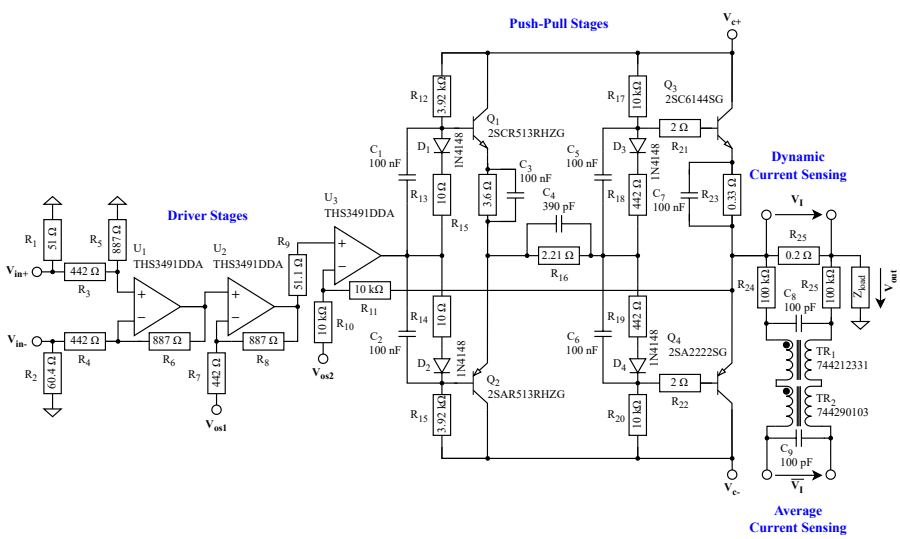


Figure 4.2: Simplified schematic of the first laboratory-grade continuous drain modulator design published in [Paper B], highlighting the driver stages for gain, complementary push-pull pairings as power stage, and drain current sensing circuitry for accurate dynamic current measurements.

Simulations were done with the Analog Devices LTspice software and the Printed Circuit Board (PCB) was designed in the Cadence OrCAD software. The PCBs were manufactured by Eurocircuits, employing standard four-layer pooling with an FR4 core substrate and chemical Nickel-Gold (Ni-Au) finish. All components were soldered onto the PCB using a stencil. The manufactured PCB of the push-pull drain modulator is depicted in Fig. 4.3, highlighting the driver stages, push-pull stages, current sensing circuitry, and RF/dc connections. Special care should be taken in the PCB design to limit the parasitic inductance in the feedback path from the push-pull stage to the output stage op-amps, going through resistor R_{11}. Moreover, the parasitic capacitance to ground around the op-amp pads is limited by removing the ground plane around and below the input and output pads. To prevent thermal issues within the op-amps, a grid of ground vias connecting from the top to the bottom layer through both intermediate layers are added below the package. Similarly, the output stage push-pull transistors are mounted to a heatsink with thermal paste in between to avoid overheating. With the jumpers the drain modulator can be configured for both GaN and GaAs devices, supporting voltage swings from 10 – 20 V and 0 – 4 V, respectively.

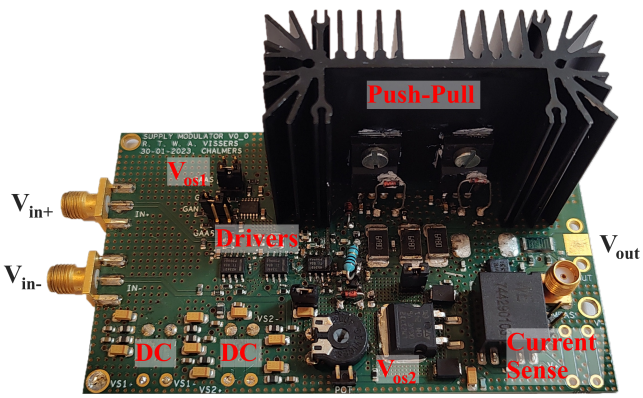


Figure 4.3: Manufactured PCB of the first laboratory-grade continuous drain modulator design published in [Paper B], highlighting the driver stages, push-pull output stage, and current sensing circuitry. The dimensions are 11.6×6×4 cm.

The drain modulator has been characterized in the GaAs configuration to evaluate the gain response, bandwidth, peaking behavior, and output impedance, as shown in Fig. 4.4. A range of frequencies are evaluated using a complementary sinusoidal input signal with a peak-to-peak voltage of 0.15 $V_{\text{pk-pk}}$. There is a significant discrepancy between the measured and simulated gain response, especially in terms of the signal peaking and high-frequency response, which can be attributed to the fact that the PNP and NPN devices did not have any parasitics modeled. This is especially crucial for the final push-pull complementary pair, since it uses a TO-220 package with large leads for the base, collector, and emitter, introducing additional unwanted parasitic induct-

ance. In the measurements the gain peaking value reaches 5.5 dB compared to 0.2 dB in simulations, while the measured half-power (3-dB) bandwidth is 130 MHz compared to 160 MHz in simulations. The output impedance is only simulated and stays below 5 Ω up to and including a frequency of 380 MHz. Lastly, an oscillation is observed at a frequency of 80 MHz, which is caused by the large gain peaking value due to the aforementioned parasitic inductances and capacitances. Possibly, this could have been avoided if a better model for the BJTs was available. In the GaN configuration, oscillation was imminent due to the aggressive gain peaking.

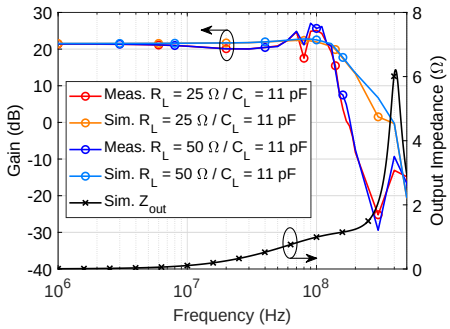


Figure 4.4: Measured and simulated large-signal response and simulated output impedance of the first laboratory-grade continuous drain modulator design published in [Paper B] in GaAs configuration. Two different load resistance values are tested, while the output capacitance is set by the compensated voltage probe capacitance, equaling 11 pF.

4.3 Load-Sharing Drain Modulator Design

Fig. 4.5 presents the second continuous linear regulator design published in [Paper A], consisting of eight Texas Instruments THS3491DDA high-speed current feedback op-amps distributed over two driver stages and one load-sharing output stage. The first stage is a differential-to-single-ended gain stage that yields most of the gain. The second stage is a non-inverting gain stage which introduces a dc offset voltage, V_{os1}, to avoid rail clipping. Hence, the first two stages are identical to the first prototype, as discussed in Section 4.2. The final stage is a load-sharing power stage which employs six current feedback op-amps in parallel. Each one of these op-amps has a linear output current of 420 mA, so combining six in parallel yields a linear output current of 2.52 A. Each output stage op-amp has a 10 Ω resistor at the output to improve the isolation to potential highly capacitive loads. In turn, this increases the output impedance of the linear regulator to approximately 1.7 Ω, having six devices in parallel. Moreover, a second dc offset voltage, V_{os2}, is applied to the output stage op-amps to ensure that the correct dc operating point is present at the output. Next to that, a PNP transistor is added at the output for current

injection if it is desired to reduce the average current of the output stage op-amps. It is crucial to connect the current injection circuitry to the middle of the six output stage op-amps due to the fact that the PNP BJT has an output capacitance of 100 pF. Connecting the PNP device to e.g. the top- or bottom-most op-amp would lead to an asymmetry in the design, which in turn yields an undesired output stage oscillation. The magnitude of the injected current can be tuned with variable resistor R_{40}. Lastly, the same dynamic current sensing circuit is added as in the first linear regulator design, of which the calibration procedure will be discussed in more detail in Section 5.3.

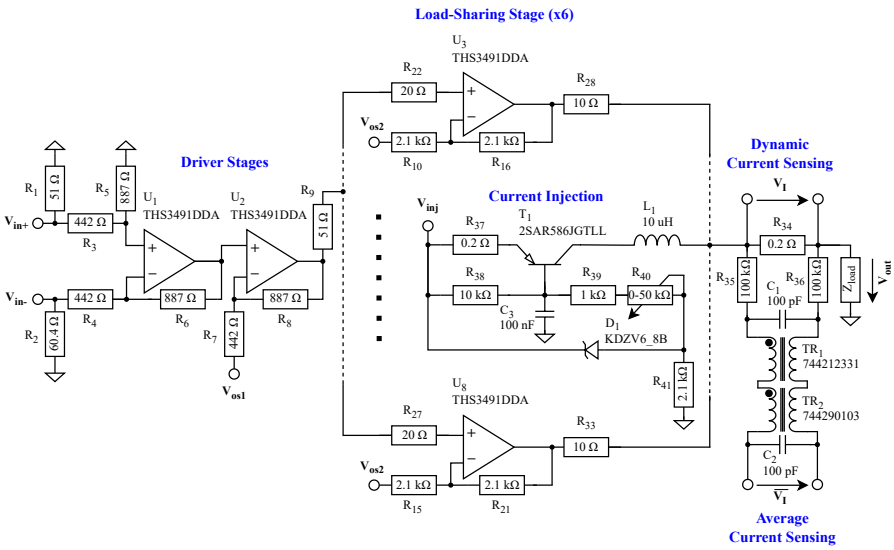


Figure 4.5: Simplified schematic of the second laboratory-grade continuous drain modulator design published in [Paper A], highlighting the driver stages for gain, load-sharing output stage with six parallel op-amps to handle at least 2.5 A of linear output current, current injection circuitry to reduce the average current of the output stage op-amps, and drain current sensing circuitry for accurate dynamic current measurements.

For this design simulations were done with the Keysight ADS software after converting the current feedback op-amp spice netlist to an ADS-compatible netlist. This enables the ability to run Electro-Magnetic (EM) simulations to improve the agreement between the measurements and simulations. Once more, the PCB design was done in the Cadence OrCAD software and the PCBs were manufactured by Eurocircuits, using the standard four-layer pooling with an FR4 core substrate and chemical Ni-Au finish. A stencil was used to solder all components on the PCB. Fig. 4.6 depicts the assembled load-sharing drain modulator PCB, highlighting the driver stages, load sharing output stage, current injection circuitry, ac current sensing circuitry, and RF/dc connections. As mentioned previously, the ground plane has been removed around and below the input and output op-amp pads to reduce the parasitic capacitance to

ground. Similarly, the ground plane has been removed around and below the feedback traces for all op-amps to reduce the parasitic capacitance. The output stage has two large combiner networks which were carefully EM-simulated to ensure balanced operation. A large grid of ground vias are added around the output stage op-amps to improve heat dissipation, connecting to both intermediate layers and the ground layer. Furthermore, the PCB is mounted on a heatsink to avoid overheating of the op-amps. Finally, the drain modulator can be reconfigured for both GaN and GaAs devices with the jumpers.

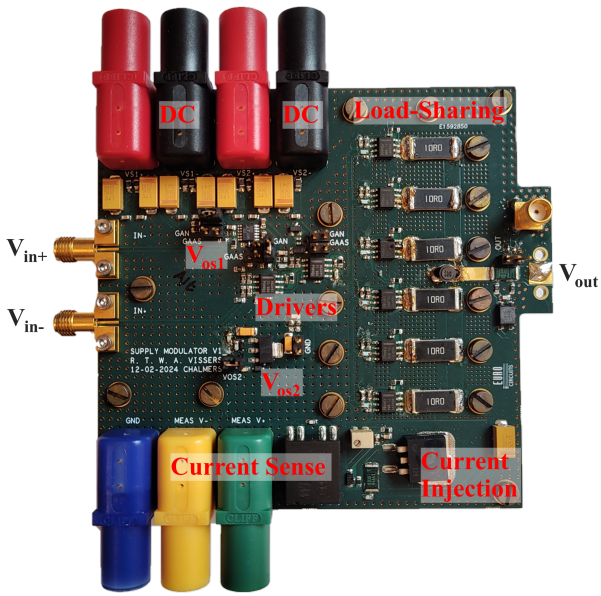


Figure 4.6: Manufactured PCB of the second laboratory-grade continuous drain modulator design published in [Paper A], highlighting the driver stages, load-sharing output stage, current injection capability, and current sensing circuitry. The dimensions are 12×12.5×5.5 cm.

Characterization of the drain modulator in GaN configuration is shown in Fig. 4.7, covering a range of frequencies from 1 MHz up to and including 500 MHz with a complementary sinusoidal input signal having an amplitude of 0.5 $V_{\text{pk-pk}}$. Excellent agreement is obtained between the measurements and simulations, even for the gain peaking and high-frequency response. For a 111 pF capacitive load the simulations yield a gain peaking value of 3.9 dB, while the measurements achieve an even lower gain peaking value of 1.5 dB. Moreover, a half-power bandwidth of 190 MHz is obtained in both measurements and simulations for the different capacitive loads. Lastly, a flat gain response with a simulated output impedance below 5 Ω is achieved up to a frequency of 80 MHz. To avoid unwanted envelope distortion, the increase in output impedance is the main bottleneck, especially for frequencies above 200 MHz where the simulated output impedance exceeds 15 Ω. Therefore, it is important that the bypass capacitors of the PA provide a low impedance path for frequencies above

200 MHz to prevent instabilities. This drain modulator design also works in the GaAs operation, which has been verified with additional measurements.

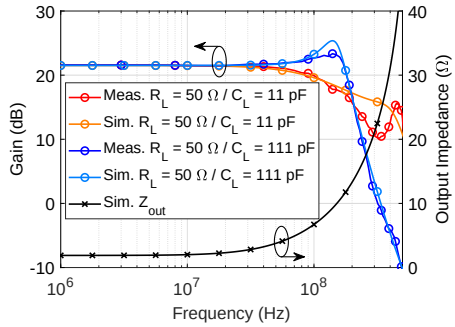


Figure 4.7: Measured and simulated large-signal response and simulated output impedance of the second laboratory-grade continuous drain modulator design published in [Paper A] in GaN configuration. The load resistance is kept at 50 Ω, while the output capacitance is varied.

Fig. 4.8 graphically illustrates the importance of performing EM simulations, providing a comparison of simulation results with and without EM-simulated combiner networks for the parallel op-amp output stage. One major observation is that no peaking behavior is present when the EM-simulated combiners are omitted. Next to that, the output impedance shows almost no variation over frequency compared to the case with EM simulations.

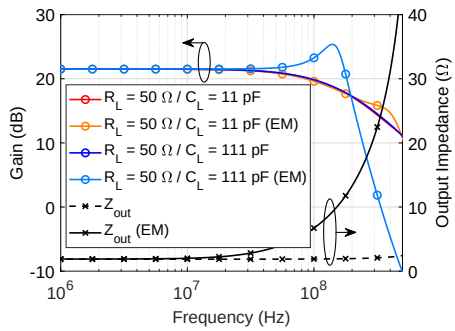


Figure 4.8: Simulated large-signal response and output impedance with and without EM-simulated combiner networks of the second laboratory-grade continuous drain modulator design published in [Paper A] in GaN configuration. The load resistance is kept at 50 Ω, while the output capacitance is varied.

Chapter 5

Dynamic Supply-Modulated Measurement Setup

This chapter presents a VNA-based measurement setup for modulated signal testing with drain modulation capability. The calibration procedure is discussed in great detail, including the VNA calibration steps, accurate extraction of the time-varying drain voltage and current waveforms, and time alignment of the RF and envelope signals. Section 5.1 presents the VNA-based modulated measurement setup with simultaneous input and output signal extraction. Section 5.2 shows the coherence options to correctly capture the signal on the VNA. Finally, Section 5.3 discusses the calibration procedure of the measurement setup, focusing on the VNA and supply modulator.

5.1 Modulated Measurements Setup

Modulated measurements are crucial to evaluate the PA operation under real-time communication scenarios with a specified bandwidth and PAPR. A multitone environment is defined by various individual sinusoidal input signals with different frequencies, which are the tones. These tones mix with each other due to the non-linear characteristics of the PA, which in turn leads to intermodulation distortion. This then yields undesired out-of-band emissions and spectral regrowth in the PA output spectrum.

The measurement setup for modulated signal testing with drain modulation, as published in [Paper A], is depicted in Fig. 5.1. It allows for generation of high-speed and real-time communication signals in a fully calibrated environment. Moreover, the setup supports drain modulation for PA efficiency enhancement. In Fig. 5.1 the internal hardware of the VNA is highlighted in blue, the external ports on the front panel are highlighted in magenta, and the calibration plane is highlighted in orange. A Keysight N5247B-423 VNA is used, which is configured in Spectrum Analysis (SA) mode. Some of the front panel jumpers have been removed to reroute the internal directional couplers of the VNA, ensuring that the isolated calibration plane is not affected by any external

component changes before forward receiver R1. One directional coupler of Port 3 is exploited since the forward directional coupler of Port 1 is inaccessible from the VNA front panel. To avoid compression of the internal receivers A, R1, B, and R2, external and internal attenuators are set accordingly. The Arbitrary Waveform Generator (AWG), mixer, driver amplifier, and Local Oscillator (LO) amplifier are independent of the calibration region and can thus freely be changed, as highlighted in red. The AWG, namely Keysight M8195A, produces real-time baseband communication signals at a sampling rate of 64 GSamples/s with an internal sample rate divider of 4, resulting in a sampling rate of 16 GSamples/s per channel. This generated baseband IQ data is then upconverted to the target RF frequency with an external mixer that takes the LO input directly from the Port 1 source output of the VNA. Furthermore, the AWG generates a specific tracking function for the drain modulator, as mentioned in Section 2.4, as well as a trigger signal for the oscilloscope. The Keysight DSOX3104G oscilloscope is configured such that it can wholly capture the tracking signal at a sampling rate of 2.5 GSamples/s to accurately measure the time-varying drain voltage and current waveforms. Multimeters are used to extract the average currents of the driver and PA stages, respectively. The main contribution of this setup is the possibility to simultaneously modulate and extract the drain voltage and current to accurately compute the efficiency improvement of drain-modulated PAs. This setup was further extended to on-wafer testing with Digital Pre-Distortion (DPD) capability in [Paper B].

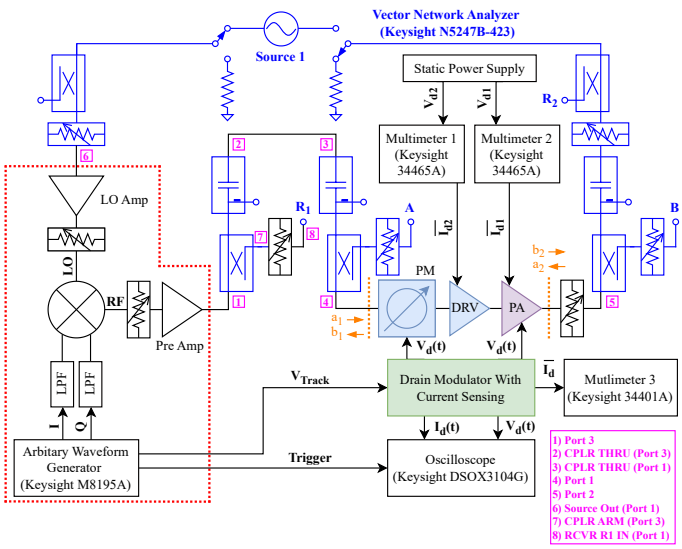


Figure 5.1: Schematic of measurement setup for modulated signal testing with drain modulation published in [Paper A], highlighting all internal components and connections of the VNA in blue, the external ports of the VNA in magenta, and the calibration plane in orange. Any external components within the red boundaries can freely be changed after calibration.

Fig. 5.2 presents the assembled measurement setup in the lab, highlighting the most crucial components and instruments. The complete setup is controlled through Virtual Instrument Software Architecture (VISA) instruments in MATLAB, utilizing the Instrument Control toolbox.

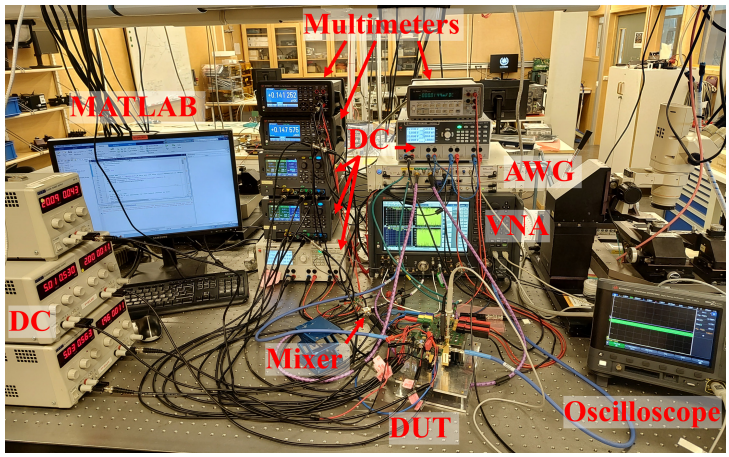


Figure 5.2: Assembled measurement setup for modulated signal testing with drain modulation.

5.2 Coherence

To correctly capture the signal it is important to have coherence between the AWG, VNA, and potentially, the oscilloscope. The 10 MHz reference clock is taken from the VNA and connected to the AWG. Next to that, the tone spacing, Δf_{tone}, has to be correctly set in the multitone environment of the SA mode of the VNA, which is calculated as

$$\Delta f_{\text{tone}} = \frac{f_{\text{s,VNA}}}{N_{\text{AWG}}}, \tag{5.1}$$

where $f_{\text{s,VNA}}$ is the sampling frequency of the VNA and N_{AWG} is the number of AWG samples. The Dynamic Range (DR) can be improved further with vector averaging, which yields more accurate measurements at increased measurement times. In the multitone environment of the VNA it is crucial to enable detector bypassing to compute the phases of the input and output signals. In this context the detector is an internal algorithm which maps the Discrete Fourier Transform (DFT) bins into display buckets, and thus is unable to display all individual phases of the input and output signals without bypass.

5.3 Calibration Procedure

A thorough calibration procedure has to be followed to obtain accurate measurements of the modulated RF signals, drain voltage, and drain current. Initially,

the VNA is calibrated with a Short-Open-Load-Through (SOLT) calibration by connecting the Port 1 source output directly to Port 3, denoted by nodes 6 and 1 in Fig. 5.1, respectively. Hence, no external components are added during calibration. To improve the accuracy of the VNA calibration, especially for the phase readings, averaging with a low Intermediate Frequency (IF) bandwidth is necessary, which significantly increases the calibration time.

For the drain modulator, the dc and ac components of the time-varying drain voltage, $V_{\mathrm{d}}(t)$, are extracted simultaneously with a compensated voltage probe connected to the output SMA connector shown in Fig. 4.6. For a static 20 V bias at the drain modulator output a 50 mV offset has been measured between the compensated voltage probe and a multimeter reading, which should be taken into account.

The drain current sensing circuitry depicted in Fig. 5.3 is used to accurately compute the dc and ac components of the time-varying drain current by measuring the voltage drop over the 0.2 Ω sensing resistor [51]. Prior to the measurements, the exact value of the 0.2 Ω sensing resistor has to be determined, which is done by connecting a known 48 Ω termination to the output SMA connector of the drain modulator. For a static 20 V bias at the drain modulator output the current through the known 48 Ω load is computed, after which the exact value of the sensing resistor, $R_{\mathrm{sense,cal}}$, is calculated as

$$R_{\mathrm{sense,cal}} = \frac{\overline{V_{\mathrm{I}}} \cdot V_{\mathrm{out}}}{R_{\mathrm{load}}}, \tag{5.2}$$

where $\overline{V_{\mathrm{I}}}$ is the decoupled output voltage, V_{out} is the voltage through the load, and R_{load} is the known termination resistor of 48 Ω.

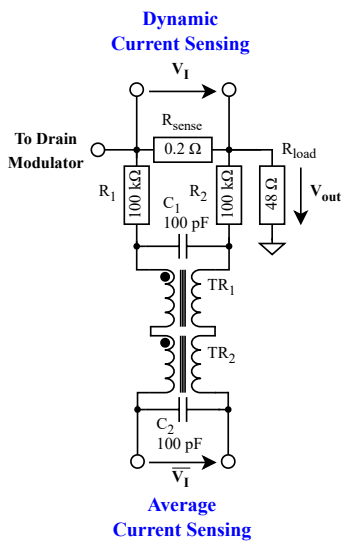


Figure 5.3: Calibration of drain current sensing circuitry for accurate dynamic current measurements with a known 48 Ω output termination.

Now that the exact value of the 0.2 Ω sensing resistor is known, the ac component of the time-varying drain current, $I_{\mathrm{d}}(t)$, is extracted with a differential probe connected over the sensing resistor, while the averaged dc component, $\overline{I_{\mathrm{d}}}$, is measured with a multimeter at the decoupled output. These two parts are extracted individually, since the differential probe is prone to dc drifting due to variations in temperature and probe positioning, which would reduce the accuracy of the dc reading. On the oscilloscope the dynamic voltage and current waveforms are time-aligned by computing their respective cross-correlation for a 100 MHz band-limited noise signal with the known 48 Ω load connected. A skew is introduced on the oscilloscope, which is kept for all future measurements. Now, the dynamic power consumption can be accurately computed by multiplying the aligned voltage and current waveforms, respectively.

Lastly, it is crucial that the correct drain voltage is presented for its corresponding input power level, so the delay between the RF and envelope path has to be computed [93]. Fig. 5.4 presents the transmitted and received time alignment signals for synchronization, where the RF signal is a 64 μs-long sequence with 16-QAM modulation from 8 μs – 40 μs and a static amplitude elsewhere for the I- and Q-signals, while the drain modulator signal is a 64 μs-long sequence with Amplitude Modulation (AM) from 48 μs – 56 μs and a static amplitude elsewhere. At the output of the PA both the RF signal with 16-QAM modulation and a delayed version of the drain modulator signal with AM are visible. By computing the cross-correlation of the PA output signal and the drain modulator AM signal, a delay of 10.9 ns is observed [50].

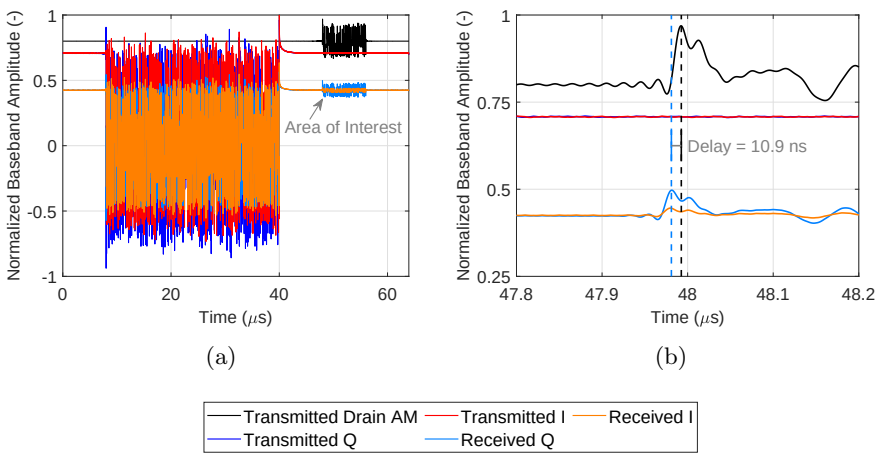


Figure 5.4: Measured transmitted and received time alignment signals for synchronization of the RF and envelope path including (a) full signal time span and (b) zoomed-in on area of interest, yielding a delay of 10.9 ns.

Chapter 6

Supply Modulation With Analog Phase Linearization

In [Paper A] a novel tuneable analog phase linearization method for drain-modulated PAs is presented. This chapter will discuss the phase correction concept, synthesis of various tracking functions, and modulated measurement results. Section 6.1 provides a motivation for this work. In Section 6.2 the phase linearization concept and the fully assembled amplifier system are shown. Section 6.3 presents the tracking function synthesis, backed by CW measurement results. Lastly, Section 6.4 discusses the modulated measurement results for a 33.75 MHz, 6 dB PAPR input signal with a 16-QAM modulation format.

6.1 Motivation

The amplitude and phase linearity of supply-modulated PAs are highly dependent on the applied tracking function, since the transistor operating point changes dynamically [28], [39]. As mentioned in Section 2.4 a flat gain trajectory exploits the non-linear gain characteristics of the PA to improve the amplitude linearity, while the phase linearity remains uncorrected. These phase non-linearities can be resolved with DPD algorithms [94], [95], which tend to have high computational complexity and can only be exploited if knowledge of the PA and IQ baseband data is available. Typically, in ground-to-satellite or mobile communication links the IQ baseband knowledge is unavailable, so the phase non-linearities have to be resolved with Analog Pre-Distortion (APD) techniques. Previously, analog phase correction for supply modulation was implemented statically with a deliberate mismatch of the source and load impedance of the PA [41]–[43], or dynamically with a phase detector feedback loop [96] or ET feedback loop [97]. These dynamic implementations both require additional control circuitry, which adds more design complexity and increases the power dissipation. The work in [Paper A] focuses on a dynamic analog phase correction method without the need for any additional control circuitry to improve the efficiency and phase characteristics of supply-modulated PAs.

6.2 System-Level Overview

The work of [Paper A] presents a tuneable APD method for phase correction in ET PA systems by integrating a custom tuneable phase modulator MMIC directly in the PA RF input path, as depicted in Fig. 6.1. The phase modulator exhibits an inverse phase characteristic compared to the PA, which corrects the phase distortion under drain modulation at the output. It can be seen that the phase modulator takes the time-varying drain voltage, $V_{\mathrm{d}}(t)$, of the PA as it control signal, and therefore, no additional control circuitry is required. Thus, the phase modulator will have negligible power consumption with a limited insertion loss below 3.4 dB. Since it is added prior to the PA and driver amplifier, this loss will have limited to no impact on the efficiency calculation. A custom linear driver amplifier is needed to drive the PA into its compression region and to ensure that the phase modulator operates in its linear region. For an intended application, the system is complemented with a directional coupler that feeds the RF input signal to an envelope detector, where the output signal will be shaped accordingly and fed to the drain modulator. This leaves the system and linearization method in an analog fashion.

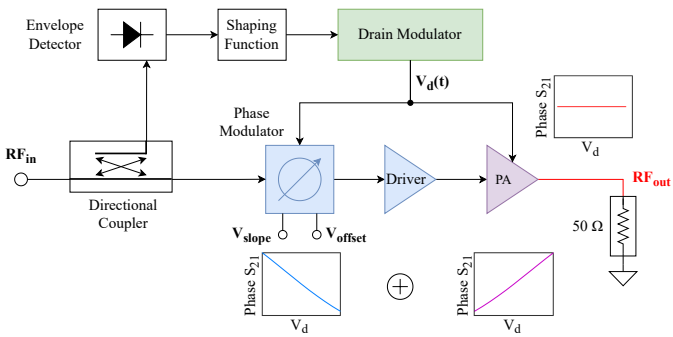


Figure 6.1: Simplified block diagram of the drain-modulated power amplifier with output phase correction using a phase modulator. The phase modulator employs an inverse phase characteristic (in blue) compared to the PA (in purple), which linearizes the output phase (in red). Each distinct color represents a separate PCB in the modular amplifier assembly.

The fully assembled amplifier is shown in Fig. 6.2, with annotations for all five custom modular parts. As mentioned in Section 4.3, the drain modulator is mounted on a heatsink to prevent overheating. Subsequently, the heatsink is mounted onto a fan, which is screwed onto the aluminum base plate. Similarly, the PA MMIC is mounted onto a carrier for heat dissipation, which is affixed to the aluminum base plate. To connect the time-varying drain voltage of the PA to the phase modulator for dynamic phase correction, an additional bias interconnect PCB is designed. The PCB that houses the phase modulator and driver MMICs was manufactured by Eurocircuits, following the RF pooling design rules for a 0.5 mm Rogers RO4350B core substrate. The PA, phase modulator, and driver amplifier MMICs will be discussed in more detail.

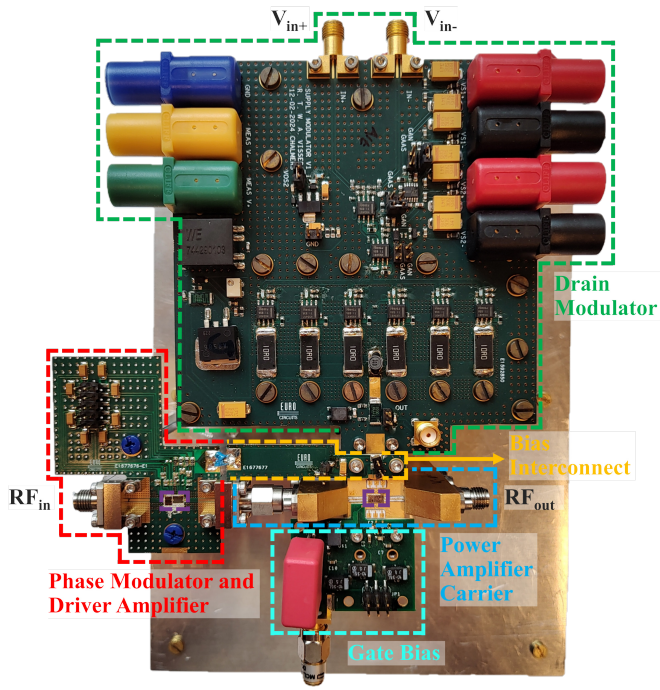


Figure 6.2: Fully assembled amplifier, highlighting its five modular parts with dimensions 16.5×20×10 cm.

The PA MMIC is designed in a 150 nm GaN-on-SiC process, which utilizes a 100 μm SiC substrate and supports a drain voltage up to 28 V. This PA consists of three stages with staging ratio 1:2:8 and is optimized for drain modulation of the last two stages [20]. It has a saturated output power of 36.5 dBm with a PAE of 40 – 45%. The large-signal saturated gain is 25 dB and covers a frequency span from 18.5 GHz up to 24.0 GHz. These results are obtained through static characterization of the PA with a drain voltage of 20 V and a quiescent current of 100 mA/mm for each stage.

Additional CW measurements are performed at a frequency of 20.5 GHz, which yields the maximum PAE. Now, the drain voltage of the last two stages of the PA is varied between 10 V and 20 V, which shows an output phase shift of 4° per 1 V step, as presented in Fig. 6.3. It can be seen that for a pure ET trajectory, as discussed in Section 2.4, the output phase of the PA varies by 42° over the range of drain voltages and versus output power. In turn, this will severely degrade the linearity metrics of the PA and thus has to be resolved.

The phase modulator MMIC was custom designed in the WIN Semiconductors PIH1-10 E-mode pHEMT process, which utilizes a 100 μm GaAs substrate. The chip photograph and simplified schematic are depicted in Fig. 6.4, where in the schematic the decoupling capacitors at the bias nodes are omitted. The core circuit is similar to the one published in [98], replicating a reflective tuneable phase modulator. To allow the time-varying drain voltage that feeds the PA to

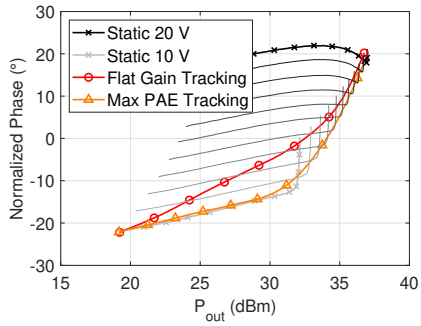
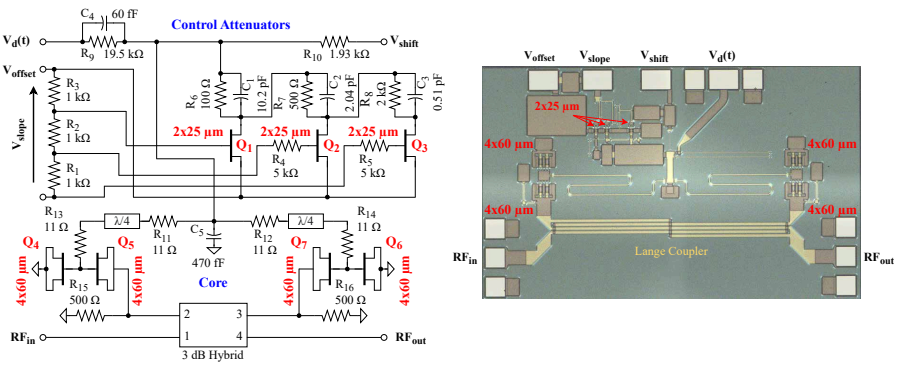


Figure 6.3: Measured PA phase variation for increasing drain voltages versus output power at a frequency of 20.5 GHz. Light gray indicates a drain voltage of 10 V and black indicates a drain voltage of 20 V in 1 V steps. The PA phase variation is illustrated for a flat gain and maximum PAE pure ET function, varying 42° over output power.

be connected directly to the phase modulator, the circuit is extended with a resistive voltage divider formed by R_9 and R_{10}. This network provides the bias voltage for the diode-connected HEMTs Q_4 – Q_7, acting as varactors. The negative voltage reference is set by the shifting voltage, V_{shift}, which can be set to alter the operating voltage range of the phase modulator. The high impedance voltage divider is loaded by bypass capacitor C_5 and the input capacitance of the varactors, which yields a low-pass frequency response of 50 kHz, prohibiting wideband modulated signals. Subsequently, this is counteracted with bypass capacitor C_4, which results in a frequency-flat voltage divider.



(a) (b)

Figure 6.4: Phase modulator (a) simplified circuit diagram and (b) chip photograph, highlighting the control attenuators to tune the slope and offset of the phase, as well as the core circuit published in [98]. The MMIC dimensions are 1.92×1.17 mm.

Moreover, an adjustable shunt resistor is implemented with three transistors $Q_1 - Q_3$, together with resistors $R_6 - R_8$, which allows for a reduction of the voltage swing across the varactors. This is controlled by the slope voltage, V_{slope}, which yields a continuous slope adjustment for the phase modulator and supports a voltage attenuation from the time-varying drain voltage to the diode bias by 21 – 45 dB. Next to that, transistors $Q_1 - Q_3$ are terminated at an additional offset voltage, V_{offset}, which can be adjusted such that these devices operate in the ohmic region. The usable range of the control attenuator is extended by connecting transistors $Q_1 - Q_3$ to the varactor bias point through a resistor ladder formed by $R_6 - R_8$, while the gate bias is provided through resistors $R_1 - R_3$. This ensures that transistor Q_3 will turn on prior to Q_1. Bypass capacitors $C_1 - C_3$ are reciprocally sized to resistors $R_6 - R_8$ to ensure that the bypass capacitance over the shunt attenuator increases when the resistance decreases. This ensures that the voltage divider has a flat response over frequency.

The effect of bypass capacitors $C_1 - C_4$ on the control voltage transmission coefficient over frequency is shown in Fig. 6.5. These simulations adhere to an attenuation setting of 40 dB, which corresponds to $V_{\text{slope}} = 1$ V. It can immediately be seen that bypass capacitor C_4 is crucial to prevent a drop at higher frequencies. Bypass capacitors $C_1 - C_3$ further flatten out the frequency response for different control attenuator settings. Another noticeable observation is that the small-signal frequency response is dependent on the drain voltage, which is due to the changing capacitance of the varactors. This can be counteracted with additional active buffers or other power consuming circuits, which is undesired.

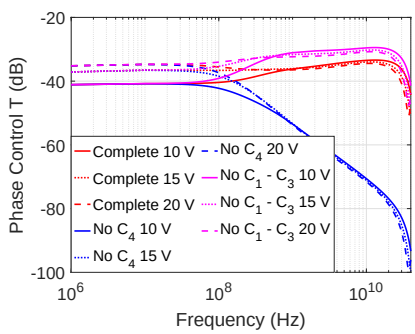
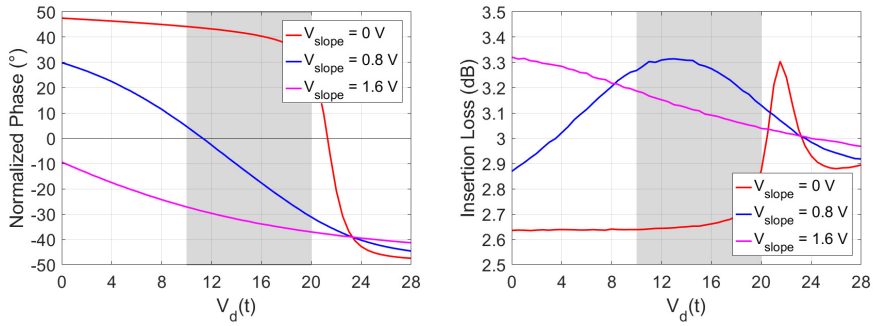


Figure 6.5: Simulation results of the control signal voltage transmission coefficient versus frequency with $V_{\text{slope}} = 1$ V and varying drain voltages.

Small-signal CW measurements were performed to evaluate the insertion loss and normalized phase behavior for varying drain voltages, as presented in Fig. 6.6. It can be observed that the phase slope is altered by changing the control attenuator bias, as shown in Fig. 6.6a. In the desired drain supply voltage region of 10 – 20 V a linear phase response with 35° is obtained for $V_{\text{slope}} = 0.8$ V. Fig. 6.6b depicts the insertion loss, which stays below 3.4 dB over the drain bias voltage range. An undesired gain variation of less than

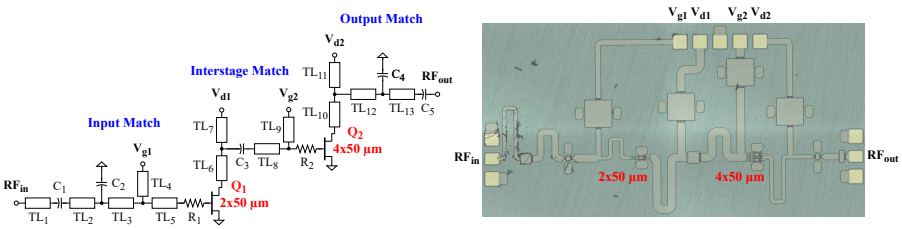
±0.1 dB is measured in the 10 – 20 V drain supply region for V_{slope} = 0.8 V.



(a) (b)

Figure 6.6: Measurement results of (a) normalized phase versus drain voltage and (b) insertion loss versus drain voltage at a frequency of 20.5 GHz for varying V_{slope} with a fixed V_{offset} of 0.5 V and V_{shift} of -1.75 V. The desired drain supply voltage region from 10 – 20 V is highlighted in light gray.

Lastly, a custom linear driver amplifier was designed and manufactured in the WIN Semiconductors NP12-01 120 nm GaN-on-SiC process, which targets mm-wave applications through 50 GHz. It is manufactured on 100 mm SiC substrates and employs a source-coupled field plate design for high breakdown voltage and reliable operation at a drain voltage of 28 V. The schematic and layout of the driver amplifier are shown in Fig. 6.7, employing a two-stage architecture to provide sufficient gain to drive the PA into full saturation. Load-pull analysis has been performed on the output stage to evaluate the optimum impedance for maximum output power. The interstage and input match both employ a conjugate match to enhance the gain of the driver. Both stages have a 20 V drain bias with a quiescent current of 94.3 mA/mm as a trade-off between gain, output power, and PAE.



(a) (b)

Figure 6.7: Driver amplifier (a) simplified circuit diagram and (b) chip photograph, highlighting the different matching network topologies used. The MMIC dimensions are 2.84×1.40 mm.

The small-signal measurement and simulation results of the driver amplifier

are presented in Fig. 6.8, where an excellent agreement is observed. A maximum small-signal gain, S_{21}, of 21.0 dB with a half-power bandwidth spanning from 17.9 GHz up to 24.5 GHz is achieved.

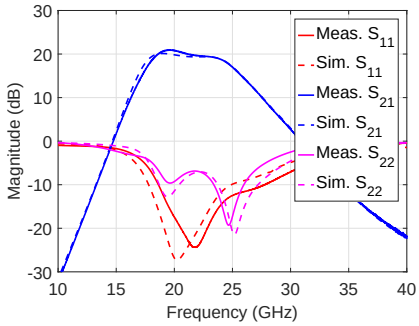
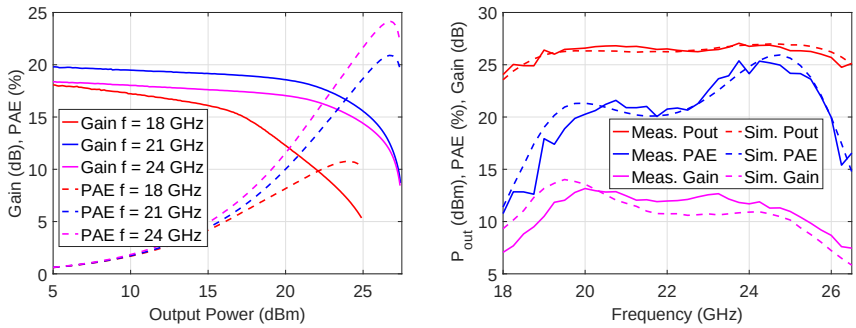


Figure 6.8: Measured and simulated small-signal response of the driver amplifier.

Large-signal characterization results of the driver amplifier are depicted in Fig. 6.9. To drive the PA fully into saturation it requires an input power level of 15 dBm, which can be supplied with 0.5 dB compression at a frequency of 21 GHz, as becomes evident from Fig. 6.9a. The maximum PAE of 25.4% is obtained at a frequency of 23.8 GHz, where the resulting large-signal gain is 11.8 dB, as shown in Fig. 6.9b.



(a) (b)

Figure 6.9: Large-signal measurement results of (a) PAE and gain versus output power and (b) output power, PAE, and gain at the maximum PAE point versus frequency.

6.3 Tracking Function Synthesis

A variety of tracking functions are investigated to obtain flat gain characteristics or achieve maximum PAE. The work of [Paper A] uses the bandwidth-reduced

PT, PT2, and PT2R tracking functions, as well as pure ET, as mentioned in Section 2.4. For each of these functions the $V_{\mathrm{d}}(P_{\mathrm{in}})$ mapping is computed from static PA measurements with varying drain voltages from 10 – 20 V in 1 V steps, where the result is presented in Fig. 6.10. The flat gain PT and PT2 trajectories have similar trends, but the PT2 trajectory becomes slightly more accurate for an increasing input power level. Next to that, the PT2R trajectory seems to be a significantly worse fit compared to the pure ET case. For maximum PAE tracking it shows that the PT2 and PT2R trajectories are an almost perfect fit to the pure ET function. However, the PT tracking function cannot accurately follow the ideal ET trajectory.

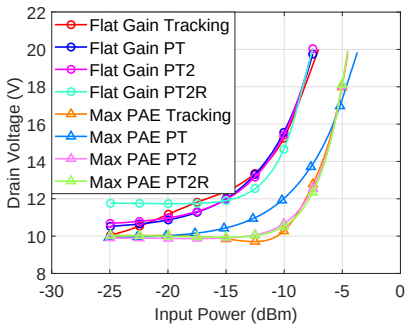


Figure 6.10: Synthesized tracking functions for flat gain and maximum PAE tracking versus input power.

Fig. 6.11 shows the CW measurement results of the amplifier at a frequency of 20.5 GHz for a varying drain voltage from 10 – 20 V without phase correction, as well as the evaluated tracking functions with phase correction. A constant gain value of 44.5 dB is set for the flat gain tracking functions, defined by the lower drain voltage limit of 10 V. It can be seen that the pure flat gain ET function exhibits an excellent response with a gain variation limited to ±0.05 dB over the measured 16 dB of DR. Furthermore, the PT and PT2 trajectories are a solid approximation of the pure ET function, having a gain variation of ±0.5 dB over the measurement range. The PT2R trajectory seems to be lacking in accuracy, especially in the back-off region. For maximum PAE tracking it can be seen that the peaks of the static PAE measurements are nicely followed by the pure ET, PT2, and PT2R trajectories. The maximum PAE PT function lacks accuracy in back-off, but can still reach the static PAE peaks for higher output power levels. This function is a trade-off between flat gain and maximum PAE tracking.

A PAE of 22.7% is measured at an output power level of 32 dBm for a static 20 V bias, which is improved to 29.5% for flat gain tracking and 32.9% for maximum PAE tracking, as can be seen in Fig. 6.11c. The phase correction is also clearly visible in Fig. 6.11b, showing that the output phase variation of 42° without phase correction is reduced to only 8 – 10° with the phase modulator enabled. In turn, this significantly improves the phase linearity under drain modulation.

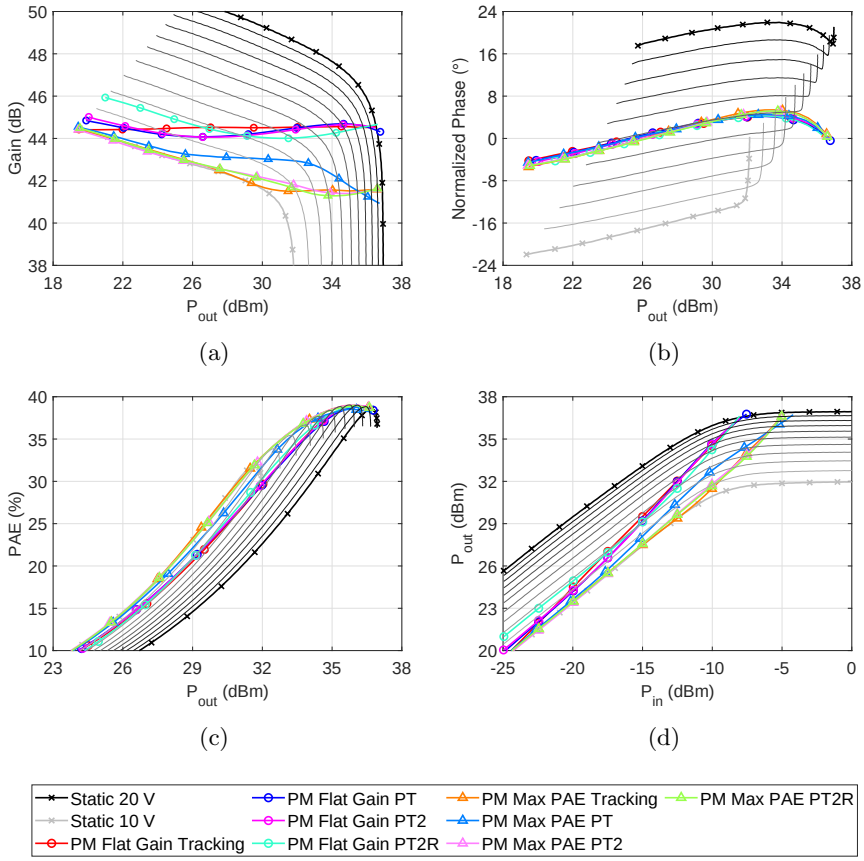
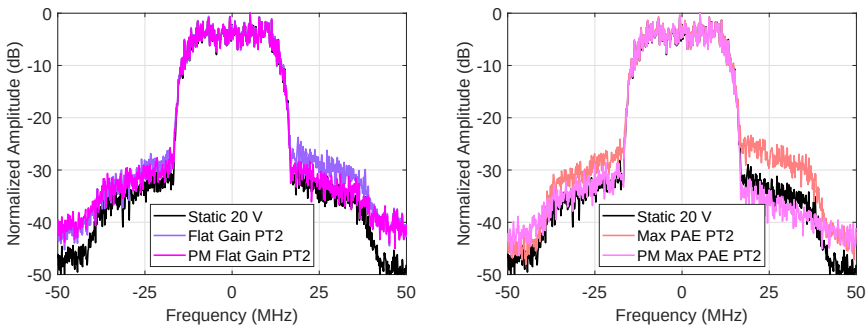


Figure 6.11: CW measurement results of (a) gain versus output power, (b) normalized phase versus output power, (c) PAE versus output power, and (d) compression characteristics versus input power at a frequency of 20.5 GHz for flat gain and maximum PAE tracking. The light gray to black lines correspond to static drain voltages spanning from 10 V up to 20 V in 1 V steps with the phase modulator disabled. Traces denoted with PM indicate that the phase modulator is enabled.

6.4 Modulated Measurements

Modulated measurements are performed with a 33.75 MHz, 6 dB PAPR input signal with a 16-QAM modulation format, utilizing the measurement setup presented in Section 5.1. The generated real-time baseband signal is up-converted to the target frequency of 20.5 GHz with an external mixer. The output spectra for the flat gain and maximum PAE PT2 tracking functions are depicted in Fig. 6.12, where the spectral regrowth is imminent under supply modulation without phase correction compared to a static 20 V bias. With the phase modulator enabled the adjacent channel power is reduced to

achieve a similar or even better linearity performance compared to a static 20 V bias. An asymmetry is visible in the output spectra due to memory effects in the amplifier, specifically due to the non-zero output impedance of the drain modulator. This also becomes more evident when looking into the gain and phase characteristics.



(a) (b)

Figure 6.12: Measured normalized output spectra for (a) flat gain PT2 and (b) maximum PAE PT2 at a frequency of 20.5 GHz and an average output power level of 32 dBm. Traces denoted with PM indicate that the phase modulator is enabled.

The gain and phase characteristics for flat gain and maximum PAE PT2 at an average output power level of 32 dBm are shown in Fig. 6.13. A rising slope is observed for the flat gain PT2 function, while the maximum PAE PT2 function exhibits a flat gain behavior. This is due to the fact that the memory effects are more prominent under modulated signal testing [29], while the tracking functions were synthesized based on CW measurements. The gain reduction at low output power levels is attributed to trapping effects in the GaN epistructure [99]. Hence, it would be more accurate to characterize the PA with supply modulation in a controlled trapping state environment, which can be achieved with prepulsing [58].

A static 20 V bias yields the highest gain, exceeding 50 dB, but the gain flatness is compromised due to soft compression of the PA. The output phase varies by 9° for the static 20 V bias. This phase variation becomes significantly worse under supply modulation without phase correction, namely 25 – 30°. Enabling the phase modulator decreases the output phase variation to only 14°. Another noticeable observation is that the output phase is overcompensated for an output power level greater than 33 dBm, which could be further improved by altering V_{slope} and V_{offset} of the phase modulator.

Fig. 6.14 presents the average PAE versus average output power, as well as the average PAE improvement compared to having a static 20 V bias. At 6 dB back the average PAE is improved by 6.5 – 7.2 percentage points (pp) for flat gain tracking and 8.7 – 9.5 pp for maximum PAE tracking. The power consumption of the laboratory-grade drain modulator is not taken into account

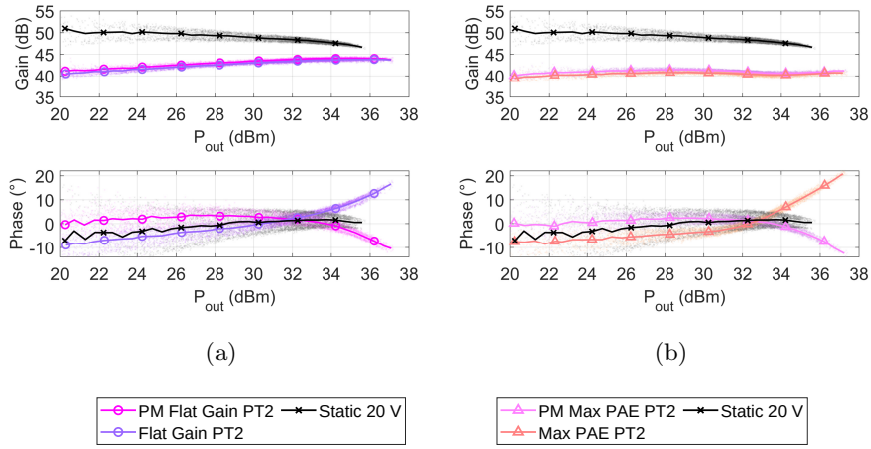


Figure 6.13: Modulated measurement results of (a) gain and phase versus output power for flat gain PT2 and (b) maximum PAE PT2 at a frequency of 20.5 GHz and an average output power level of 32 dBm. The dots represent individual samples and the lines represent the moving average through these samples. Traces denoted with PM indicate that the phase modulator is enabled.

in the efficiency calculations, as it is seen as a measurement tool. Hence, only the power consumption of the phase modulator, driver amplifier, and PA MMICs are considered.

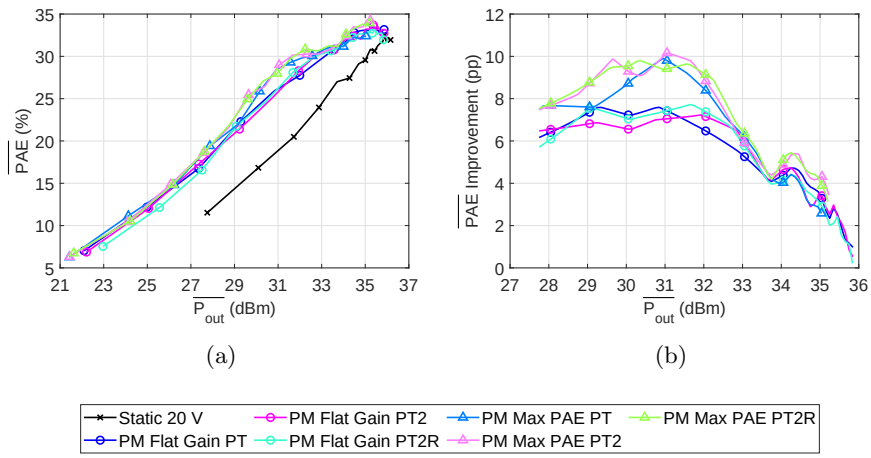


Figure 6.14: Modulated measurement results of (a) average PAE versus average output power and (b) average PAE improvement compared to a static 20 V bias versus average output power at a frequency of 20.5 GHz for flat gain and maximum PAE tracking. Traces denoted with PM indicate that the phase modulator is enabled.

Linearity is investigated in terms of the Adjacent Channel Power Ratio (ACPR) and RMS EVM and is shown in Fig. 6.15. For the flat gain PT and PT2 trajectories the ACPR improves by 3 – 4 dB in back-off with the phase correction enabled, which reflects to an RMS EVM improvement of 1.5 – 2 pp. The flat gain PT2R trajectory follows a near-static 12 V bias up to an average output power level of 27 dBm, thus showing similar ACPR and RMS EVM for the corrected and uncorrected case. For an output power level exceeding 27 dBm, an ACPR improvement of 2 – 3.5 dB is observed with phase correction, which yields a reduction in the RMS EVM of 0.7 – 1.5 pp.

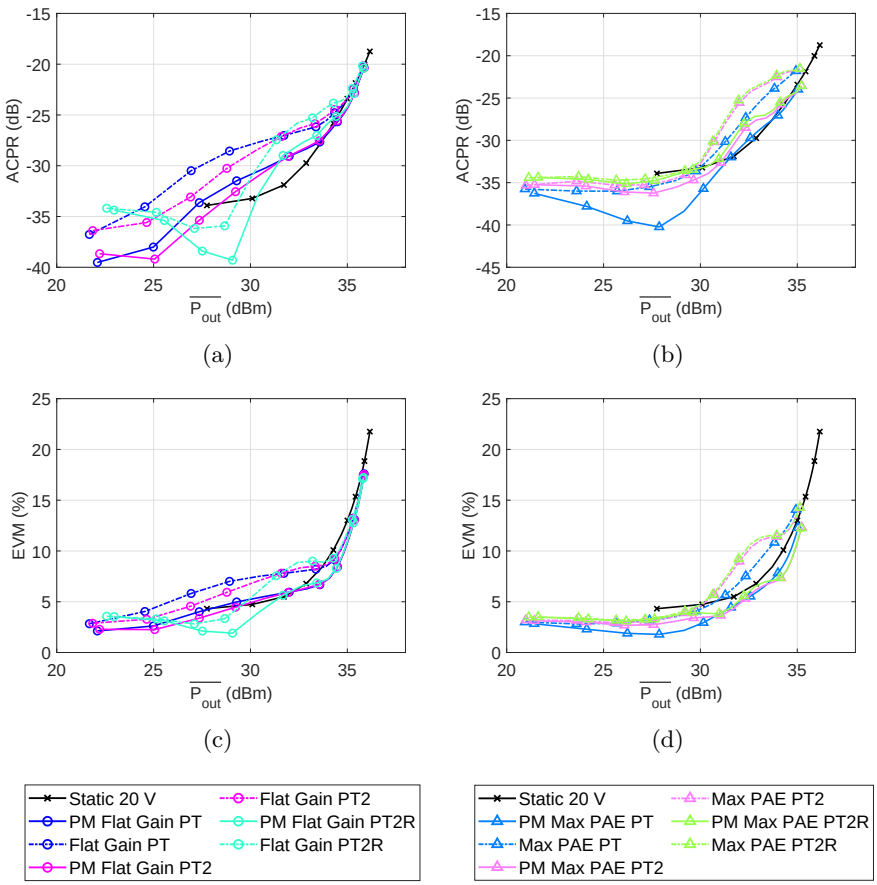


Figure 6.15: Modulated measurement results of (a) ACPR versus average output power for flat gain tracking and (b) maximum PAE tracking, and (c) RMS EVM versus average output power for flat gain tracking and (d) maximum PAE tracking at a frequency of 20.5 GHz. Traces denoted with PM indicate that the phase modulator is enabled.

Similarly, the ACPR and RMS EVM of the maximum PAE PT2 and PT2R trajectories are almost equal with and without phase correction up to an

average output power level of 29 dBm, since a near-static drain bias of 10 V is observed. For an average output power greater than 29 dBm, the ACPR improves by 3 – 5 dB and the RMS EVM shows an improvement of 2 – 4 pp with the phase modulator correction. The maximum PAE PT function shows an ACPR improvement of 2 – 5 dB with an RMS EVM improvement of 1.5 – 3 pp over the full average output power range with the phase modulator active.

Once again it can be seen that the maximum PAE tracking functions generally show better linearity in comparison to the flat gain tracking functions. As mentioned previously, all tracking functions were synthesized based on static CW measurements, and therefore the memory effects of the amplifier were not taken into account. Since a reduced voltage swing on the drain is observed, these memory effects become less prominent for an average output power level below 28 dBm. In turn, this improves the ACPR for the flat gain tracking functions for reduced average output power levels. However, the maximum PAE tracking functions achieve similar or even better linearity performance compared to having a static 20 V bias over the whole measured average output power range, since both the gain and phase exhibit more linear behavior under modulated signal testing.

As concluded from the gain and phase characteristics in Fig. 6.13, the phase was slightly overcompensated for an increasing output power level, which increases the ACPR. For a set average output power level the ACPR can be further reduced by sweeping V_{slope} and V_{offset} of the phase modulator to find the optimal bias point for phase correction, as presented in Fig. 6.16. Since V_{slope} is referenced to V_{offset} a parallelogram shape is obtained. The optimal bias point that yields the lowest ACPR of -36.8 dB is given by $V_{\text{slope}} = 1.02$ V and $V_{\text{offset}} = 0.48$ V.

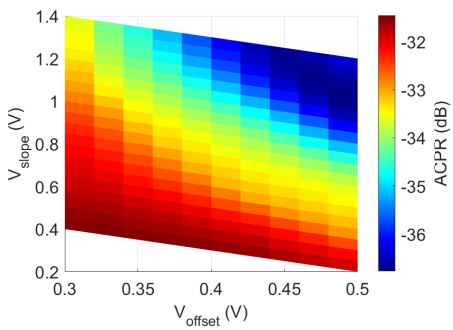


Figure 6.16: Modulated measurement results of ACPR versus V_{slope} and V_{offset} of the phase modulator for maximum PAE PT tracking at a frequency of 20.5 GHz and an average output power level of 30 dBm.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis has provided a comprehensive investigation of supply-modulation for back-off efficiency enhancement, driven by the growing demand for higher data throughput with high energy efficiency. The main focus lays on drain modulation, which can significantly enhance the back-off efficiency by reducing the voltage overhead of the PA. However, this improvement comes at the cost of reduced gain and phase linearity due to the varying supply voltage. The gain flatness can be improved by utilizing a specified tracking function, while the phase non-linearity has to be resolved in another way.

One of the achievements of this thesis is the design and characterization of two custom laboratory-grade continuous supply modulators. The first design exhibits a push-pull output stage nested in a non-inverting op-amp feedback loop for high output current handling and to obtain a very low output impedance. Unfortunately, this design showed an oscillation due to the lack of modeled parasitics in the BJTs. The second design accommodates a parallel load-sharing output stage to provide sufficient linear output current with a bandwidth of 130 MHz.

Another achievement is the development of a VNA-based modulated measurement setup with drain modulation capability. This setup supports simultaneous input and output extraction, supply modulation, and if desired, DPD. The calibration procedure has been discussed in great detail, focusing on the VNA and drain modulator.

The main achievement of this thesis is the novel analog phase correction method, implemented with a custom tuneable phase modulator MMIC in the PA RF input path to counteract the drain voltage-induced phase characteristic of the supply-modulated PA. The custom tuneable phase modulator MMIC was designed in the WIN Semiconductors PIH1-10 E-mode pHEMT GaAs process. This phase modulator directly uses the time-varying drain voltage of the PA

as its control signal. The overall system efficiency is not influenced, since the phase modulator has a low insertion loss and negligible power consumption. Modulated measurements have verified that the analog linearization method achieves a similar or even better linearity in comparison to having a static 20 V bias, while the back-off efficiency is improved by up to 9.5 pp for maximum PAE tracking.

In summary, this thesis has provided theoretical and practical insight into supply modulation, addressing a new way to overcome unwanted non-linearities. These finding will contribute to the advancement of modern wireless communication systems by improving linearity and efficiency.

7.2 Future Work

Built upon the findings of this thesis there are several research directions to pursue. The author believes the following topics might be interesting to investigate in the future:

- **Highly efficient discrete supply modulator design.** Chapter 4 presents two laboratory-grade continuous supply modulators that are highly inefficient and were not considered in the efficiency calculations. A discrete supply modulator could be included in the compound efficiency computation to compute a more accurate efficiency improvement.

- **Discrete supply modulation with phase correction.** Chapter 6 introduces the phase correction method under continuous supply modulation. The phase modulator was initially designed for high-bandwidth discrete supply modulation, which might be worthwhile to investigate. The phase modulator could also compensate for potential ringing, which is common for discrete supply modulators.

- **Wider modulation bandwidths.** In Chapter 6 a modulation bandwidth of 33.75 MHz is used, which could be extended to e.g. 50 MHz or even 100 MHz following the bandwidth specifications of the laboratory-grade continuous supply modulator.

- **Simultaneous analog and digital linearization.** The setup proposed in Chapter 5 supports APD and DPD. Therefore, it might be interesting to investigate if the linearity can be further improved with simultaneous APD and DPD.

- **Dynamic extraction of tracking functions.** In Chapter 2 and Chapter 6 it was mentioned that the tracking functions were synthesized based on CW measurements, thus not taking into account potential memory effects. For more accurate synthesis it would be valuable to characterize the PA in a controlled trapping state.

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