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A Balanced 100-114 GHz Millimeter-Wave GaAs MMIC Power Amplifier with High Gain

Göksu Kaval, *Graduate Student Member, IEEE*, Gregor Lasser, *Member, IEEE*, Marcus Gavell, *Member, IEEE*, and Christian Fager, *Senior Member, IEEE*

***Abstract*—This paper presents a balanced MMIC power amplifier (PA) operating from 100 to 114 GHz for backhaul applications, fabricated using a commercial 0.1 µm GaAs pHEMT technology. The amplifier achieves a saturated output power ranging from 20.3 dBm to 24.1 dBm, with a power-added efficiency (PAE) between 5.3% and 11.9% across the operating band. Additionally, the amplifier provides up to 18.2 dB gain with only three common-source stages.**

***Index Terms*—Power Amplifiers, Millimeter-wave, Backhaul, W-Band**

I. Introduction

TECHNOLOGICAL advances have enabled emerging applications that demand wireless links with high data rates and low latency. Millimeter-wave (mmWave) bands provide abundant spectrum for point-to-point backhaul links, making them attractive for meeting these requirements.

The 100 GHz–114 GHz range includes three spectrum allocations for fixed radio services, each offering over 2.25 GHz of continuous bandwidth [1], [2]. Its potential for high-capacity communication has been experimentally validated in [3]. However, realizing power amplifiers (PAs) that combine high output power with energy efficiency remains a key challenge—particularly when using high-yield commercial semiconductor processes.

In this work, we present a three-stage balanced PA covering the 100 GHz–114 GHz band. Implemented in a commercial 100 nm GaAs process. The design achieves a record per-stage gain of 6.1 dB among reported GaAs PAs, delivering a saturated output power of 24.1 dBm and a peak power-added efficiency above 11.9%.

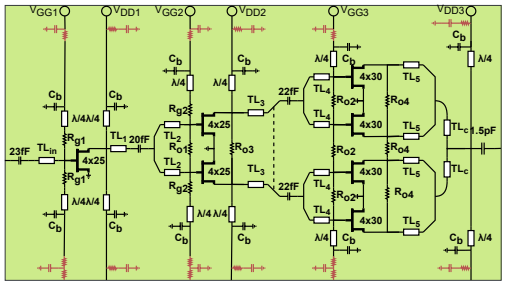
II. MMIC Design

The circuit is fabricated using the WIN Semiconductors PP10-20 pHEMT platform. The core of this technology is a 160 GHz f_{T}, 0.1 µm-gate D-mode transistor qualified for 4V operation. This platform provides two interconnect metals with air-bridge crossovers, MIM capacitors, thin-film resistors, backside metallization, and through-wafer vias.

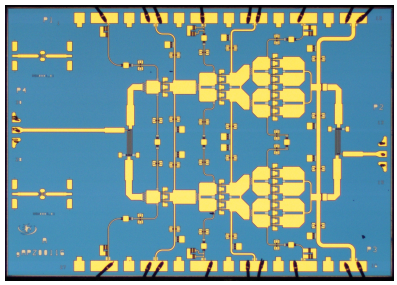
The amplifier consists of two identical branches, as shown in Fig. 1a. Each branch features three common-source stages, biased with a current density of $300\,\mathrm{mA/mm}$ for Class-AB operation. Identical 35 Ω Lange couplers are employed for input power splitting and output power combining, forming the complete MMIC PA shown in Fig. 1b. All circuit and electromagnetic (EM) simulations were performed in the Keysight ADS environment using foundry-provided transistor models.

G. Kaval and M. Gavell are with Gotmic AB, 411 33 Gothenburg, Sweden (e-mail: goksu.kaval@gotmic.se; marcus.gavell@gotmic.se).

G. Lasser and C. Fager are with Department of Microtechnology and Nanoscience, Chlmers University of Technology, 41296 Gothenburg, Sweden (e-mail: gregor.lasser@chalmers.se; christian.fager@chalmers.se).



(a)



(b)

Fig. 1. (a) Schematic of a single branch of the PA. (b) Photograph of the 3.4×2.4 mm MMIC comprising two balanced branches.

The PA branches employ $4 \times 25\,\mu\mathrm{m}$ transistors in the first and second stages, achieving a maximum available gain (MAG) of 8.1 dB at 100 GHz and 6.5 dB at 114 GHz. The output stage uses four $4 \times 30\,\mu\mathrm{m}$ transistors with an MAG of 7.6 dB at 100 GHz and 6.1 dB at 114 GHz. At 114 GHz, a single $4 \times 30\,\mu\mathrm{m}$ transistor delivers 16.7 dBm RF output power at the 1 dB compression point.

Fig. 2 presents the optimal source and load impedances for each stage. The load impedance for maximum output power, $Z_{\mathrm{L,Pout}}$, closely aligns with the simultaneous conjugate match for gain, $Z_{\mathrm{L,Gain}}$, across the frequency range. Similarly, the impedance for peak PAE, $Z_{\mathrm{L,PAE}}$, nearly overlaps with $Z_{\mathrm{L,Pout}}$ and is omitted from the figure for clarity. A similar trend is observed among the source impedances $Z_{\mathrm{S,Pout}}$, $Z_{\mathrm{S,PAE}}$, and $Z_{\mathrm{S,Gain}}$. This convergence allows for a design with minimal trade-off between gain, PAE, and output power.

The matching network implementation is illustrated in Fig. 1a. The characteristic impedances (Z_{c}) and electrical lengths (θ) of the transmission lines at the 107 GHz center frequency are reported in Table 1 in [4]. Each of the thinnest

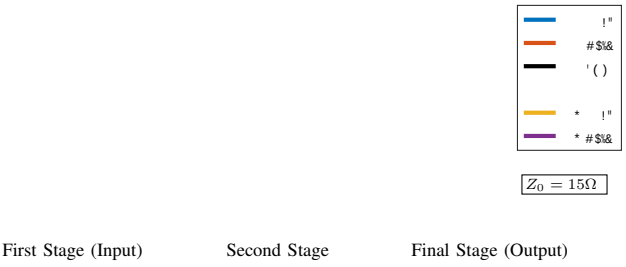
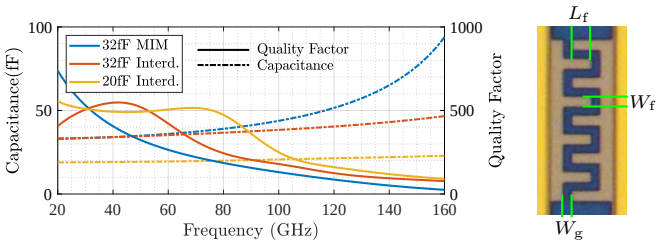


Fig. 2. Source and load termination impedances yielding maximum RF output power and small-signal gain for each amplifier stage over the 100 GHz–115 GHz range. Additionally, the simulated load impedances presented to each stage are shown. Circular markers indicate the lower edge of the frequency range.

output transmission lines ($\mathrm{TL_c}$) is rated for an RMS current of 140 mA, offering approximately a 2.8-fold margin over the maximum power delivery requirement.

The process supports MIM capacitors down to 32 fF using 10 µm × 5 µm metal plates. Lower capacitance values were realized using interdigitated single-metal fingers. Fig. 3 shows the simulated quality factor of a 20 fF interdigitated capacitor with $L_\mathrm{f} = 9\,\mu\mathrm{m}$, $W_\mathrm{f} = 3\,\mu\mathrm{m}$, $W_\mathrm{g} = 5\,\mu\mathrm{m}$, and number of fingers (NOF) $= 9$. For comparison, quality factors for 32 fF MIM and interdigitated capacitors with $\{L_\mathrm{f},\, W_\mathrm{f},\, W_\mathrm{g}\} = \{13.5,\, 5.0,\, 3.0\}\,\mu\mathrm{m}$ and NOF $= 13$ are also shown. Results indicate that interdigitated capacitors offer higher quality factors in this capacitance range.

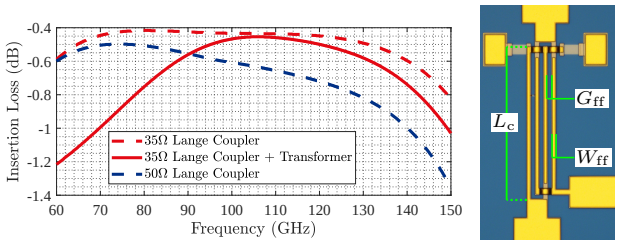


(a) (b)

Fig. 3. (a) Simulated capacitance and quality factors for various MIM and interdigitated capacitor implementations. (b) A photograph of a 9-finger, 20 fF interdigitated capacitor.

To combine the two amplifier branches, Lange couplers, as shown in Fig. 4, were employed. Simulated back-to-back insertion loss comparisons were performed for various coupler designs, all using a fixed finger length ($L_\mathrm{c} = 247\,\mu\mathrm{m}$). The Lange coupler fingers are implemented using both interconnect metal layers. Implementing a 50 Ω coupler requires a narrow finger width ($W_\mathrm{ff} = 2.7\,\mu\mathrm{m}$), while the finger gap ($G_\mathrm{ff} = 5\,\mu\mathrm{m}$) violates design rules, resulting in elevated ohmic losses—particularly at higher frequencies. In contrast, a 35 Ω coupler with $W_\mathrm{ff} = 7.5\,\mu\mathrm{m}$ and $G_\mathrm{ff} = 5.7\,\mu\mathrm{m}$ complies with layout constraints and exhibits lower insertion loss. Even when followed by a quarter-wavelength transformer for 50 Ω matching, the 35 Ω design outperforms its 50 Ω counterpart, as illustrated in Fig. 4. The simulated directivity of the final 35 Ω couplers remains approximately 15 dB ± 1 dB across the frequency range.

The matching networks (MNs) transform frequency-dependent complex impedances—specifically, the load pre-



(a) (b)

Fig. 4. (a) EM simulated back to back insertion loss of Lange couplers with different configurations. (b) Photograph of the Lange coupler.

sented by one stage into the optimal source impedance required by the next, which is also frequency-dependent and complex known as double matching in the literature [5]. Modern circuit simulators support frequency-dependent complex terminations at circuit ports, enabling straightforward evaluation of MN performance, especially when near-conjugate matching conditions are targeted. Fig. 5 shows the loss introduced by each MN, expressed as its transducer gain (G_TU), when the first port is terminated with $Z^*_{\mathrm{L,Gain}}$ (or 50 Ω for the input MN) and the second with $Z^*_{\mathrm{S,Gain}}$ (or 50 Ω for the output MN). For MNs employing Lange couplers, G_TU is defined from the combined interface to one of the balanced branches, with the other branch identically terminated. Under near-simultaneous conjugate matching conditions, the overall amplifier gain can be approximated as the sum of each stage's MAG and the G_TU of MNs. The figure shows that G_TU decreases at lower frequencies and is maximized at higher frequencies to compensate for the downward-sloping MAG of the transistors, thereby flattening the overall gain response. The load presented to each stage are shown in Fig. 2 as $Z_{\mathrm{L,Imp}}$.

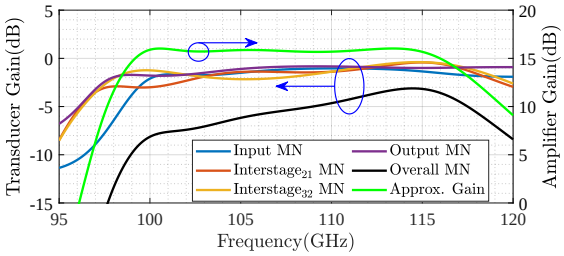


Fig. 5. Transducer gain of the matching networks and the approximated overall amplifier gain. $\mathrm{Interstage}_{ij}$ denotes the matching network between stages i and j.

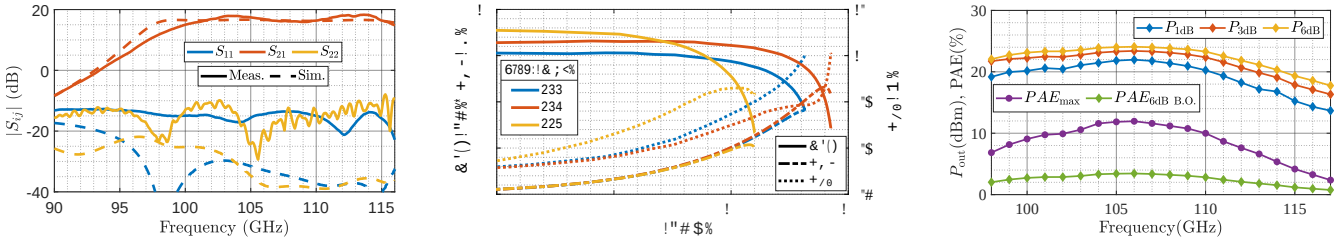
Bias lines for each stage were implemented using a quarter-wavelength transmission line followed by a capacitor (C_b). The capacitor, C_b, was chosen as 175 fF to resonate with the ground via inductance at the operating frequency band, thereby achieving an RF-optimal short. The branch design was completed with bypass capacitors, as highlighted in red in Fig. 1a.

The transistors in the design are unconditionally stable over the operating frequency range, as verified by the Rollet stability criterion [6] and geometrically derived stability conditions [7]. The absence of right half-plane poles at every circuit interface was confirmed using Nyquist contours [8]. Based on these analyses, series 12 Ω thin-film resistors ($R_{\mathrm{g1,2}}$) were added to the gate bias networks, and decoupling capacitors

TABLE I
COMPARISON WITH OTHER WORKS IN THE LITERATURE OPERATING IN OR CLOSE TO THE TARGET FREQUENCY BAND

Reference	Frequency(GHz)	Process	Gain(dB)	$P_{\mathrm{dc,q}}$(W)	P_{sat}(dBm)	PAE (%)	Num. Stage	Size(mm × mm)	Gain Per Stage (dB)
[9]	92-102	65 nm CMOS	32.5	-	32.1	15.0	4	2.9×1.5	8.1
[10]	110-150	250 nm InP	29.4	3.46	23.2-24.0	5.8-7.0	5	2.1×1.0	5.9
[11]	102-118	0.14 µm GaN	19.7-20.1	-	28.0-29.0	8.0	6	3.3×1.9	3.9-4.2
[12]	65-125	50 nm InGaAs	16.8	2.15	22.5	7.6	4 (Stacked)	1.3×2.8	4.2
[13]	100-113	0.1 µm GaAs	4.0-7.0	-	22.0-24.0	-	2.0	2.3×1.6	2-3.5
[14]	90-112	0.1 µm GaAs	22.0	-	15.2	3.5	3 (Cascode)	1.5×0.8	7.3
[15]	85-116	0.1 µm GaAs	20.5	-	22.5	4.0	5	2.8×3.0	4.1
[16]	92-102	0.1 µm GaAs	27.0	3.00	27.0	12.5	5	3.0×3.0	5.4
This Work	100-114	0.1 µmGaAs	15.2-18.2	1.87	20.3-24.1	11.9-5.3	3	2.6×2.4 *	5.1-6.1

* The long transmission line at the input used to align the PA with the reticle plan was de-embedded to accurately report the PA size.
** $P_{\mathrm{dc,q}}$ denotes the quiescent DC power consumption.



(a) (b) (c)

Fig. 6. Measured results for the PA: (a) Small-signal performance in comparison with simulated results, (b) measured gain and PAE versus RF output power at center and edge frequencies, and (c) output compression points and PAE versus operating frequency.

(highlighted in red) were damped with 10 Ω thin-film resistors to reduce their quality factor. Additionally, 30 Ω thin-film resistors ($R_{\mathrm{o1,2}}$) and 50 Ω resistors ($R_{\mathrm{o3,4}}$) were placed between the balanced transistors of each branch to suppress parasitic odd-mode excitations. The resistor values were tuned until Nyquist contours for each node confirmed stability.

III. Measurement Results and Discussion

The manufactured MMIC is mounted on a test PCB using conductive epoxy. DC pads are connected to 120 pF single-layer capacitors and then to the designated PCB interfaces via wire bonds. RF probes access the RF ports. A vector network analyzer with frequency extenders, calibrated using substrate standards, is used for small-signal measurements. For power sweeps, custom automatic level-controlled sources are employed, and RF power calibrations and measurements are performed using an Erickson PM5B power meter.

Fig. 6a shows that the simulated and measured gains are in good agreement, with the target frequency falling within the 3 dB bandwidth. The input and output reflection coefficients remain below 10 dB across the frequency range, owing to the balanced design. However, discrepancies in S_{11} and S_{22} between simulation and measurement, suggest that the transistor models could be further refined and directivity of the couplers can be improved. Fig. 6b illustrates that the PA compresses smoothly without any signs of parametric oscillations at both the center and edge frequencies. Additionally, Fig. 6c presents the output compression points ($P_{1\mathrm{dB}}$, $P_{3\mathrm{dB}}$, and $P_{6\mathrm{dB}}$) across the frequency range, along with the maximum power-added efficiency (PAE_{max}) and the PAE at 6 dB back-off from $P_{6\mathrm{dB}}$.

Table I summarizes selected MMIC PAs operating near the target frequency range. CMOS [17]–[19] and SiGe [20], [21] PAs typically deliver lower RF output power than III–V technologies, with the exception of [9], where 128 CMOS PAs were successfully power-combined. InP-based PAs [10], [22] generally offer wide bandwidth and higher output power at elevated frequencies [23]; however, their commercial adoption is limited by the brittle nature of InP substrates. Owing to its wide bandgap, GaN achieves the highest power levels among all technologies [11], [24], [25]. Nonetheless, when considering volume, cost, and yield, GaAs remains a highly favorable and practical choice.

This PA demonstrates one of the highest per-stage gains among GaAs PAs, enabled by low-loss matching networks as discussed in Section 2 and the mature technology developed by WIN Semiconductors. The high gain per stage allows the output stage to employ 2.4 times the transistor periphery of the preceding driver stage, whereas most prior works rely on equal peripheries for the driver and output stages. This contributes to the highest reported PAE among GaAs implementations beyond 100 GHz. While [14] employs cascode stages to enhance gain and [16] reports higher P_{sat} in a slightly lower frequency band, this work still achieves competitive output power, gain, and energy efficiency. The bandwidth is limited by the low input and output impedances of the transistors, which could be improved by realizing devices with higher output impedance, as demonstrated in [12].

IV. Conclusion

We present an MMIC PA operating from 100 GHz to 114 GHz, fabricated using a commercial 0.1 µm GaAs process. Low-loss matching network implementations are introduced, and losses from each network are reported. The amplifier achieves 15.2 dB–18.2 dB gain, with a record per-stage gain above 6 dB. The saturated output power reaches 24.1 dBm, with PAE ranging from 11.9% to 5.3%. This represents the highest reported PAE among GaAs PAs operating beyond 100 GHz, demonstrating the design's competitive performance.

Acknowledgments

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