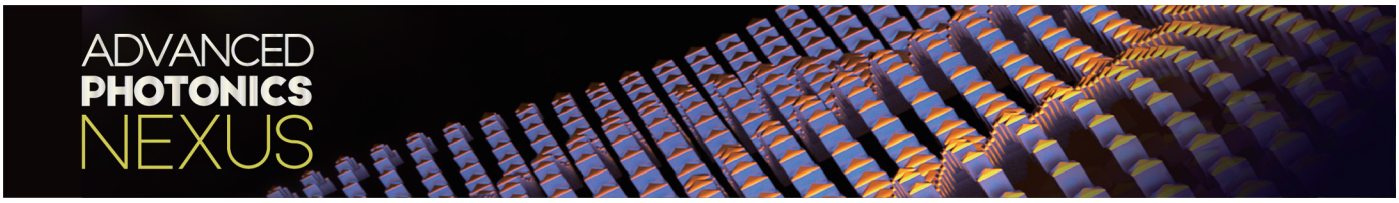
Homodyne coherent inter-satellite communications with IM/DD comparable DSP

Research Article



Homodyne coherent inter-satellite communications with IM/DD comparable DSP

Junda Chen,[a,b] Kun Li,[a] Tianjin Mei,[a] Mingming Zhang,[a] Zihe Hu,[a] Jiajun Zhou,[c] Chen Liu,[a,*] Ming Tang,[a,*] and Peter A. Andrekson[b]

[a]Huazhong University of Science and Technology, School of Optical and Electronic Information, Wuhan National Laboratory for Optoelectronics & Next Generation Internet Access National Engineering Laboratory & Hubei Optics Valley Laboratory, Wuhan, China
[b]Chalmers University of Technology, Department of Microtechnology and Nanoscience, Gothenburg, Sweden
[c]JFS Laboratory, Wuhan, China

Abstract. The rapid development of low earth orbit (LEO) satellite communication networks imposes stringent bandwidth, cost, and power consumption requirements. Conventional intradyne detection (ID) architectures struggle with high Doppler frequency shifts (DFSs), necessitating excessive sampling rates and complex digital signal processing (DSP), resulting in elevated power consumption. This study proposes an inter-satellite polarization division multiplexing self-homodyne detection (PDM-SHD) architecture that compensates for DFSs in the optical domain by co-transmitting a polarization-orthogonal carrier light. The proposed architecture could achieve Nyquist sampling and half-quantization noise, leading to a 53.9% reduction in analog-to-digital converter power consumption under 40 Gbps 16-QAM transmission with a 16 dB signal-to-noise ratio. By demodulating I/Q axis signals independently with real-valued single-input single-output (SISO) processing, it requires only about 15% DSP complexity and achieves intensity-modulation and direct-detection comparable. SISO processing also has the potential to transmit I and Q components from separate devices or satellites, enabling a flexible satellite communication network. The results demonstrate that the proposed architecture achieves detection sensitivities of −40.8 dBm for 80 Gbps quadrature phase-shift keying transmission and −33.0 dBm for 160 Gbps 16-QAM transmission with Nyquist sampling, whereas the ID architecture can hardly work. The proposed architecture effectively balances satellite power constraints with DSP computational demands for high-speed mega-constellation communications.

Keywords: inter-satellite optical communications; self-homodyne detection; digital signal processing; low power consumption.

Received Aug. 20, 2025; accepted for publication Sep. 9, 2025; published online Oct. 2, 2025.

[DOI: 10.1117/1.APN.4.5.056010]

1 Introduction

Satellite communication networks, with their extensive global coverage, are becoming indispensable in telecommunications, emergency rescue, navigation, remote sensing, and other critical fields.[1] The deployment of low Earth orbit (LEO) satellite constellations, combined with free-space optical inter-satellite links (OISLs), has emerged as the dominant paradigm for achieving seamless connectivity.[2,3] Although advanced intensity modulation and direct detection (IM/DD) systems show high potential in terms of spectral efficiency and computational complexity,[4,5] the high-power local oscillator (LO) in coherent detection enables high sensitivity detection and precise digital filtering.[6,7] As LEO constellations evolve into a pivotal component of sixth-generation (6G) wireless systems,[1] the adoption of high-order modulation formats—such as quadrature phase-shift keying (QPSK) and 16-quadrature amplitude modulation (16-QAM)—alongside coherent detection, is widely regarded as the optimal pathway for advancing next-generation satellite communications.[8,9]

The limited orbital altitude restricts the coverage area of individual LEO satellites, necessitating ultra-large-scale constellations for global service continuity. For instance, the Starlink project plans to deploy 42,000 satellites in its Gen2 system,[10] imposing stringent constraints on per-satellite cost, weight,

*Address all correspondence to Chen Liu, liuchen@hust.edu.cn; Ming Tang, tangming@mail.hust.edu.cn

and power consumption. The inter-satellite communication terminals are critical to meeting these specifications, with each satellite typically requiring three to four terminals to maintain continuous connectivity. Within each terminal, the modem subsystem constitutes the dominant power-consuming component, accounting for up to 40 W of the 100 W total power budget.[11] This subsystem is primarily comprised of analog-to-digital converters (ADCs) and digital signal processing (DSP) chips. Although state-of-the-art coherent transmitters with 7 nm application-specific integrated circuit (ASIC) chips could achieve high-speed communications at reduced power,[12] their inherent algorithmic redundancy presents significant opportunities for further power optimization. Practically, engineering realities dictate that to support each 100 W increase in power consumption, satellites must accommodate 2 kg of batteries and 0.45 m^2 of solar panels,[13,14] thereby incurring a substantial increase in launch costs exceeding $10,000.[15] These constraints underscore the urgent need for low-power consumption OISL technologies.

As the theoretical minimal alias-free sampling rate, Nyquist sampling has long been a goal pursued by researchers to reduce ADC power consumption and cost.[16] In conventional intradyne detection (ID) architectures, the frequency offset between the separately generated LO and signal forces the ADC sampling rate to exceed the sum of the symbol rate and frequency offset to avoid aliasing.[9] Appendix A analyzes the Doppler frequency shift (DFS) of a satellite network[17] as a case study (with a 580 km height and composed of 6 orbital planes with 58 satellites each), demonstrating that the DFS varies gradually within a 7 GHz bandwidth, completing a full cycle roughly every 43 min. Consequently, the substantial DFS in LEO satellite communications renders near-Nyquist sampling unfeasible with conventional ID architecture.[8] For instance, a 10 Gbaud transmission in this network would require sampling rates of >17 GSa/s, causing ADC power consumption to surge by 70%. This fundamental conflict between the DFS tolerance and power efficiency severely challenges the viability of conventional ID architecture designs in LEO applications.

Achieving Nyquist sampling necessitates precise LO to signal frequency alignment. Optical phase-locked loops (OPLLs) offer a potential solution by enabling real-time LO tuning,[18,19] but their implementation demands that the residual error of the PLL be significantly less than the minimum phase angle of the constellation diagram. This stringent requirement introduces considerable precision and complexity into circuit design. Differential phase-shift keying (DPSK) mitigates phase mismatch by distributing the damage uniformly across symbols through delayed differential detection and achieves IM/DD comparable to DSP.[20] This allows phase mismatch to be treated as negligible additive noise. However, this differential processing simultaneously induces the accumulation of untreated noise, degrading detection sensitivity by over 3 dB. Self-homodyne detection (SHD) architectures offer an alternative approach by co-transmitting the LO and signal, and consequently mitigating the impact of frequency impairments, including DFSs, in the optical domain.[21] Owing to these inherent passive frequency impairment compensation benefits, SHD architectures have been extensively utilized in power-consumption-sensitive applications.[22,23] Although Nyquist sampling fiber communication employing SHD architectures has been realized,[24] their direct application in OISLs is hindered by the substantial link losses, which preclude the direct utilization of the co-transmitted carrier (LO) for detection at the receiver.[25] To overcome this limitation, optical injection locking (OIL) was employed at the receiver to reconstruct the pilot.[26,27] This reconstructed pilot is then governed by a PLL to maintain phase locking, an approach termed optical injection PLL (OIPLL). Nevertheless, the feedback signal in OIPLL architectures is dependent on the Q-channel signal from the 90 deg hybrid, intrinsically limiting its application to binary frequency-shift keying (BPSK) modulation formats. Achieving a balance between high-speed communication, high-order modulation, and low power consumption remains a significant challenge in existing works.

To address the exponentially growing communication demands in LEO mega-constellations, we recently experimentally demonstrated a polarization division multiplexing SHD (PDM-SHD) architecture for the inter-satellite communications using low-complexity DSP and Nyquist sampling.[28] In this paper, the equalization algorithm is further simplified from complex-valued multiple-input multiple-output (MIMO) to a real-valued single-input single-output (SISO) scheme, achieving only 15% complexity compared with the conventional ID architecture. By transmitting the signal and carrier in orthogonal polarization states, the DFS impairment of OISL is passively compensated in the optical domain, and the following key advantages are achieved: (1) achieving Nyquist sampling as well as mitigating effective number of bits (ENOB) penalty; (2) suppressing the time-varying channel response of OISL, allowing for the application of a constant tap equalizer; (3) decoupling the correlation of I/Q components to enable real-valued DSP with IM/DD comparable complexity. Beyond these core advantages, this architecture potentially enables independent I/Q signal transmission with asynchronous clocks, heterogeneous rates, or distinct modulation formats. This constitutes a systemic resolution to the critical trade-off between satellite power constraints and DSP computational demands in high-speed mega-constellation communications.

2 PDM-SHD Architecture Using IM/DD Comparable DSP

In coherent optical communication systems, power consumption optimization presents critical challenges as ADCs and DSP modules collectively account for over 70% of the total power budget of reconfigurable modems. It is well established that conventional ID architecture utilizes an independent LO, typically an external cavity laser (ECL), to extract phase and intensity information. By contrast, the SHD scheme transmits a pilot carrier through the orthogonal polarization state of the signal, as shown in Fig. 1(a). A carrier recovery module compensates for power loss induced by the free-space optical path. In OISLs, orthogonal circular polarizations can be used to transmit the signal and carrier,[29] which ensures that relative satellite rotation does not alter the polarization angle. Combined with the vacuum link, which prevents polarization degradation, the receiver can then separate signal and carrier using a simple polarization beam splitter (PBS).

The structural divergence leads to distinct impairment compensation requirements. ID architecture necessitates comprehensive DSP-based compensation for dynamic channel impairments, especially for DFSs and phase noise due to its fixed-wavelength LO implementation. Conversely, the SHD architecture passively mitigates these impairments through the co-transmission of signal and pilot components. As both components experience identical channel conditions, their phase

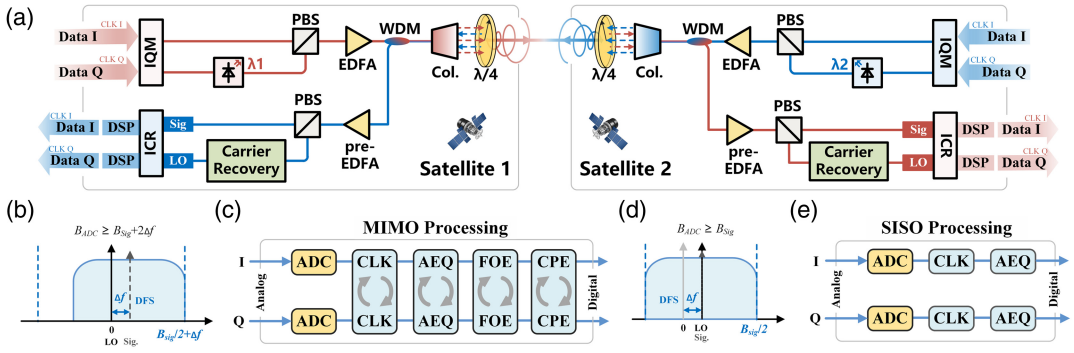


Fig. 1 (a) PDM-SHD diagram for the bi-directional optical inter-satellite communication link; (b) ID architecture ADC bandwidth limitation; (c) ID architecture Rx chip workflows; (d) PDM-SHD architecture ADC bandwidth limitation; (e) PDM-SHD architecture Rx chip workflows.

noise and DFSs compensate themselves in the optical domain before detection. This optical-domain impairment compensation fundamentally decouples the I/Q coordinate dependencies before DSP. The simplification enables two paradigm-shifting advancements: (1) realization of Nyquist (1-sample per symbol) sampling and (2) enabling real-valued SISO-DSP algorithms. Figures 1(b)–1(d) illustrate the comparative frequency domain signal spectrum and on-chip workflows between conventional ID and SHD coherent schemes. A detailed comparative analysis of ASIC chip optimization between these architectures will follow.

2.1 Nyquist Sampling ADCs

Under identical ADC architectures and manufacturing processes, the power consumption model of an ADC follows $P_{\mathrm{ADC}} = \mathrm{FOM}_W \cdot f_s \cdot 2^b$, governed by linear proportionality to sampling rate f_s and exponential dependence on number of bits b, where Walden's figure of merit (FOM) quantifies ADC power efficiency.[30] The SHD structure inherently enables Nyquist sampling communication while simultaneously relaxing ENOB penalty compared with ID architectures.

According to the Nyquist–Shannon theorem, alias-free signal acquisition mandates a sampling rate greater than twice the signal bandwidth. As illustrated in Figs. 1(b) and 1(d), the presence of DFS (Δf) between signal and LO necessitates sampling rates exceeding $2\Delta f$ to fully capture spectral information. Conversely, the SHD architecture passively compensates Doppler impairments through co-transmission of signal and pilot carriers, as both components experience identical channel-induced DFSs. This passive compensation mechanism at the coherent detection stage enables the realization of high-speed optical communication systems operating at the theoretical minimum alias-free sampling rate of 1 sample per symbol (Nyquist sampling).

Subfigures within Fig. 2 compare constellation characteristics of ID versus SHD coherent receivers. ID architecture exhibits rapid constellation rotation due to uncompensated DFS between signal and LO, whereas SHD maintains stationary points. Assuming uniform signal distribution across quantization intervals, DFS-induced rotation in ID systems amplifies maximum I/Q component amplitudes by a factor of $\sqrt{2}$ relative to SHD. The quantization noise equivalent model gives $P_q = \frac{1}{12} \cdot \frac{V_{\mathrm{FS}}^2}{4^{\mathrm{ENOB}}}$, where P_q denotes the quantization noise and V_{FS} is

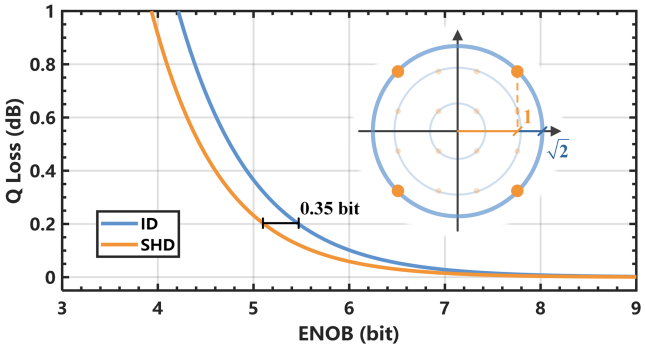


Fig. 2 Simulated Q-factor penalty versus ENOB for ID and SHD architectures under a 16 dB signal-to-noise ratio (SNR).

the full-scale signal amplitude.[31] Given equals the maximum amplitude at sampling points, SHD architecture reduces system quantization noise by 50%, thereby providing ENOB design margin. Figure 2 quantifies the Q-factor penalty versus ENOB for both architectures at a simulated 16 dB SNR. The 0.35-bit quantization noise equivalence indicates ID systems require 5.45-bit resolution to match 5.10-bit SHD architecture performance under 0.2 dB Q factor loss, with $Q(\mathrm{dB}) = 20\log[\sqrt{2}\,\mathrm{erfc}(2 \cdot \mathrm{BER})]$, where erfc() is the Gauss error function and BER is the bit error rate. It should be noted that this result specifically reflects the ENOB design margin for SHD architecture under 16-QAM modulation at a 16 dB SNR. Altering modulation format, SNR, or Q-loss threshold will modify the ENOB design margin.

Considering a ±3.5 GHz DFS scenario (as calculated in Appendix A) in a 10 GBaud 16-QAM modulated system, this fundamental difference imposes critical implementation constraints. ID architectures necessitate ≥17 GSa/s sampling rate to satisfy Nyquist criteria for DFS-containing signals, whereas SHD systems can achieve Nyquist sampling at 10 GSa/s. Even when both architectures are operating at their minimum sampling rates, the combined effects of reduced sampling rate (10 versus 17 GSa/s) and half-quantification noise enable homodyne receivers to achieve $\frac{10}{17} \times \frac{2^{5.10}}{2^{5.45}} \approx 46.1\%$ remaining ADC power consumption compared with the ID architecture.

2.2 IM/DD Comparable SISO DSP

DSP represents another major power consumption component in the receiver chips. As shown in Fig. 1(c), signal impairment compensation requires multiple complex-domain algorithms in conventional ID architectures: (a) clock recovery, (b) adaptive equalization, (c) DFS compensation, and (d) phase noise mitigation. Crucially, the sequential placement of DFS and phase noise compensation at the DSP chain's terminal stage—mandated by their need for minimally distorted signals—forces all preceding algorithms to operate on phase-impaired data, necessitating complex field computations through the entire workflow. By contrast, SHD architecture fundamentally addresses this limitation by establishing a fixed phase relationship between the signal and carrier. This facilitates two critical simplifications: (a) decomposition of complex field operations into dual real-valued signal processing, and (b) elimination of the DFS and phase noise compensation DSP modules. Consequently, as shown in Fig. 1(e), the optimized DSP workflow retains only two essential algorithms: Nyquist sampling clock recovery and real-valued SISO equalization. It should also be noted that DSP power consumption also scales linearly with sampling rates, underscoring the direct power-saving benefits of Nyquist sampling.

2.2.1 Nyquist sampling recovery

Nyquist sampled systems impose stringent requirements on transmitter-side pulse shaping, necessitating the use of minimal roll-off factor ($\alpha \to 0$) filters to suppress spectral spreading and prevent aliasing artifacts. This introduces a fundamental incompatibility with the Gardner clock recovery algorithm,[32] the predominant algorithm in ID fiber-optic systems. The Gardner algorithm depends on analyzing waveform transitions between adjacent symbols, requiring (a) sufficient excess bandwidth (typically $\alpha \geq 0.15$) to preserve waveform edges and (b) 2-SPS sampling to capture transition details. These conditions render the Gardner algorithm inherently unsuitable for the Nyquist sampled systems with ultra-low roll-off factors ($\alpha \leq 0.05$).

By contrast, the Mueller–Muller (M–M) algorithm offers an alternative by deriving error estimates from inter-symbol interference (ISI) analysis.[33] Its error function models each symbol as an impulse response, quantifying ISI leakage between adjacent symbols, written as

$$\begin{cases} e_I(k) = \text{sign}[I(k)] \cdot I(k-1) - \text{sign}[I(k-1)] \cdot I(k) \\ e_Q(k) = \text{sign}[Q(k)] \cdot Q(k-1) - \text{sign}[Q(k-1)] \cdot Q(k) \end{cases}, \quad (1)$$

where $e_I(k)$ and $e_Q(k)$ are the cost function results for the kth symbol and sign() is the sign operation. Notably, this approach exhibits improved performance with decreasing roll-off factors, rendering it well-suited for Nyquist sampled systems. Comparisons of S-curve characteristics for both algorithms, under varying α with QPSK modulation, are presented in Fig. 3(a). The results show that the M–M algorithm achieves optimal timing sensitivity at $\alpha = 0.01$, whereas the Gardner algorithm fails to converge under identical conditions.

Equation (1) also demonstrates that the error functions of I and Q components in the Muller clock recovery algorithm are independently computed without overlapping. This separation gives the ability to conduct timing recovery for entirely unrelated I and Q signals without mutual interference. However, it renders the M–M clock recovery sensitive to phase rotations. As illustrated in Fig. 3(b), significant S-curve distortion arises in the presence of DFS or phase noise. This limitation can be easily overcome in SHD architectures, where optical-domain compensation of frequency and phase impairments establishes phase-stable conditions that satisfy the M–M algorithm's operational requirements. This advancement is a key enabler for adopting the M–M algorithm in next-generation coherent OISLs.

2.2.2 Real-valued & constant coefficient SISO equalizer

In contrast to the dynamically varying polarization states in fiber-optic communications, inter-satellite communications utilize circular polarization to eliminate the need for adaptive polarization adjustment.[29] However, residual ISI remains due to hardware imperfections and bandwidth constraints, necessitating equalization algorithms to compensate. The unique orbital dynamics of satellite communication result in quasi-static channel conditions: once established, satellite links maintain stable connections with optical-domain DFS compensation, eliminating the only time-varying impairments. This stability

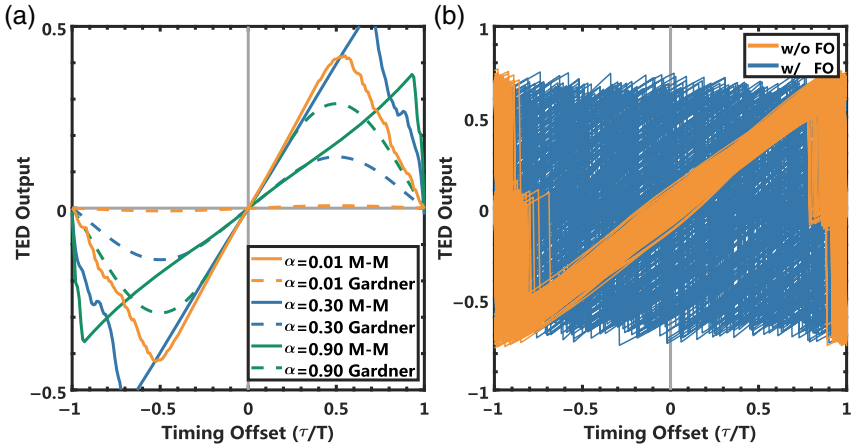


Fig. 3 Under QPSK modulation (a) S-curve characteristics for the Gardner and M–M clock recovery algorithms, under varying α; (b) S-curve characteristics for the M–M clock recovery algorithm, with or without FO.

enables a hybrid equalization strategy. During initial link setup, feed-forward equalizers, such as decision-directed (DD) equalizers, are employed to adaptively optimize the finite impulse response (FIR) coefficients of the ISI compensation filter. Subsequently, the feedback loop can be disconnected, and the optimized FIR filter is used until link termination, realizing the constant tap equalizer.

In ID architectures, rapid phase rotation requires simultaneous complex field equalization on both I/Q components, necessitating $4N$ real multiplications per FIR tap. Conversely, the I/Q decoupling in SHD architecture allows for independent I/Q real-valued equalization, reducing the computational demand to $2N$ real multiplications per tap. This dual advantage—constant tap and SISO equalization positions SHD architectures as the optimal solution for power-constrained spaceborne systems.

2.3 Complexity Analysis

The proposed SISO DSP architecture for the SHD system is fundamentally simplified through its independent real-domain computation of I and Q components. This approach enables independent demodulation of I and Q signals, capitalizing on the inherent decorrelation between orthogonal axes in SHD systems. By decoupling the I and Q axes in coherent detection, the architecture effectively transforms the process into two independent direct detection processes. As a result, established IM/DD DSP algorithms, including M–M clock recovery[34] and DD equalization,[35] are directly applicable to SHD systems. On the other hand, this design also supports the transmission of independent signals on the I and Q axes, potentially allowing signals with different rates, SNRs, and modulation formats from separate devices. This capability is well-articulated and highlights the architecture's flexibility and efficiency.

Under the Nyquist sampling assumption, Tables 1 and 2 (with detailed derivations in Appendix C) quantify the computational requirements for ID, SHD, and IM/DD architectures using fundamental algorithms with baseline optimizations. Considering an analysis based on 25-tap equalizer implementation, it reveals that conventional DSP requires 377 multiplications and 310 additions per symbol. By contrast, the proposed constant tap SISO DSP for the SHD architecture reduces computational complexity to 52 multiplications and 51 additions per symbol. This results in only 13.8% multiplications and 16.3% additions required for the SHD architecture compared with ID architecture. Notably, manufacturer-specific optimizations are excluded from this comparative framework to account for implementation heterogeneity.

3 Experimental Setup

Figure 4 illustrates the experimental configuration and DSP flow of the proposed PDM-SHD architecture utilizing constant tap SISO DSP. The transmitter employs a tunable ECL as the light source, with adjustable simulated DFSs. A polarization-maintaining 95:5 coupler divides the light into signal and carrier paths. The signal path uses a 60 GHz integrated IQ modulator, driven by a 90 GSa/s arbitrary waveform generator (AWG), to modulate a single-polarization signal at 10/20/40 GBaud with QPSK or 16-QAM formats. The carrier path incorporates a polarization-maintaining variable optical attenuator (PM-VOA) to precisely control CSPR according to the signal power. After recombination via a polarization beam combiner (PBC), the composite signal is amplified to 20 dBm using a single-mode erbium-doped fiber amplifier (EDFA).

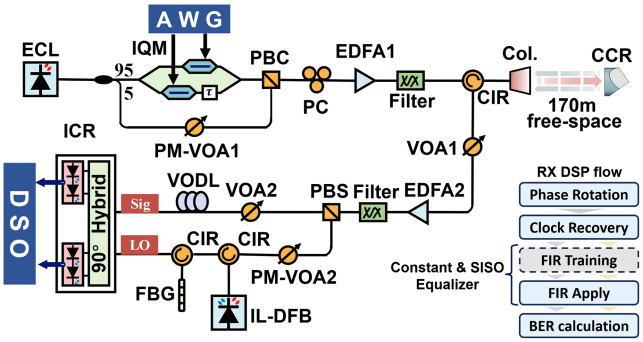


Fig. 4 Experimental diagram of the proposed PDM-SHD system and corresponding DSP flow.

Table 1 Real multiplier usage comparison for ID and SHD communication structures.

	Clock recovery	D-D equalization	DFS compensation	PN compensation	Total
ID	4	Adaptive: $14N$	13	10	Adaptive: $27+14N$
		Constant: $4N$			Constant: $27+4N$
SHD IM/DD	2	Adaptive: $10N$	N/A	N/A	Adaptive: $2+10N$
		Constant: $2N$			Constant: $2+2N$

Table 2 Real adder usage comparison for ID and SHD communication structures.

	Clock recovery	D-D equalization	DFS compensation	PN compensation	Total
ID	6	Adaptive: $12N$-1	4	4	Adaptive: $10+12N$
		Constant: $4N$-1			Constant: $10+4N$
SHD IM/DD	2	Adaptive: $8N$-1	N/A	N/A	Adaptive: $2+8N$
		Constant: $2N$-1			Constant: $1+2N$

The inter-satellite path is emulated with a 170 m free-space optical (FSO) link and a programmable VOA. The FSO link consists of a fiber circulator, a collimator, and a corner cube retroreflector (CCR) under hallway conditions. The optical power received is ∼8 dBm, with a programmable VOA simulating inter-satellite attenuation. This transmit-receive co-aperture setup serves laboratory verification simplicity, whereas actual OISLs normally employ separate antennas to avoid crosstalk from circulator isolation limitations. A pre-EDFA then amplifies the signal along with a 0.6 nm filter to suppress amplified spontaneous emission (ASE) noise. A polarization controller (PC) compensates for polarization rotation induced by the pre-EDFA and interconnecting single-mode fibers, which is unnecessary in actual OISLs because the circularly polarized vacuum transmission will maintain inherent polarization stability.

Following amplification, a PBS separates the carrier and signal components. The carrier recovery subsystem employs an innovative optical injection-locking architecture using an isolator-free distributed feedback (DFB) laser,[36,37] stabilized with an input power of −11 dBm and an output power of 13 dBm. This master-slave phase synchronization operates via frequency pulling: when the master laser's (carrier pilot) emission frequency falls within the capture range of the injection locking laser's (IL-DFB) free-running frequency, it achieves carrier reconstruction. A 9 GHz fiber Bragg grating (FBG) provides fine filtering for LO light for its limited bandwidth requirement. Optical-domain DFS compensation requires high correlation between signal and carrier, achieved through similar optical path lengths. A variable optical delay line (VODL) ensures path length synchronization with <10 cm precision, compensating for differential propagation delays between signal and LO paths. The SHD detection chain includes a 40 GHz integrated coherent receiver (ICR) and a digital storage oscilloscope (DSO), configured for symbol-synchronous sampling at programmable rates (10/20/40 GSa/s). To facilitate direct performance comparison with conventional ID architectures, the IL-DFB can be replaced by a duplicate ECL, selectively activated to realize comparison between ID and SHD architectures.

In the transmitter DSP, a raised cosine (RC) filter with a 0.01 roll-off factor is implemented to mitigate signal aliasing artifacts. The receiver DSP, constrained by the limitation of Nyquist sampling, precludes digital filtering implementations. In practice, a slight phase change arises between the signal and carrier paths due to fiber-induced mechanical vibrations and receiver fiber length mismatch (as detailed in Appendix B). For laboratory validation, a global phase rotation is applied to each captured signal segment (20 μs duration) prior to DSP processing to compensate for these phase changes. The timing recovery algorithms for ID and SHD architectures are the Gardner and M–M algorithms, respectively, with cubic Lagrange interpolation for data resampling, whereas the equalization algorithm for both is DD equalization.[38] Subsequent performance evaluation utilizes our proposed DSP framework, comparing: (1) conventional MIMO versus SISO signal processing implementations; (2) constant versus adaptive coefficient equalization strategies; and (3) SHD versus ID algorithms.

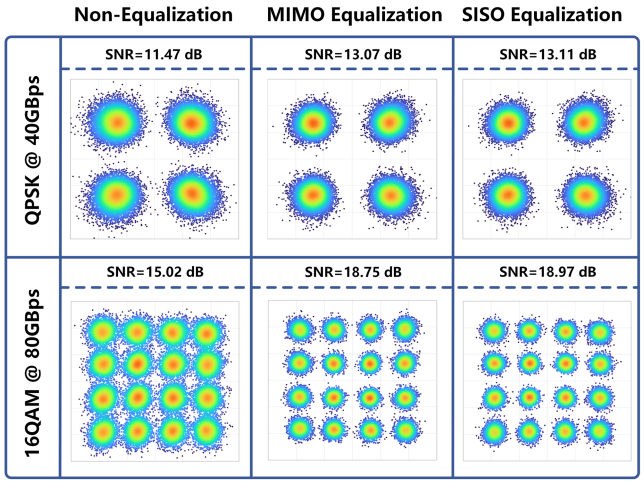


Fig. 5. Constellation diagrams and corresponding SNR metrics for 40 Gbps QPSK (–37.8 dBm) and 80 Gbps 16-QAM (–29.8 dBm) signals, with no equalization, complex equalization, and real equalization.

4 Results and Discussion

Under PDM-SHD architecture, Fig. 5 presents constellation diagrams and corresponding SNR for 40 Gbps QPSK and 80 Gbps 16-QAM signals under optimal processing conditions (including sufficient ENOB, extended number of equalization taps, and optimized clock recovery), with non-equalization, conventional MIMO equalization, and proposed SISO equalization, respectively. At received powers of −37.8 dBm (QPSK) and −29.8 dBm (16-QAM), the equalization process yields SNR improvements of about 1.6 and 3.9 dB, respectively. This divergence arises from the higher SNR requirement of the 16-QAM format. The fundamental difference between SISO and MIMO equalization lies in their impairment compensation mechanisms. As shown in the eye diagrams in Fig. 6, SISO equalization

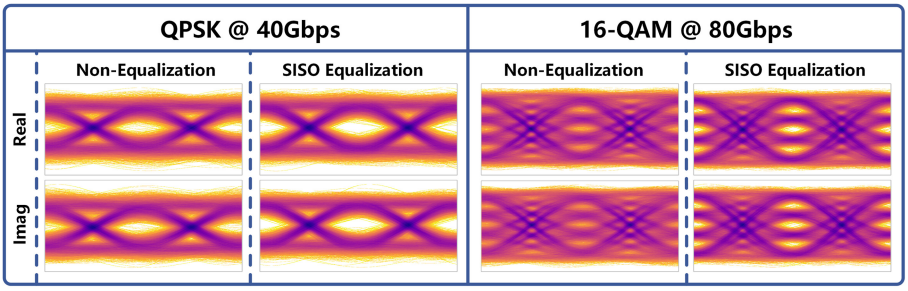


Fig. 6 Pre-equalization and post-equalization eye diagrams for 40 Gbps QPSK (–37.8 dBm) and 80 Gbps 16-QAM (–29.8 dBm) signals using a SISO equalizer.

processes the I and Q axes independently, whereas MIMO equalization leverages the joint optical field magnitude $E = \sqrt{I^2 + Q^2}$, for unified compensation. Inevitable system asymmetries in practical manufacturing could include axis-specific impairments because of the unequal gain or bandwidth in transimpedance amplifiers (TIAs), data converters (ADCs/DACs), or any I/Q components. These asymmetries lead to slight differences in I/Q frequency response, resulting in improved performance when the I and Q paths are processed with independent equalizers. Consequently, measurable SNR differences of 0.04 dB (QPSK) and 0.22 dB (16-QAM) are observed between the two equalization methods.

As discussed in Tables 1 and 2, the number of taps for equalizer significantly influences the DSP complexity. Figure 7 illustrates the relationship between tap requirements and Q-factor degradation for both SISO and MIMO equalizers across QPSK (−43.4 dBm) and 16-QAM (−36.8 dBm) systems under varying symbol rates. The results show that higher symbol rates require progressively more taps to compensate for equivalent ISI durations: QPSK systems require 16, 19, and 28 taps at 10, 20, and 40 Gbaud, respectively, whereas 16-QAM systems require 28, 45, and 92 taps under the same 0.1 dB Q-factor penalty threshold. The increase for 16-QAM arises from the greater sensitivity to residual linear impairments of advanced modulation formats compared with QPSK. In the experiment, both equalizers are based on the adaptive step-size DD equalizer, which introduces penalty jump as the number of taps increases. Increased tap numbers yield diminished residue error on the cost function of the equalizer, which subsequently reduces adaptation step sizes, resulting in abrupt Q-penalty transitions, especially for the 16-QAM curves. The result also shows that the SNR gain produced by the SISO equalizer in Fig. 7 is similar to that shown in Fig. 5, corroborating the SNR advantage of SISO equalization over the MIMO equalization algorithm.

Figures 5–7 utilize adaptive equalizers, with the FIR filter trained independently based on the respective data. Theoretically, given that equalizers are designed to primarily mitigate linear channel impairments rather than ASE noise and non-linear distortions, the training process should produce consistent results across varying power levels. Figures 8(a) and 8(b) compare the equalizer performance between adaptive and constant equalizers based on the BER versus ROP curves. The constant coefficient equalizers were trained at an ROP level when the BER was slightly over the 3.8×10^{-3} hard decision-forward error correction (HD-FEC) threshold to ensure the stability of such an equalizer. The output FIR filter was then applied to the dataset using identical modulation formats, symbol rates, and equalization approaches (SISO or MIMO). The results show that employing constant coefficient equalizers instead of adaptive equalizers introduces a marginal performance penalty of ∼0.1 dB in proximity to the FEC threshold. This negligible performance degradation is deemed highly cost-effective, particularly when considering using only about 15% computational resources in the DSP process. The reduction in complexity is primarily attributed to the elimination of adaptive filter coefficient updates while maintaining the same number of taps for the linear convolution operation.

Figures 8(c) and 8(d) illustrate the performance differences between the signals on the I and Q axes as the ROP, transmission rate, and modulation format change. The Q-difference is calculated by subtracting the Q-factor corresponding to the I/Q independent Q-factor from the mean BER. The results demonstrate that the proposed SISO-DSP can achieve completely independent demodulation of the I and Q axis signals. The average Q-differences are ∼0.08 dB for the QPSK signal and 0.2 dB for the 16-QAM signal. The consistent I-channel superiority over Q-channel (Figs. 5–8) indicates transmitter-originated impairment rather than receiver limitations, as receiver-induced disparities would exhibit dependency on vibration-induced phase change. This fundamental transmitter asymmetry explains the SISO equalizer performance advantage over MIMO equalization. Crucially, even when I/Q channels maintain matched BER despite divergent noise spectra and frequency responses, SISO maintains superiority through channel-specific optimization, a phenomenon extending beyond the observed Q-difference metric.

In addition to ROP changing, the relative motion of satellites also introduces DFS variations for OISLs. Figures 9(a) and 9(b) depict the Q-factor variations for 40 Gbps QPSK (−41.2 dBm) and 80 Gbps 16-QAM (−35.0 dBm) modulation formats,

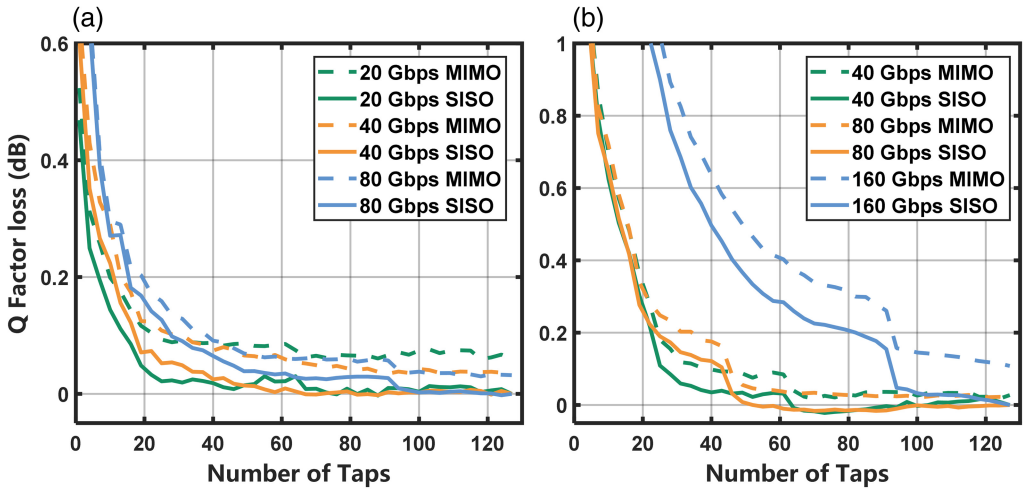


Fig. 7 Number of taps requirements versus Q-factor penalty for both SISO and MIMO equalizers across (a) QPSK (–43.4 dBm) and (b) 16-QAM (–36.8 dBm) signals.

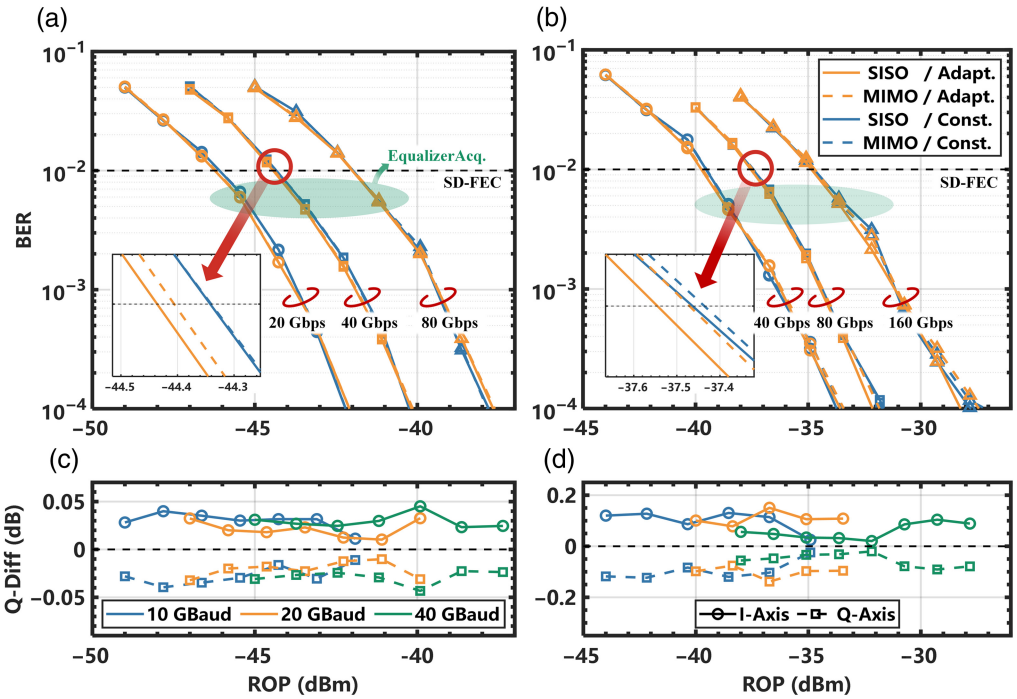


Fig. 8 BER versus ROP characteristics for both adaptive and constant equalizers across (a) QPSK and (b) 16-QAM signals; Performance differences between the signals on the *I* and *Q* axes across (c) QPSK and (d) 16-QAM signals.

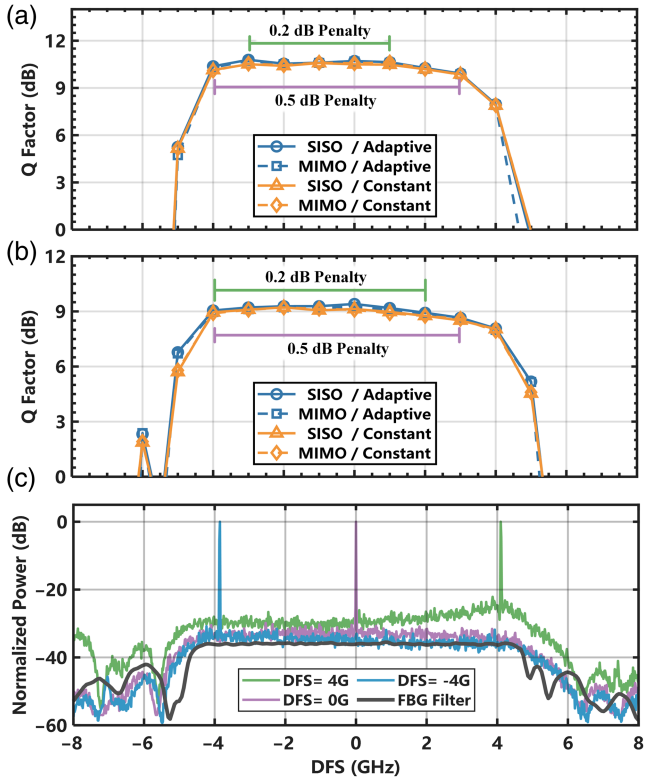


Fig. 9 *Q*-factor versus DFS for (a) 40 Gbps QPSK (−41.2 dBm) and (b) 80 Gbps 16-QAM (−35.0 dBm) modulation formats; (c) regenerated carrier spectrum after filtering.

respectively, as the simulated DFS is swept from −8 to +8 GHz by tuning the transmitter laser wavelength. Figure 9(c) illustrates the regenerated carrier spectrum at the receiver and the transmission spectrum of the FBG filter. The results show stable performance on both modulation formats across a significant DFS range. Specifically, QPSK exhibits a *Q*-factor penalty of 0.2 dB over a 4 GHz DFS range, whereas 16-QAM sustains the same penalty over a 6 GHz range. Relaxing the *Q*-factor penalty threshold to 0.5 dB extends the operational DFS range to −4 to +3 GHz for both formats, achieving the 7 GHz DFS tuning range required for the OISL. This asymmetric DFS tolerance arises from the asymmetric locking range between the master and slave lasers for OIL,[36] which locks more readily at negative than positive frequency shift. As shown in Fig. 9(c), the noise floor of the carrier recovery spectrum at +4 GHz DFS after OIL is ∼7.5 dB higher than that at zero DFS. This elevated noise results in performance penalties of 2.6 dB for QPSK and 1.1 dB for 16-QAM. Counterintuitively, QPSK shows a larger *Q*-factor loss to DFS impairments than 16-QAM. This occurs because the frequency offset tolerance of OIL-based carrier recovery decreases with lower injection power, and QPSK, operating at reduced power levels, makes the carrier recovery process more susceptible to DFS-induced degradation. It should be noted that although the behavior of individual OIL lasers depends on device-specific parameters, their maximum locking ranges universally scale with injected optical power. Consequently, a larger locking range can be established by increasing the preamplifier gain.

The fundamental requirement for employing a constant-tap equalizer is the maintenance of time-invariant channel impulse responses. However, the channel response and corresponding equalization filter would change with the sampling time, leading

to the requirement of a precise clock recovery as discussed in Sec. 2.2.1. Figure 10 shows the impact of residue clock errors on equalizer performance, specifically analyzing SISO and MIMO equalizers with a constant-tap configuration only as adaptive equalizers can compensate for the timing-error-induced ISI adaptively. Both SISO and MIMO equalization algorithms exhibit rapid performance degradation as clock skew increases, with identical degradation trends observed for each. Positive and negative clock skews produce equivalent effects on equalizer performance, showing symmetrical trends around zero skew. The clock skew tolerance of the QPSK modulation format exceeds that of 16-QAM, with tolerances corresponding to the 0.2 dB Q-factor penalty thresholds of $\pm 4.3\%$ and $\pm 2.3\%$, respectively.

For 20 GBaud synchronized QPSK and 16-QAM signals, Fig. 11 presents recovery outcomes using 20-μs data captures under varying SNR conditions. As it is difficult to establish a hardware-based voltage-controlled oscillator (VCO) clock tracking with offline DSO, cubic Lagrange interpolation for data resampling and a PID controller for optimal delay search/tracking instead. The PID controller achieves clock locking within 3 μs for both modulations. Although the clock recovers, lower-SNR signals exhibit greater timing jitter due to signal noise. However, although corresponding BER values [Figs. 11(c) and 11(d)] remain larger than the HD-FEC threshold, residual clock errors could be measured below $\pm 1.5\%$ (QPSK) and $\pm 2.1\%$ (16-QAM), confirming the algorithm's robust tracking capability despite implementation constraints.

The SHD architecture simultaneously transmits both carrier and signal to the receiver. However, a high CSPR can lead to signal power loss under constraints of received ROP, whereas a low CSPR may introduce noise during LO regeneration. Thus, the CSPR parameter needs to be optimized, as shown in Fig. 12. The results indicate that optimal CSPR values are -1 dB at 10 GBaud, -2 dB at 20 GBaud, and -3 dB at 40 GBaud for each respective symbol rate, applicable to both QPSK and 16-QAM modulation formats. These identified CSPR settings were consistently applied across all experimental tests in this study. Notably, optimal CSPR depends critically on carrier recovery noise levels, varying with different OIL

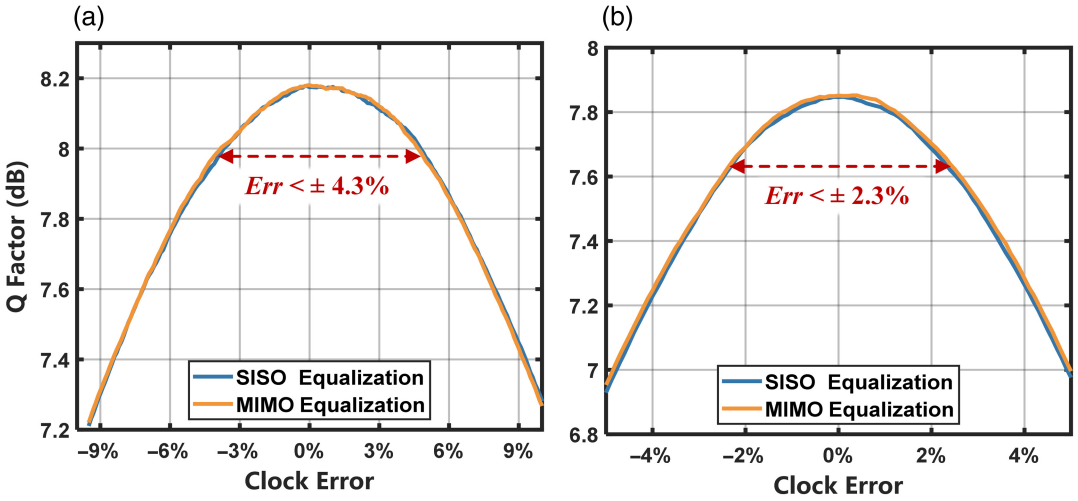


Fig. 10 Impact of clock recovery errors on constant-tap equalizers under (a) QPSK (−41.2 dBm, 40 Gbps) and (b) 16-QAM modulation (−36.7 dBm, 80 Gbps) formats.

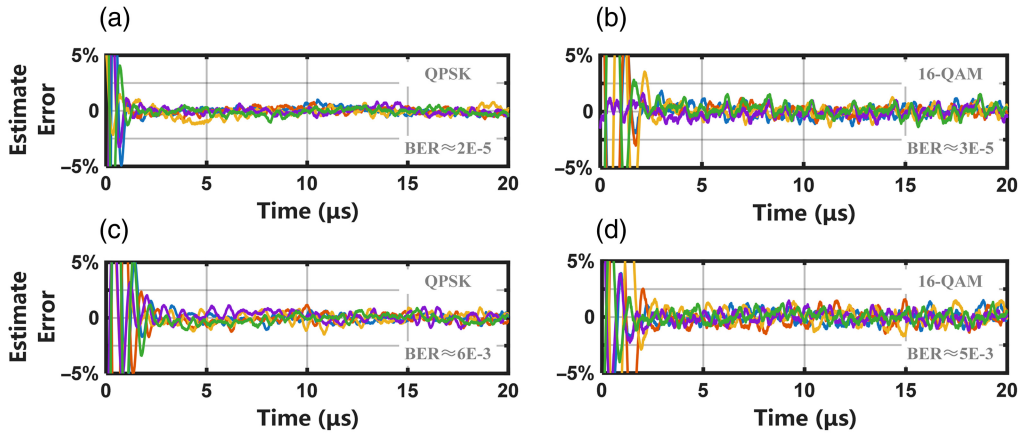


Fig.11 Recovery outcomes using 20-μs data captures with (a) QPSK format when BER = 2×10^{-5}; (b) 16-QAM format when BER = 3×10^{-5}; (c) QPSK format when BER $\approx 6 \times 10^{-3}$; (d) 16-QAM format when BER $\approx 5 \times 10^{-3}$.

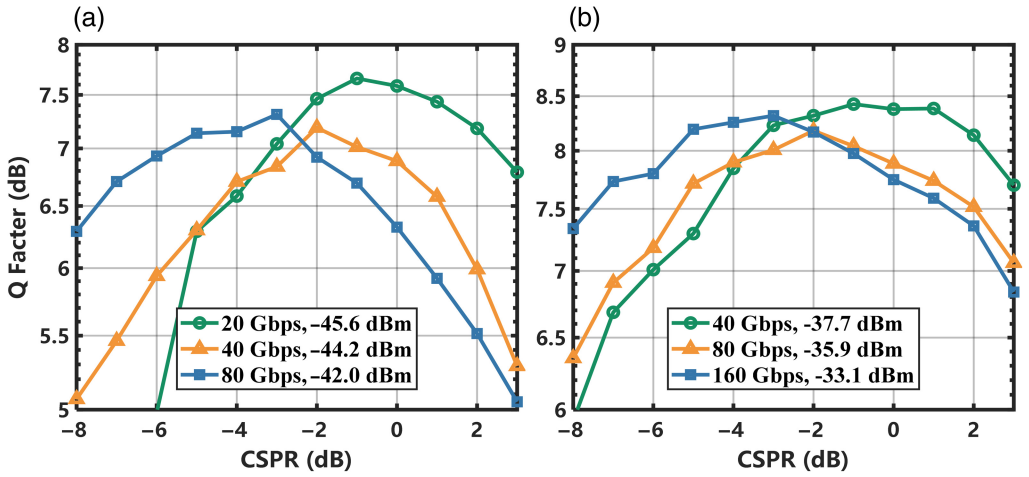


Fig. 12 Impact of CSPR on *Q*-factor results under (a) QPSK and (b) 16-QAM modulation formats.

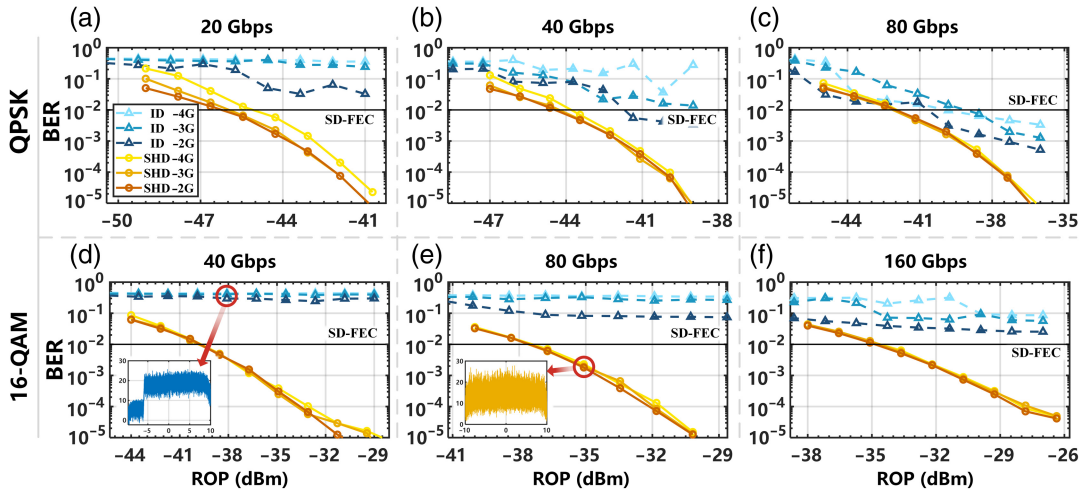


Fig. 13 Influence of ROP on BER across (a) 20 Gbps QPSK, (b) 40 Gbps QPSK, (c) 80 Gbps QPSK, (d) 40 Gbps 16-QAM, (e) 80 Gbps 16-QAM, and (f) 160 Gbps 16-QAM conditions under the DFS distortion of −2, −3, and −4 GHz using Nyquist sampling.

configurations, pre-amplifier settings, and FBG implementations.

Figure 13 illustrates the influence of ROP on BER across different baud rates and modulation formats under the DFS distortion of −2, −3, and −4 GHz using Nyquist sampling, with ID or SHD architecture. For SHD links, the proposed simplest DSP with a constant tap SISO equalizer is employed. By contrast, the ID DSP initially performs manual pre-compensation for DFSs, as conventional blind frequency offset recovery algorithms are not applicable to such significant DFS distortion. In addition, as Nyquist clock recovery is also unachievable in the presence of DFS and phase noise, physical clock attachment and adaptive equalization were employed during ID transmission. Despite the use of a complex algorithm and advanced information, the ID receiver still can't achieve the HD-FEC threshold under most conditions. This limitation arises from the DFS part of the signal spectrum beyond the ADC sampling range, resulting in spectral truncation by the anti-aliasing filter, as detailed in the subfigures. Conversely, the proposed PDM-SHD architecture exhibits remarkable stability across most conditions, with its performance remaining unaffected by DFSs for all tested 16-QAM conditions and the 80 Gbps QPSK conditions. At 20 and 40 Gbps QPSK conditions, a 4 GHz DFS induces sensitivity losses of ∼1.5 and 0.8 dB, respectively, primarily due to reduced power at the carrier regeneration module. This could potentially be mitigated through optimized CSPR selection or enhanced OIL modules. Recent proposals of OIL with sensitivities below −80 dBm suggest that OIL performance is not a fundamental constraint for the PDM-SHD architecture.[39] For the QPSK modulation, receiver sensitivities at the HD-FEC threshold for 20, 40, and 80 Gbps transmission links are −44.9, −43.2, and −40.8 dBm, respectively. Similarly, for the 16-QAM modulation format, receiver sensitivities for 40, 80, and 160 Gbps transmission links are −38.2, −36.1, and −33.0 dBm, respectively.

5 Conclusion

Given the stringent bandwidth and power consumption constraints of LEO OISLs, a low-complexity PDM-SHD architecture is experimentally demonstrated. By co-transmitting a low-power carrier, DFS impairments are compensated in the optical domain, enabling Nyquist sampling and IM/DD comparable signal processing. Compared with the conventional ID configuration, the PDM-SHD architecture requires only 46.1% ADC power consumption (40 Gbps 16-QAM) and about 15% DSP computation. Experimental results indicate that the proposed architecture exhibits robust performance across 7 GHz DFS distortion and ROP variations.

In the experiment, the phase rotation primarily originates from unavoidable mechanical vibrations in the devices' fiber pigtails under laboratory conditions, necessitating digital frame phase pre-compensation before the real-valued SISO DSP. It can alternatively be mitigated using integrated photonic devices or low-speed phase tracking devices. With DFS and phase impairments compensated in the optical domain, the I and Q axis signals are fully decoupled, indicating that the PDM-SHD architecture has the potential to transmit I and Q signals independently, even with differing clocks, SNRs, or modulation formats. This capability allows I and Q signals to originate from different devices or satellites, significantly optimizing satellite interconnection networks. The SISO DSP comprises only a clock recovery algorithm and SISO equalization, optimized for Nyquist sampling. Its complexity aligns with that of an IM/DD system, merging the high speed and sensitivity of coherent communication with the low complexity of IM/DD communication.

Although pilot carrier occupation of a polarization dimension precludes polarization multiplexing of data channels, the PDM-SHD architecture maintains fundamental WDM compatibility. This enables bandwidth expansion through wavelength-level system replication or employs optical frequency combs to further reduce carrier spectral efficiency loss.[40] Although the transmission of a pilot carrier would increase transmitter power consumption, the power savings substantially outweigh the associated overhead. Contemporary LEO constellations feature satellite spacings of only 1000 to 1500 km, which enables the emission optical power reduction from >2 W to ~100 mW, whereas carrier transmission adds <1 W overhead, considering a 10% EDFA efficiency. Comparative analysis of contemporary 200 Gbps modules reveals stark efficiency differences: IM/DD consumes 1.5 W[41] versus 19 W[42] for coherent detection. This tenfold difference primarily originates from simplified IM/DD DSP. Consequently, despite pilot transmission overhead, SHD achieves substantial net power savings in LEO crosslinks, establishing a practical technical framework for future OISLs.

6 Appendix A: Analysis of Practical DFSs in OISLs

During transmission, the relative motion between transmitter and receiver induces a frequency shift in the signal, known as DFSs. In LEO OISLs, this DFS causes the laser frequency shift to vary continuously as the satellites move. Given the low orbital altitudes and high velocities of LEO satellites, DFSs can significantly impair inter-satellite communication links.[8,43] Considering DFSs, the received signal can be represented in the frequency domain as

$$f_{\mathrm{RX}} = f_{\mathrm{TX}} \frac{1-(u_{\mathrm{RX}}/c)\cos\theta_{\mathrm{RX}}}{1-(u_{\mathrm{TX}}/c)\cos\theta_{\mathrm{TX}}}, \tag{2}$$

where f_{TX} and f_{RX} are the frequency domain signal at the transmitter and receiver, u_{TX} and u_{RX} are the speed of the two satellites, θ_{TX} and θ_{RX} are the angles between the established link and the movement direction of the satellite with the transmitter and receiver, and c is the speed of light.

LEO satellites are typically part of satellite constellations, with each satellite establishing communication links with only 3 to 5 neighboring satellites instead of the whole constellation. Consequently, satellite constellations must be considered when calculating DFSs. For the Walker constellation[9,43,44] consisting of N satellites distributed across P orbital planes, each plane is populated with $S = N/P$ satellites. The phase factor F controls the relative angular offset between satellites in adjacent planes and θ controls the inclination of orbital planes. Position vector for the kth satellite in the ith orbit can be expressed as

$$\begin{aligned} x_{ik} &= -R\cos\theta\sin\psi\sin\varphi + R\cos\psi\cos\varphi y_{ik} \\ &= R\cos\theta\cos\psi\sin\varphi + R\sin\psi\cos\varphi z_{ik} \\ &= R\sin\theta\sin\varphi, \end{aligned} \tag{3}$$

where

$$\psi = 2\pi\frac{i}{P}, \varphi = \omega t + 2\pi\left(\frac{k}{S}+\frac{iF}{PS}\right),$$

and $R = R_{\mathrm{earth}} + H$ is the distance between the satellite and the earth center with $R_{\mathrm{earth}} \approx 6371$ km as the Earth's radius and H as the orbital height. ω is the angular velocity of a satellite with $\omega = \sqrt{\mathrm{GM}/R^3}$, where $\mathrm{GM} \approx 3.9857 \times 10^{14}$ m^3/s^2.

For the communication link established between two satellites occupying the same orbit, the DFS does not exist because they do not undergo relative displacement. Here, we only focus exclusively on situations where a communication link is established with the kth satellite of a nearby orbit. The DFS is given by

$$\Delta f = -f_{\mathrm{TX}} \cdot \frac{c}{\omega R} \cdot \frac{\sqrt{a\cos(2\omega t+\xi)+b}}{a\sin(2\omega t+\xi)}, \tag{4}$$

where

$$\begin{aligned} &\xi = \frac{2\pi F}{PS},\ \chi = \frac{2\pi}{P}, \\ &a = \sin^2\theta(1-\cos\chi), \\ &\mathrm{b} = 2\cos\theta\sin\kappa\sin\xi \\ &\quad -(\sin^2\theta - \sin^2\theta\cos\chi + 2\cos\chi)\cos\xi + 2. \end{aligned} \tag{5}$$

Referring to a communication satellite constellation configuration,[17] Fig. 14 shows the DFS for satellites within a constellation defined by the following parameters: $H = 560$ km, $P = 6$, $S = 58$, $F = 3$, and $\theta = 70$ deg, whereas the satellite orbits the Earth every 42 min. The two satellites engaged in communication both commence from the ascending node of their respective orbits. Each orbit around the Earth results in two cycles of variations in DFS impairment, with the maximum shift of ± 3.52 GHz.

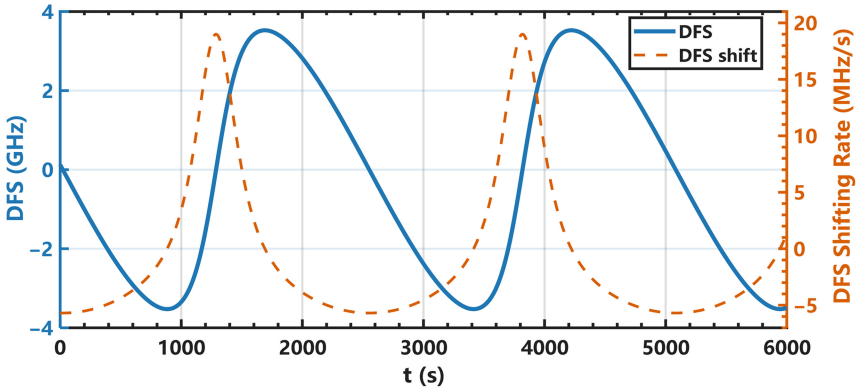


Fig. 14 DFS fluctuation and shifting rate for satellite constellation with $H = 560$ km, $P = 6$, $S = 58$, $F = 3$, and $\theta = 70$ deg.

7 Appendix B: Dynamic DFS-Induced Phase Change

In the ideal SHD reception, the carrier and signal originate simultaneously from the same laser, establishing perfectly stable phase coherence. However, the practical demonstration processes induce distinct optical paths for signal and carrier, which length difference causes the signal and LO to correspond to non-simultaneous DFS timestamps. When rapid laser frequency drift occurs, the resultant phase discrepancy is expressed as

$$\Delta\nu = \frac{n\Delta L}{c} \cdot \Delta f', \tag{6}$$

where $\Delta\nu$ denotes the residual frequency shift between the signal and the carrier, c is the light speed, and $\Delta f'$ is the DFS shifting rate. This causes a phase change between the signal and carrier

$$\Delta\varphi = 2\pi \int_0^t \Delta\nu(\tau)\mathrm{d}\tau = \frac{2\pi}{c}\Delta f \cdot n\Delta L, \tag{7}$$

with $\Delta\varphi$ representing the phase change after time t. Equation (7) demonstrates that the optical path difference-induced phase change scales linearly with $\Delta f \cdot n\Delta L$.

For the constellation detailed in Appendix A, the DFS shifting rate ranges periodically between -5 and 20 MHz/s. Given 10 cm fiber length mismatch, Fig. 15 quantifies the resulting frequency offset and phase change evolution. The results show that despite the megahertz-scale frequency offset induced by dynamic DFSs, accumulated phase rotation attains ± 10 rad due to the 41-min cycle duration. The DFS-induced frequency shifts remain much below fiber vibration frequencies, enabling simultaneous compensation of both effects. However, when integrated devices are employed to eliminate fiber vibration effects, the optical path difference must be constrained to prevent significant phase accumulation. For instance, maintaining a path difference of ≤ 0.1 mm could limit the phase difference to $\leq \pm 1$ deg.

8 Appendix C: DSP Complexity Analysis

DSP algorithms should be applied after the receiver captures the signal to mitigate residual impairments, including clock offset, ISI, DFS, and phase noise. Considering fundamental DSP algorithms only, multipliers' and adders' requirements for the proposed PDM-SHD and conventional ID architectures are discussed as follows.

8.1 Clock Recovery

As detailed in Sec. 2.2.1, the receiver architecture determines the selection of the timing recovery algorithm: ID architecture employs Gardner algorithm,[45] whereas SHD employs the M–M algorithm.[33] Their respective error functions are expressed as

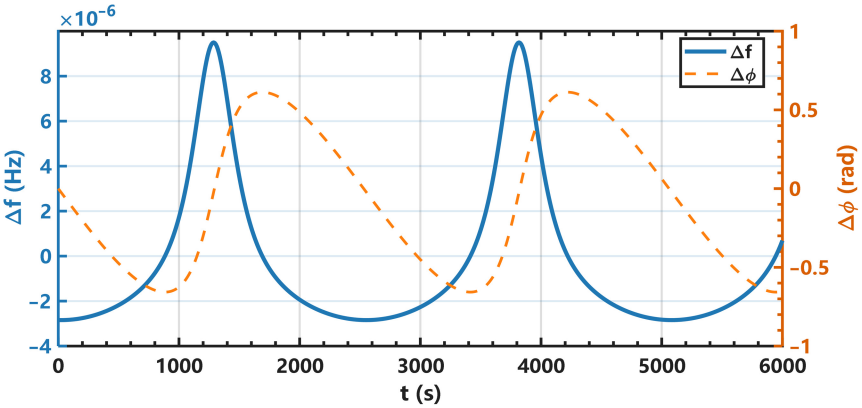


Fig. 15 Dynamic DFS-induced frequency and phase shift with 10 cm fiber length mismatch of satellite constellation with $H = 560$ km, $P = 6$, $S = 58$, $F = 3$, and $\theta = 70$ deg.

$$e_{\text{Gardner}}(n) = [I(n) - I(n-1)] \cdot I\left(n - \frac{1}{2}\right) + [Q(n) - Q(n-1)] \cdot Q\left(n - \frac{1}{2}\right), \tag{8}$$

$$\begin{cases} e_{\text{Muller},I}(n) = \text{sign}[I(n)] \cdot I(n-1) - \text{sign}[I(n-1)] \cdot I(n) \\ e_{\text{Muller},Q}(n) = \text{sign}[Q(n)] \cdot Q(n-1) - \text{sign}[Q(n-1)] \cdot Q(n) \end{cases}, \tag{9}$$

where e denotes the error function value at sample index n. Modern implementations typically employ VCO direct tuning for timing realignment, circumventing computational overhead associated with interpolation filters. The Gardner algorithm necessitates two samples per symbol, demanding 4 real multiplication operations and 6 addition operations per symbol. Conversely, the M–M algorithm achieves zero multiplication operations with only 2 real addition operations per symbol.

8.2 Equalization

Equalization algorithms in coherent communication systems exhibit diverse implementations including feed-forward equalizers (FFEs), decision feedback equalizers (DFEs), and maximum likelihood sequence estimation (MLSE). This study focuses on the fundamental DD-based N-tap DFE,[38] whose operation comprises two distinct phases: FIR filter application and coefficient updating.

In the FIR filter application stage for ID architecture, the equalized outputs $E_I(n)$ and $E_Q(n)$ are computed through coupled signal processing

$$\begin{cases} E_I(n) = \sum_{k=0}^{N-1} [p_{I,k}(n) x_{I,k}(n) + p_{Q,k}(n) x_{Q,k}(n)] \\ E_Q(n) = \sum_{k=0}^{N-1} [-p_{Q,k}(n) x_{I,k}(n) + p_{I,k}(n) x_{Q,k}(n)] \end{cases}, \tag{10}$$

where $p_{I,k(n)}$ and $p_{Q,k(n)}$ represent the I/Q tap coefficients, $x_{I,k(n)}$ and $x_{Q,k(n)}$ denote the delayed I/Q components. This cross-coupled computation addressing phase rotation effects requires $4N$ real multipliers and $4N-1$ real adders per sample. Remarkably, SHD architecture eliminates I/Q coupling considerations, simplifying the expressions to

$$\begin{cases} E_I(n) = \sum_{k=0}^{N-1} p_{I,k}(n) x_{I,k}(n) \\ E_Q(n) = \sum_{k=0}^{N-1} p_{Q,k}(n) x_{Q,k}(n) \end{cases}, \tag{11}$$

reducing computational load to $2N$ real multipliers and $2N-1$ adders.

Coefficient updating occurs exclusively during link establishment. The update functions for the ID architecture employ

$$\begin{cases} p_{I,k}(n+1) = p_{I,k}(n) + \mu(R_k^2 - E_I^2 - E_Q^2)(E_I x_{I,k} + E_Q x_{Q,k}) \\ p_{Q,k}(n+1) = p_{Q,k}(n) + \mu(R_k^2 - E_I^2 - E_Q^2)(-E_Q x_{I,k} + E_I x_{Q,k}) \end{cases}, \tag{12}$$

where μ denotes the convergence step-size, R_k is the decided radius for the kth signal, which is a constant for QPSK constellations. It demands $10N$ multiplications and $8N$ adders for coefficient updating, giving a total requirement of $14N$ real multipliers and $12N-1$ adders. The SHD architecture permits further simplification

$$\begin{cases} p_{I,k}(n+1) = p_{I,k}(n) + \mu(1 - E_I^2) E_I x_{I,k} \\ p_{Q,k}(n+1) = p_{Q,k}(n) + \mu(1 - E_Q^2) E_Q x_{Q,k} \end{cases}, \tag{13}$$

achieving $8N$ multiplications and $4N$ adders for coefficient updating, giving the total requirement would be $10N$ real multipliers and $8N-1$ adders.

8.3 DFS Compensation

The DFS manifests as significant time-varying frequency offsets, which can be mitigated through carrier recovery algorithms in ID architectures. The classical Viterbi–Viterbi (V–V) frequency offset estimation algorithm[46] employs Mth power schemes to eliminate M-ary phase modulation effects. The process initiates with conjugate multiplication between consecutive symbols to capture phase differences, followed by the fourth-power operation to remove phase modulation components

$$d(n) = \frac{1}{4} \arg\{[x(n) \cdot x^*(n-1)]^4\}, \tag{14}$$

where $d(n)$ is the phase change on the nth signal and x^* denotes the complex conjugation. Subsequent averaging over L symbols enhances noise immunity

$$\hat{d}(n) = \frac{1}{L} \sum_{k=0}^{L-1} d(n-k). \tag{15}$$

Notably, the fourth-power operation decomposes into two sequential squaring stages, requiring 6 real multipliers, whereas the initial complex multiplication consumes 3 real multipliers. The arctangent operation employs coordinate rotation digital computer (CORDIC) algorithms[47] or lookup tables without a multiplier. The accumulated phase compensation $D(n) = D(n-1) + \hat{d}(n)$ applies via trigonometric transformation

$$\begin{cases} I_{\text{out}} = I_{\text{in}} \cos D(n) - Q_{\text{in}} \sin D(n) \\ Q_{\text{out}} = I_{\text{in}} \sin D(n) + Q_{\text{in}} \cos D(n) \end{cases}, \tag{16}$$

The DFS compensation based on the V–V algorithm achieves 13 real multipliers and 4 adders in total.

8.4 Phase Noise Compensation

The V–V algorithm serves dual purposes in coherent systems, being applicable to both carrier recovery and phase noise compensation. The key distinction lies in their processing focus: DFS compensation extracts inter-symbol phase differences, whereas phase noise compensation evaluates absolute phase characteristics. The phase noise estimation algorithm gives

$$\varphi(n) = \frac{1}{4} \arg[x^4(n)], \tag{17}$$

$$\hat{\varphi}(n) = \frac{1}{L} \sum_{k=0}^{L-1} \varphi(n-k), \tag{18}$$

where $\varphi(n)$ represents the combined phase distortion from phase noise and ASE at the nth symbol, with $\hat{\varphi}(n)$ being the noise-suppressed estimate. The compensation applies

$$\begin{cases} I_{\text{out}} = I_{\text{in}} \cos \hat{\theta} - Q_{\text{in}} \sin \hat{\theta} \\ Q_{\text{out}} = I_{\text{in}} \sin \hat{\theta} + Q_{\text{in}} \cos \hat{\theta} \end{cases}, \tag{19}$$

Fourth-power calculation requires 6 real multipliers (two squaring steps) and phase rotation consumes 4 real multipliers, totaling 10 real multipliers and 4 adders.

Disclosures

The authors declare that there are no financial interests, commercial affiliations, or other potential conflicts of interest that could have influenced the objectivity of this research or the writing of this paper.

Code and Data Availability

The data supporting this paper are available from the corresponding author upon reasonable request.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant Nos. 62401220, 62205111, and 62225110), the Major Program (JD) of Hubei Province (Grant No. 2023BAA001-1), and the Key Research and Development Program of Hubei Province of China (Grant No. 2025BAB007). The computation is completed in the HPC Platform of Huazhong University of Science and Technology.

References

1. O. Kodheli et al., "Satellite communications in the new space era: a survey and future challenges," *IEEE Commun. Surv. Tutorials* **23**(1), 70–109 (2021).
2. H. Kaushal and G. Kaddoum, "Optical communication in space: challenges and mitigation techniques," *IEEE Commun. Surv. Tutorials* **19**(1), 57–96 (2017).
3. N. Ye et al., "Techno-economic assessment of LEO mega-constellation with multi-satellite collaboration," *IEEE Commun. Mag.* **62**(11), 36–42 (2024).
4. Y. Zhao et al., "Dual-polarization IMDD system for data-center connectivity," *J. Lightwave Technol.* **43**, 6044–6049 (2025).
5. E. E. Elsayed and B. B. Yousif, "Performance evaluation and enhancement of the modified OOK based IM/DD techniques for hybrid fiber/FSO communication over WDM-PON systems," *Opt. Quant. Electron.* **52**(9), 385 (2020).
6. S. Yamakawa, T. Araki, and Y. Hisada, "Trade-off between IM-DD and coherent system in high-data-rate optical interorbit links," *Proc. SPIE* **3615**, 80–89 (1999).
7. E. Ip et al., "Coherent detection in optical fiber systems," *Opt. Express* **16**, 753–791 (2008).
8. M. A. Fernandes et al., "Digitally mitigating Doppler shift in high-capacity coherent FSO LEO-to-Earth links," *J. Lightwave Technol.* **41**(12), 3993–4001 (2023).
9. I. P. Vieira, T. C. Pita, and D. A. A. Mello, "Modulation and signal processing for LEO-LEO optical inter-satellite links," *IEEE Access* **11**, 63598–63611 (2023).
10. S. M. McKevett, "Between sky and space: NEPA's extraterritorial application to the stratosphere and implications for SpaceX's Starlink satellite constellation," *Geo. Environ. Law Rev.* **36**, 375 (2023).
11. DARPA, "Space-based adaptive communications node (Space-BACN)," https://www.darpa.mil/work-with-us/space-based-adaptive-communications-node (accessed 1 May 2024).
12. E. Pincemin et al., "End-to-end interoperable 400-GbE optical communications through 2-km 400GBASE-FR4, 8 × 100-km 400G-OpenROADM and 125-km 400-ZR fiber lines," *J. Lightwave Technol.* **41**(4), 1250–1257 (2023).
13. F. Farmakis et al., "High specific energy lithium cells for space exploration," *E3S Web Conf.* **16**, 08003 (2017).
14. D. I. Suryanti, S. Ramayanti, and M. Mukhayadi, "Preliminary power budget analysis for equatorial low Earth orbit (LEO) communication satellite," *Indones. J. Aerosp.* **19**(1), 67–78 (2021).
15. C. C. Helms, "A survey of launch services 2016–2020," in *AIAA Propulsion and Energy 2020 Forum, Virtual Event*, American Institute of Aeronautics and Astronautics (2020).
16. T. Gui et al., "Real-time demonstration of homodyne coherent bidirectional transmission for next-generation data center interconnects," *J. Lightwave Technol.* **39**(4), 1231–1238 (2021).
17. N. Pachler et al., "An updated comparison of four low Earth orbit satellite constellation systems to provide global broadband," in *IEEE Int. Conf. Commun. Workshops (ICC Workshops)*, IEEE, Montreal, QC, pp. 1–7 (2021).
18. M. Gregory et al., "TESAT laser communication terminal performance results on 5.6 Gbit coherent inter satellite and satellite to ground links," *Proc. SPIE* **10565**, 37 (2017).
19. R. Larsson, K. Vijayan, and P. A. Andrekson, "Zero-offset frequency locking of lasers at low optical powers with an optical phase locked loop," *J. Lightwave Technol.* **42**(3), 1183–1190 (2024).
20. M. Seimetz, M. Noelle, and E. Patzak, "Optical systems with high-order DPSK and star QAM modulation based on interferometric direct detection," *J. Lightwave Technol.* **25**(6), 1515–1530 (2007).
21. T. Miyazaki and F. Kubota, "PSK self-homodyne detection using a pilot carrier for multibit/symbol transmission with inverse-RZ signal," *IEEE Photonics Technol. Lett.* **17**(6), 1334–1336 (2005).
22. M. Morsy-Osman et al., "DSP-free 'coherent-lite' transceiver for next generation single wavelength optical intra-datacenter interconnects," *Opt. Express* **26**(7), 8890 (2018).
23. W. Li et al., "SOA enabled self-homodyne coherent bidirectional transmission for metro-datacenter interconnects," *J. Lightwave Technol.* **41**(9), 2601–2612 (2023).
24. M. Zhang et al., "Self-homodyne coherent transmission with all-optical clock synchronization for DSP-free co-packaged optics," in *Opt. Fiber Commun. Conf. (OFC)*, Optica Publishing Group, San Diego, CA, p. M3E.3 (2023).
25. H. Zhou et al., "Demonstration of turbulence-resilient self-homodyne 12-Gbit/s 16-QAM free-space optical communications using a transmitted pilot tone," *J. Lightwave Technol.* **41**(11), 3438–3445 (2023).
26. M. J. Fice et al., "Homodyne coherent optical receiver using an optical injection phase-lock loop," *J. Lightwave Technol.* **29**(8), 1152–1164 (2011).
27. A. W. Bernini, M. J. Fice, and K. Balakier, "Phase locking of an optical injection phase-lock loop coherent receiver under emulated atmospheric fading conditions," in *Opt. Fiber Commun. Conf. (OFC)*, IEEE, San Diego, CA, pp. 1–3 (2023).
28. K. Li et al., "Simplest DSP enabled baud rate sampling self-homodyne coherent architecture for inter-satellite communications," in *ECOC 2024; 50th Eur. Conf. Opt. Commun.*, pp. 410–413 (2024).
29. X. Zhao et al., "Circle polarization shift keying with direct detection for free-space optical communication," *J. Opt. Commun. Netw.* **1**(4), 307 (2009).
30. J. Mo et al., "Hybrid architectures with few-bit ADC receivers: achievable rates and energy-rate tradeoffs," *IEEE Trans. Wireless Commun.* **16**(4), 2274–2287 (2017).
31. A. Molev-Shteiman et al., "New equivalent model of a quantizer with noisy input and its applications for MIMO system analysis and design," *IEEE Access* **8**, 162601–162624 (2020).

32. F. Gardner, "A BPSK/QPSK timing-error detector for sampled receivers," *IEEE Trans. Commun.* **34**(5), 423–429 (1986).
33. K. Mueller and M. Muller, "Timing recovery in digital synchronous data receivers," *IEEE Trans. Commun.* **24**(5), 516–531 (1976).
34. K. Yadav, P.-H. Hsieh, and A. C. Carusone, "Loop dynamics analysis of PAM-4 Mueller–Muller clock and data recovery system," *IEEE Open J. Circuits Syst.* **3**, 216–227 (2022).
35. J. Im et al., "A 40-to-56 Gb/s PAM-4 receiver with ten-tap direct decision-feedback equalization in 16-nm FinFET," *IEEE J. Solid-State Circuits* **52**(12), 3486–3502 (2017).
36. Z. Liu and R. Slavik, "Optical injection locking: from principle to applications," *J. Lightwave Technol.* **38**(1), 43–59 (2020).
37. E. K. Lau, L. J. Wong, and M. C. Wu, "Enhanced modulation characteristics of optical injection-locked lasers: a tutorial," *IEEE J. Sel. Top. Quantum Electron.* **15**(3), 618–633 (2009).
38. M. E. Austin, "Decision-feedback equalization for digital communication over dispersive channels," Tech. Rep. 461, MIT Research Laboratory of Electronics, Cambridge, Massachusetts (1967).
39. J. C. Skehan, M. Karlsson, and P. A. Andrekson, "Phase-locked, pre-amplified optical injection locking at low input powers," *Opt. Express* **32**(2), 1956–1965 (2024).
40. C. Zhang et al., "Clone-comb-enabled high-capacity digital-analogue fronthaul with high-order modulation formats," *Nat. Photonics* **17**(11), 1000–1008 (2023).
41. Cisco, "Cisco transceiver modules – Cisco 200G QSFP56 cables and transceiver modules data sheet," https://www.cisco.com/c/en/us/products/collateral/interfaces-modules/transceiver-modules/nb-06-200g-qsfp56-cables-trans-mod-ds-cte-en.html (accessed 6 July 2025).
42. Cisco, "Cisco transceiver modules – Cisco digital CFP2-DCO coherent optical module data sheet," https://www.cisco.com/c/en/us/products/collateral/interfaces-modules/transceiver-modules/datasheet-c78-743732.html (accessed 6 July 2025).
43. Q. Yang, L. Tan, and J. Ma, "Doppler characterization of laser inter-satellite links for optical LEO satellite constellations," *Opt. Commun.* **282**(17), 3547–3552 (2009).
44. E. Lansard, E. Frayssinhes, and J.-L. Palmade, "Global design of satellite constellations: a multi-criteria performance comparison of classical walker patterns and new design patterns," *Acta Astronaut.* **42**(9), 555–564 (1998).
45. D. Lim, "A modified Gardner detector for symbol timing recovery of M-PSK signals," *IEEE Trans. Commun.* **52**(10), 1643–1647 (2004).
46. C. Spatharakis et al., "Frequency offset estimation and carrier phase recovery for high-order QAM constellations using the Viterbi-Viterbi monomial estimator," in *Int. Symp. Commun. Syst. Netw. Digit. Signal Process. (CSNDSP)*, IEEE, Manchester, pp. 781–786 (2014).
47. J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Trans. Electron. Comput.* **EC-8**(3), 330–334 (1959).

Junda Chen has been a postdoctoral researcher at the School of Optical and Electronic Information in Huazhong University of Science and Technology, Wuhan, China, since 2023 and joined the Department of Microtechnology and Nanoscience in Chalmers University of Technology in 2024. He holds a PhD from Huazhong University of Science and Technology in 2023. He has authored 28 academic publications and presented his work at premier international conferences, including the European Conference on Optical Communication (ECOC) and the Optical Fiber Communication Conference (OFC). His research focuses on space optical communication and fiber-optic communication systems.

Kun Li received his BS degree in the School of Optical and Electronic Information from Huazhong University of Science and Technology in 2023. He is currently pursuing his MS degree, with research interests in free space optical communications and injection locking lasers.

Tianjin Mei received his BS degree in optoelectronic information science and engineering from Huazhong University of Science and Technology in 2020. Since 2021, he has been pursuing his PhD in optoelectronic information engineering at the School of Optical and Electronic Information, Huazhong University of Science and Technology. His research interests include free-space optical communication and indoor optical wireless communication systems.

Mingming Zhang has been a postdoctoral researcher at the School of Optical and Electronic Information in Huazhong University of Science and Technology since 2025. He holds a PhD from Huazhong University of Science and Technology in 2025. He is interested in datacenter optical interconnections and fiber-optic communication systems.

Zihe Hu received her BS degree in 2013 from the School of Electronic Information and Communications and her MSc degree in 2016 from the School of Optical and Electronic Information, Huazhong University of Science and Technology, where she is currently working toward her PhD with the School of Optical and Electronic Information. Her research interests include long-haul optical communications, digital signal processing, and integrated sensing and communications.

Jiajun Zhou has been an assistant researcher at the JFS Laboratory since 2023, and earned her PhD from Huazhong University of Science and Technology in 2023. Her research focuses on fiber-optic communication systems and silicon photonics.

Chen Liu received his PhD from Huazhong University of Science and Technology in 2004. From 2006 to 2019, he was with the School of Optical and Electronic Information, Huazhong University of Science and Technology, as an associate professor. Since 2020, he has been a professor with the School of Optical and Electronic Information and the Jinyinhu Laboratory, Wuhan, China. His research interests include free-space optical communications and optical phased arrays.

Ming Tang is a professor and party committee secretary at the School of Optical and Electronic Information, Huazhong University of Science and Technology. As a distinguished scholar, he is a recipient of the National Science Fund for Distinguished Young Scholars, one of China's most prestigious academic foundations. He received his bachelor's degree from Huazhong University of Science and Technology (2001) and his PhD from Nanyang Technological University (2005). His research spans optical communications and optical sensing, where he has made significant contributions, publishing over 500 research papers and conference articles. He holds the distinction of an IEEE Senior Member.

Peter A. Andrekson is a full professor at the Department of Microscience and Nanoscience, Chalmers University of Technology, where he earned his PhD in 1988. With an outstanding career spanning over three decades in optical communications, he has authored approximately 500 scientific publications, including *Nature, Advances in Optics and Photonics, Light Science and Applications*, etc. His leadership in the field is demonstrated through his roles as general chair for both ECOC 2017 and the upcoming ECOC 2025. Recognized as a Fellow of both Optica and IEEE, and as a member of the Royal Swedish Academy of Engineering Sciences (IVA), he has made seminal contributions to optical parametric amplifiers and high-speed communication systems.