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A FR3, 25 dBm Unbalanced MMIC GaAs Doherty Power Amplifier with Auxiliary Gate Voltage Modulation for Linearity Improvement

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***Abstract*—This paper presents a compact and fully monolithically integrated unbalanced Doherty power amplifier (DPA) for the FR3 mid-band spectrum, implemented in the WIN Semiconductors PQH1-0P 180 nm E-mode GaAs pHEMT technology. The design absorbs the intrinsic device output capacitance, C_{out}, using a parallel inductor in the Doherty combiner network to enhance bandwidth (BW). The asymmetric structure helps to improve output back-off (OBO) performance by more than 7 dB and makes it suitable for high peak to average power ratio (PAPR) signals. The DPA was evaluated under different auxiliary gate voltages to find the proper function as a gain enhancement technique in the saturation region to improve linearity. The DPA demonstrates a maximum small signal gain of 12.8 dB at 7.3 GHz, an output power of 23 – 24.5 dBm at saturation, a saturation drain efficiency (DE) of 45 - 57% and a 7 dB back-off DE of 30 - 45% over the BW from 7.3 to 8.7 GHz, which is equal to 17.5% fractional bandwidth (FBW), with a compact size of 2.5 mm × 2 mm.**

***Index Terms*—auxiliary gate voltage function, Linearity, Doherty power amplifier, fully integrated MMIC, GaAs HEMT, output back-off, peak-to-average power ratio, FR3 6G**

I. Introduction

6G communication systems widely adopt complex and modern modulation schemes with high PAPR signals to improve transmission rate and spectral efficiency, which requires PAs to provide a greater back-off level and enhanced efficiency. DPAs are a classic and promising OBO efficiency enhancement architecture, which has been widely studied [1], [2]. In addition, other load modulated architectures, including reverse-modulated DPA [3], distributed efficient PA (DEPA) [4], [5], and load modulation balanced amplifier (LMBA) [6], [7], have also been reported. Significant gain compression at saturation is the drawback of DPAs which can degrade the linearity performance.

This paper addresses DPA gain compression at saturation of the main amplifier by applying RF input power dependent auxiliary gate bias modulation to the fabricated DPA. This technique leverages the auxiliary gate voltage function finding algorithm (AGVFFA) to mitigate the gain compression problem at saturation and improve linearity, [8], [9]. The quarter-wavelength transformer (QWT) of the designed DPA is implemented using a lumped π-type network to reduce the occupied size. The auxiliary branch of output combiner is the simplest with only one parallel resonant inductor to absorb C_{out}, and a small series inductor L_S compensates for the deviation of the parasitic output capacitance C_{out} of transistor in different power states and a zero phase shift network. The results show that this scheme can reduce the complexity of the auxiliary branch design and minimize insertion loss. Furthermore, the asymmetric structure helps to improve the OBO range. The paper is organized as follows. Section II discusses the DPA design methodology, which comprises two sections: the Low-Q output network with C_{out} compensation and the input network including power splitting. In Section III, DPA characterization is presented, covering small-signal analysis, power gain, efficiency, bandwidth, and exploration of an algorithm to find the auxiliary gate voltage function. Finally,

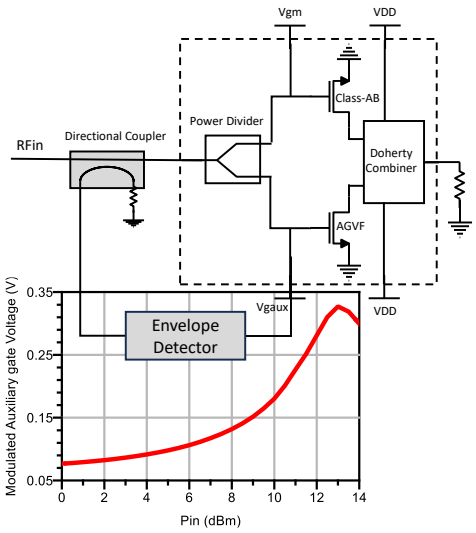

Fig. 1. An AGVF biased DPA structure. A sample of the input power level from directional coupler generates AGVF using envelope detector.

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a comparison table and concluding remarks are provided in Section IV.

II. Doherty power amplifiers Design

A. Compact Doherty Output Network Design with Absorbed Output Capacitance, C_{out}

The DPA block diagram along with the auxiliary gate voltage modulation architecture is illustrated in Fig. 1. As shown in Fig. 2, the transistor can be modeled as a current source with a nonlinear parasitic output capacitance, C_{out}, which can cause performance deterioration. The enhancement in bandwidth has been applied by compensating C_{out} of the main and auxiliary transistors using a shunt inductor L_P. The output network of the DPA includes a high-pass lumped element π-type network with a characteristic impedance of $\sqrt{2}\,R_{\text{out}}$ as a QWT in the main path and a bandpass network with zero phase shift composed of L_1, C_1, L_2, and C_2 in the auxiliary path, operates as an impedance transformer in saturation region (SR) and maintains the open circuit of the output impedance in the back-off region (BOR) at the same time. The C_{out} of the auxiliary transistor in the BOR and SR is different due to power dependency of average C_{out}. As a result, the open-circuit requirement in the BOR and optimal power matching in the SR cannot be satisfied at the same time with a single shunt inductor. To address this, a power enhancing series inductor L_s is placed after auxiliary transistor to compensate C_{out} nonlinearity. Finally, a post impedance matching network to 50 Ω can be added to the output combiner. The impedance of L_s should be much smaller than R_{opt} as defined in Equ. 1, [2], which ω is angular frequency.

$$\omega L_s < R_{opt}/5. \tag{1}$$

In the main path, L_{pM} and the first L_T of QWT are connected in parallel. Similarly, the second L_T of the QWT in the main path is in parallel with L_2 of the zero phase shift bandpath filter in the auxiliary path. As depicted in Fig. 3, the equivalent inductances resulting from these parallel combinations are implemented in the final design of the output combiner. To implement the equivalent of L_{pM} in parallel with L_T and L_{pA}, off-chip inductors or bonding wires with high Q-factors are potential candidates [10], [11]. However, to achieve full monolithic integration, on-chip components are utilized for both L_{pM} and L_{pA}. These inductors are realized using on-chip transmission lines (TLs), due to their higher Q-factors and better DC current handling compared to conventional on-chip inductors.

B. Power Splitting and Input Network

To improve the overall gain of the DPA, the auxiliary PA is biased at the shallower class-C and a reversed uneven power splitter (RUPS) is adopted to deliver more power to the main PA [12]. However, the gain of DPA in the SR is reduced because of a class-C operation of the auxiliary PA and also degrades in the back-off region caused by a shortage of the input power toward the main. Asymmetric stabilizing networks

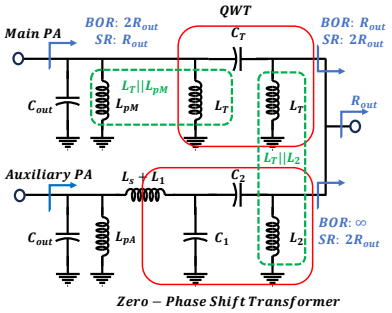

Fig. 2. Initial design of a Low-Q DPA output network includes C_{out} absorption inductor, a high-pass lumped element π-type network as the QWT in the main path and a bandpass network with a zero phase shift in the auxiliary path incorporating a power enhancing series inductor, L_s.

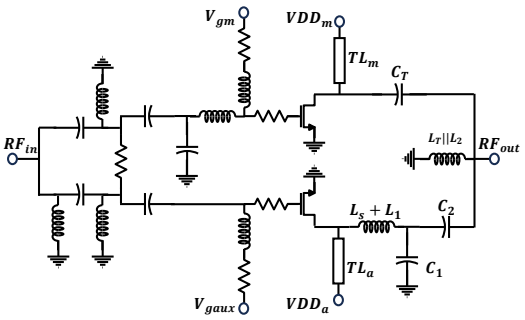

Fig. 3. The DPA top schematic including power splitter, input matching network and circuit evolution of Doherty output combiner from initial design.

are applied for DPA by adding a resistor of 5 Ω and 3 Ω to the gate of main and auxiliary PA, respectively. In fact, the main PA dominates the small signal stability of the DPA, since the auxiliary PA provides no gain in the BOR. The DPA is implemented in WIN Semiconductors PQH1-0P 180 nm E-mode GaAs pHEMT technology. The device size for main and auxiliary PA are selected as 8×50 um and 8×75 um, respectively. The DPA top schematic and chip photograph are shown in Fig. 3 and Fig. 4, respectively. The chip size is only 2.5 mm × 2 mm.

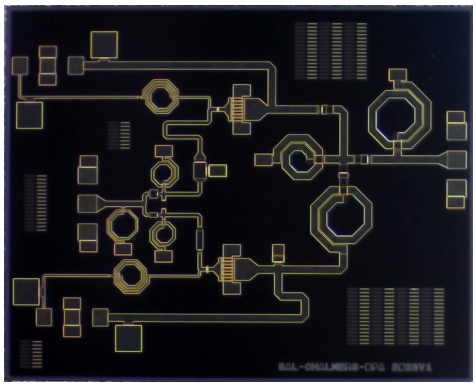

Fig. 4. DPA Chip photograph fabricated in 180 nm GaAs technology, Chip size is 2.5 mm × 2 mm.

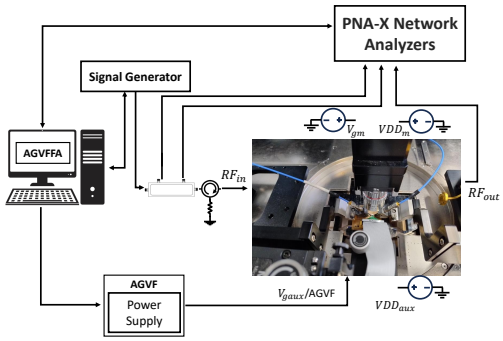

Fig. 5. Measurement set-up for auxiliary class-C and AGVF biasing.

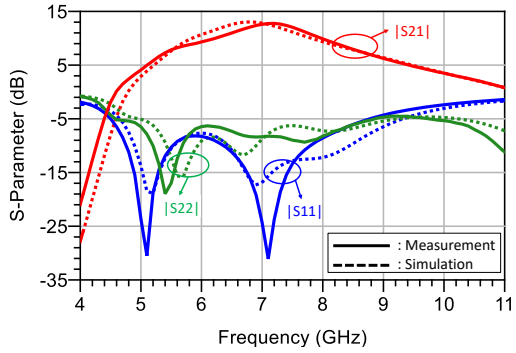

Fig. 6. DPA S-parameter, A comparison between simulation (dash line) and measurement (solid line).

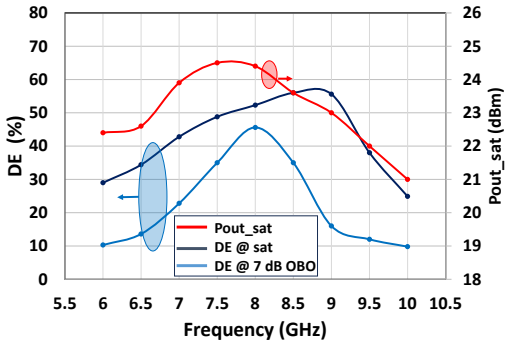

Fig. 7. Saturated output power, DE at saturation and 7 dB OBO over frequency range from 6 to 10 GHz, DE more than 30% at 7 dB OBO over the frequency range from 7.2 to 8.7 GHz, which is equal to 1.5 GHz BW, 18.9 % FBW.

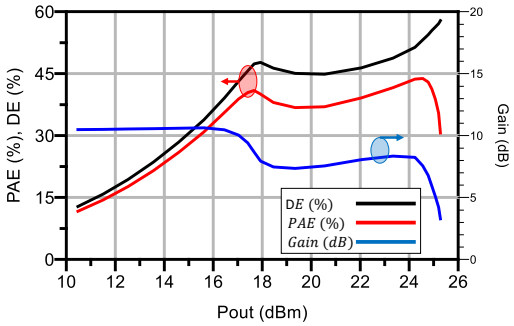

Fig. 8. Large signal performance under single tone CW signal at 8 GHz.

III. DPA Characterization and Auxiliary Gate Voltage Function Finder Algorithm

A. DPA Characterization

The Doherty Power Amplifier implemented in this work employs an asymmetric configuration and achieves an OBO performance greater than 7 dB. Fig. 5 presents the measurement setup and on-wafer probe measurements performed under the following bias condition for the chip: V_{dd} = 4V (I_{DQ} = 19.7 mA), V_{gm} = 0.42 V and V_{gaux} = 0 V.

The DPA is characterized using DC and small-signal simulations, as well as measurements from 4 to 11 GHz. The S-parameter comparison between simulation and measurement is shown in Fig. 6. Good agreement is observed between simulation and measurement for the small signal S-parameters of the DPA over the 4 to 11 GHz frequency range. The small-signal gain exceeds 9 dB from 6 to 8.3 GHz, with a peak gain of 12.8 dB at 7.3 GHz.

The DPA characterized under large signal CW single-tone excitation using two different biasing conditions for the auxiliary device. In the first condition, the main amplifier operates in Class-AB with V_{gm} = 0.42 V (I_{DQ} = 19.7 mA), while the auxiliary amplifier is biased in Class-C with V_{gaux} = 0 V, ensuring efficient operation across varying power levels.

The large signal performance of the DPA from 6 to 10 GHz in 500 MHz increments, including output power (dBm), DE (%) at saturation, and 7 dB OBO depicted in Fig. 7. The DPA achieves a DE greater than 30 % at 7 dB OBO over the frequency range from 7.2 to 8.7 GHz, which is equal to 1.5 GHz BW or 18.9 % FBW. At saturation, the output power exceeds 23.5 dBm and the DE remains above 45 % across this frequency range.

In Fig. 8, large signal performance of the DPA shows the power gain and power added efficiency (PAE) at 8 GHz. The results demonstrate a power gain of 10.6 dB at the BOR, a saturated output power of 24.5 dBm with a PAE and DE of 44.5 % and 58.3 %, respectively. At 7 dB OBO, the PAE and DE reach 41.7 % and 48.5 %, respectively. However, the gain compression from 7 dB OBO to saturation exceeds 3 dB. To address this gain degradation, an external auxiliary gate voltage function proportional to the input power is applied to the gate of the auxiliary amplifier.

B. Auxiliary Gate Voltage Function Finder Algorithm

In the second bias condition, the auxiliary gate voltage is swept from 0 V (Class-C) to 0.42 V in 0.02 V increments at each input power level, while measuring the corresponding gain and efficiency of the DPA.

The target gain is first determined based on the DPA performance in the low output power region, which serves as the reference. To improve linearity of the DPA, we define a maximum allowable gain variation of 1 dB within the SR. In contrast, a conventional DPA with a fixed auxiliary gate voltage typically exhibits about 3 dB of gain compression in the same region. Thus, this technique yields an approximate 2

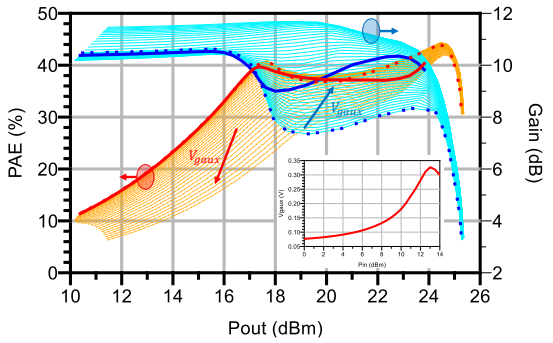

Fig. 9. Gain and efficiency of the DPA versus output power for various auxiliary gate voltages, ranging from 0 V (Class-C) to 0.42 V in 0.02 V steps. Solid thick lines represent the linearized gain (blue) and the corresponding PAE (red), while the dashed lines show the performance of the DPA with the standard V_{gaux} = 0 V.

dB improvement in linearity. To implement this improvement and find the auxiliary gate voltage function, we sweep the auxiliary gate voltage and collect gain and efficiency data across the output power range. The analysis is then constrained to only those gain and efficiency where the gain remains within the predefined 1 dB variation linear region. For each output power levels within this region, we identify the auxiliary gate voltage that provides the highest efficiency. This results in a dynamic gate voltage profile that ensures improved linearity while maintaining optimal efficiency, as shown in Fig. 9. Since the efficiency values corresponding to the linear gain region are filtered, the auxiliary gate voltage function is identified using the maximum efficiency at each output power level and selects the associated gate voltage. In this manner, the optimal auxiliary gate voltage function ensures a 1 dB gain variation in the linear region while maximizing efficiency. Once the auxiliary gate voltage function is established, it can be implemented in hardware using envelope detector circuits. These circuits generate the desired gate voltage function by sampling the input power, which is extracted via a RF coupler, thereby enabling practical DPA linearization. In table I, the DPA with standard auxiliary gate voltage bias performance and comparison with similar prior works are summarized.

TABLE I
COMPARISON WITH OTHER GAAS MMIC DPAS.

	[1]	[7]	This work
Technology	GaAs 250 nm	GaAs 250 nm	GaAs 180 nm
Architecture	Asym. DPA	LMBA	Asym. DPA
Frequency (GHz)	4.3–6	4.2–5.2	7.2–8.7
FBW (GHz / %)	1.7 / 33	1 / 21.1	1.5 / 18.9
P_{sat} (dBm)	29.4–30.4	30.2–31.8	24–24.5
DE at SAT (%)	46.4–57.1	34.3–52.9	46–58.3
OBO (dB)	9	6	7
DE at OBO (%)	31–43	27.7–40.4	30–46
Chip Size (mm×mm)	1.8 × 1.35	2.6 × 1.8	2.5 × 2

IV. CONCLUSION

In this work, the successful implementation of a FR3 6G mid-band GaAs MMIC DPA incorporating AGVF bias to improve the linearity of DPA at saturation of the main amplifier is presented. The DPA achieves a peak output power of 24.5 dBm, a large signal gain of 10.5 dB at BOR, and a drain efficiency of 58.3% at saturation. In conclusion, the AGVF applied to DPA demonstrates a significant improvement in gain performance compared to the standard DPA at 8 GHz. The gain compression observed between 7dB OBO and peak output power exceeds 3 dB in the standard DPA. In contrast, the AGVF DPA exhibits reduced gain compression, remaining below 1 dB. This enhancement highlights the effectiveness of the dynamic gate bias technique in improving linearity and mitigating gain compression of the main amplifier in SR. The use of lumped component in the designing Doherty output network and input network ensures the compact MMIC implementation. These findings confirm the viability of this approach for future high-performance, energy-efficient III-V power amplifiers.

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