Ultra-Broadband Frequency Multiplier (x8) Chain in 90-nm SiGe BICMOS Technology at H-Band

Ultra-Broadband Frequency Multiplier (x8) Chain in 90-nm SiGe BiCMOS Technology at H-band

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***Abstract*— This work presents an H-band (220–325 GHz) frequency octupler realized in a 90-nm SiGe BiCMOS process. The 3-dB bandwidth is between 234–305 GHz, resulting in a fractional bandwidth of 26.3 %. The multiplier achieves a conversion gain between 230–310 GHz. The peak output power is −0.5 dBm, using an input power of −5 dBm. The DC power consumption is 122 mW. This type of circuit is suitable for future communication and radar systems.**

***Keywords*— 220–325 GHz, Broadband, Frequency multiplier, H-band, Octupler, SiGe, x8**

I. Introduction

High data rate communication and radar systems are actively taking advantage of the development of semiconductor processes, which support increasing frequencies. The millimeter wave spectrum offers more bandwidth and higher resolution, but struggles with output power. The oscillator design is especially cumbersome at 200+ GHz, which is why frequency multipliers are usually used. Successful high frequency low power multipliers in InP DHBT/HEMT technology have been presented in [1] [2]. However, for large-scale commercial production, silicon technologies are preferred, due to cost and yield. In [3], a 40-nm CMOS x9 multiplier is presented that covers 213 to 233 GHz. For larger bandwidths and higher frequencies, there are several SiGe BiCMOS solutions [4] [5] [6] [7] [8] [9], showing the potential of high-frequency SiGe BiCMOS multipliers. High output power can be achieved, but requires high DC power consumption. For low DC power consumption, the fractional bandwidth is limited. For large fractional bandwidth, the output power is limited.

In this work a power efficient, broadband H-band (220–325 GHz) SiGe BiCMOS octupler is presented. It achieves a conversion gain between 230 and 310 GHz, and the 3-dB bandwidth is between 234 and 305 GHz. The peak output power is −0.5 dBm, and only −5 dBm is needed to drive the frequency multiplier.

II. Circuit Design

The frequency multiplier is designed and manufactured using a 90-nm SiGe BiCMOS process (B12HFC) developed by Infineon technologies. The process includes high-speed npn HBTs with f_t/f_{max} of 300 GHz/500 GHz [10]. The frequency multiplier consists of two cascaded frequency doublers, followed by a two-stage buffer amplifier and a last-stage frequency doubler. The circuit block diagram can be seen in Fig. 1.

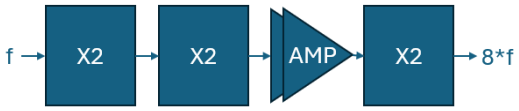

Fig. 1. Simple block diagram of the frequency multiplier.

The first two doublers in the multiplier chain use the same topology. The simplified schematic is shown in Fig. 2. It is a class-B biased emitter coupled pair which is differentially fed. The differential signal is created using a passive folded Marchand balun. The combined waveform from the collectors is rich in the second harmonic, while the fundamental and uneven harmonics are ideally canceled out. The output of the combined collectors is fed to the emitter of a cascoded transistor to achieve a higher output power. Both input and output are stub matched to 50 Ω to enable easy integration. The size of the transistors of the first emitter coupled pair and the cascoded transistor is 8 μm. The second stage also has 8 μm transistors, but in this case two base fingers are chosen instead of one. This is done to slightly increase the output power while keeping the design energy efficient.

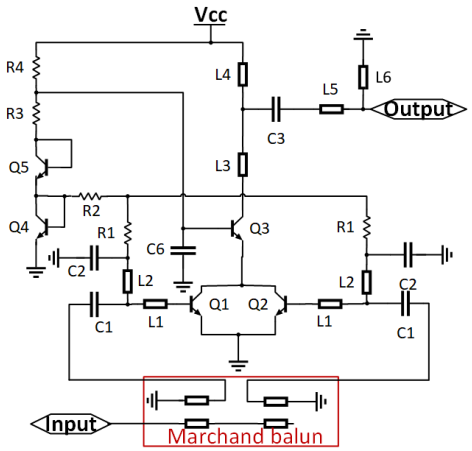

Fig. 2. Simplified schematic of the doublers used in the first two stages.

The D-band buffer amplifier is based on a two-stage common emitter topology. The simplified schematic is shown in Fig. 3. The interstage matching has high pass characteristics, to achieve a wideband flat gain, covering the entire D-band. The emitter size of both transistors is 8 μm.

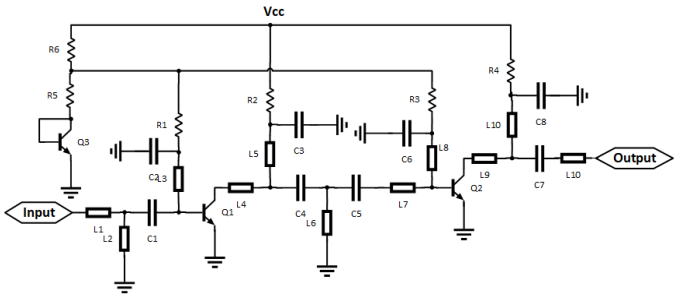

Fig. 3. Simplified schematic of the two stage D-band buffer amplifier.

The doubler of the last stage uses a similar design as the first two, excluding the cascoded transistor (Fig. 4). For the upper part of the H-band such a configuration will not provide any gain (f_t = 300 GHz in this process). The size of the transistors of the emitter coupled pair is 4 μm. All stages in the multiplier chain use internally biased bases, through diod and resistor stacks.

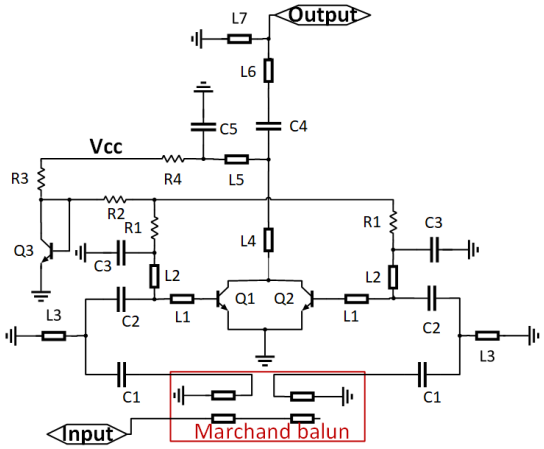

Fig. 4. Simplified schematic of the last stage H-band doubler.

The combined circuit was simulated using Cadence. In Fig. 5, a harmonic balance simulation of the first eight harmonics of the multiplier is shown. The HiCUM model was used and the input power of the multiplier is -5 dBm. The suppression of unwanted harmonics is more than 25 dB.

In Fig. 6, a photo of the frequency octupler can be seen, with the input to the left and the output to the right. The circuit is using two different DC-bias (2.4 V and 1.8 V), corresponding to first-stage doublers and buffer amplifier/last-stage doubler. The size of the circuit including the pads is 580 μm $\times$ 1250 μm, resulting in an area of 0.725 mm^2.

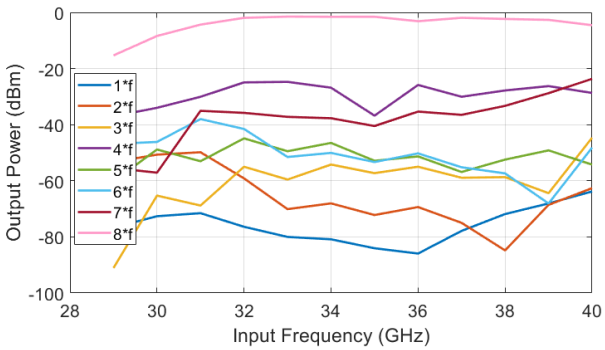

Fig. 5. Simulated harmonics of the frequency multiplier. The input power is -5 dBm.

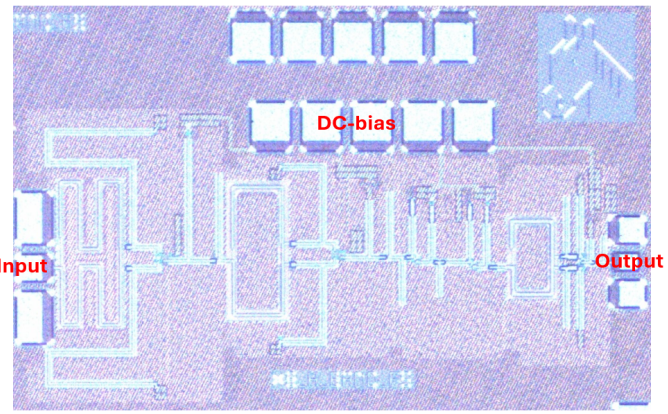

Fig. 6. Photo of the fabricated frequency octupler. The size of the circuit is 580 μm $\times$ 1250 μm including pads.

III. Measurement Results

The frequency multiplier was evaluated on-wafer using a probe station (MPI TS200 and Cascade MPS150). The input matching of the multiplier and the D-band buffer amplifier, as well as the D-band balun was measured using a Anritsu VectorStar (ME7838G) broadband VNA. The measured and simulated input matching can be seen in Fig. 7.

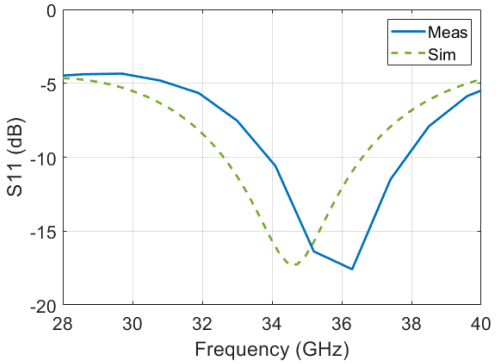

Fig. 7. Measured and simulated input matching.

In Fig. 8, the S-parameter measurements of the buffer amplifier are shown. The buffer amplifier's maximum

conversion gain was 7.4 dB, and the 3-dB bandwidth was between 108 and 170 GHz, thus covering the entire D-band.

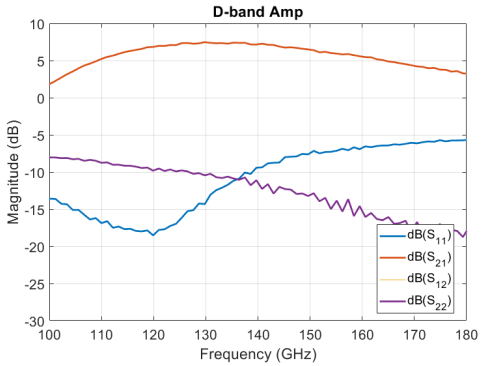

Fig. 8. Measured conversion gain of the D-band buffer amplifier.

The insertion loss and phase balance of the D-band Marchand balun (a breakout) used at the last stage doubler was also measured. The phase/amplitude imbalance was less than 3.5 degrees and 1.2 dB for the entire D-band. The measurement can be seen in Fig. 9.

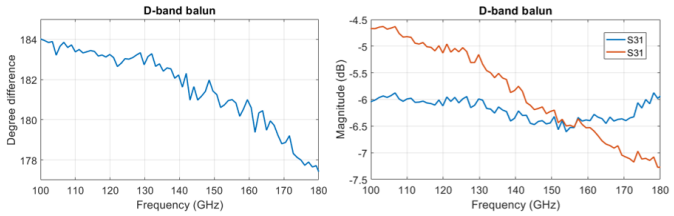

Fig. 9. Measured insertion loss and phase balance of the D-band balun, used before the last stage of multiplication.

The multiplier's output power was measured using a Keysight PNA-X (67 GHz N5247A). The input signal (-5 dBm) was connected using a coaxial cable and a 67 GHz GGB probe. The output signal was connected through an Infinity probe (I67) and a VDI extender (WR 3.4) to the PNA-X. The measured and simulated output of the 8th harmonic can be seen in Fig. 10. The measured 3-dB bandwidth is between 234 and 305 GHz, and the multiplier achieves a conversion gain between 230 and 310 GHz. That corresponds to a 3-dB fractional bandwidth of 26.3%. The peak output power is -0.5 dBm. The measurement and simulation agree on the output power. However, the frequency is shifted down $\approx$ 10 GHz, which corresponds to less than 4%.

The output power of the octupler was measured for varying input power, between -9 and -1 dBm. In Fig. 11, the result for 230, 260, 280, 290, 300 and 310 GHz can be seen. An input power of -5 dBm is enough to saturate the multiplier. 290 GHz has the highest output power, and 260 GHz is saturated for the entire sweep.

The total DC power consumption for the octupler is 122 mW, and the maximum conversion gain is 4.5 dB.

The unwanted harmonics were characterized (Fig. 12) in the same way as the 8th harmonic. The 9th, 7th and 6th harmonic was measured using the same extender (WR 3.4).

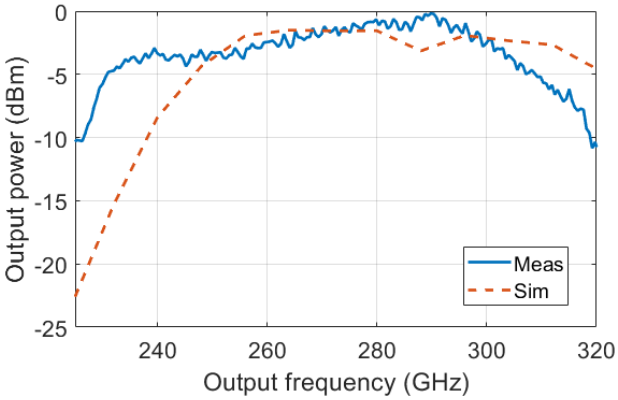

Fig. 10. Measured and simulated output power of the 8th harmonic. The input power was -5 dBm.

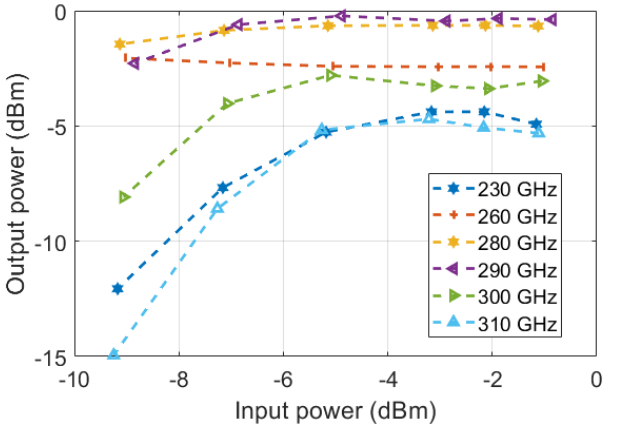

Fig. 11. Measured output power vs input power for different frequencies.

The 5th harmonic was measured using a WR 5.1 extender and the corresponding probe. The 4th harmonic was also measured with the WR 5.1 extender, as well as with a WR 8.0 extender. The 3rd harmonic used the WR 8.0 extender, and the 2nd harmonic used WR 12.0. The fundamental tone was measured using a 67 GHz infinity probe. The input power was -2 dBm, which is double the input power required for the octupler.

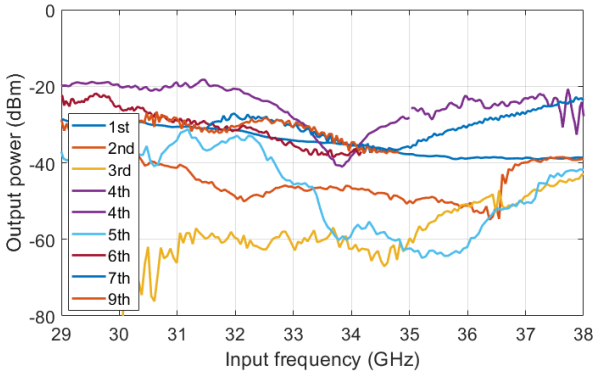

Fig. 12. Measured power of the unwanted harmonics harmonic. The input power was -2 dBm.

Table 1. Comparison with other 200+ GHz frequency multipliers in SiGe BiCMOS

Reference	[4]	[5]	[6]	[7]	[8]	[9]	**[this work]**
f_t / f_{max}	250/370	350/450	350/450	470/650	350/450	470/650	**300/500**
Frequency (GHz)	210–291	281–320	245–295	244–300	212–260	238–278	**234–305**
Multiplication factor	8	4	8	9	4	6	**8**
Fractional bandwidth (%)	32.3	13.0	18.5	20.7	20.3	15.5	**26.3**
P_{sat} **(dBm)**	-7.7	2.5	-5	9.6	5.5	4.3	$\mathbf{-0.5}$
Harmonic suppression (dB)	>22.3	N/A	>25	>30	>20*	>20	**>18**
DC power (mW)	240	384	125	660	270	119	**122**

*simulated value

IV. Conclusion

In this work, an H-band octupler in a SiGe BiCMOS technology is designed and evaluated. In Table 1 the circuit is compared with other 200+ GHz SiGe BiCMOS multipliers. It achieves the second largest fractional bandwidth, with almost half the DC power consumption and more than 4 times the output power. The frequency multiplier only needs -5 dBm input power and has a maximum conversion gain of 4.5 dB. It has a 3-dB bandwidth that covers more than 70 GHz. Furthermore, it is area efficient using only 0.725 mm^2. The circuit is an excellent candidate for energy efficient, ultra-broadband H-band communication and radar systems.

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