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Fabrication and development of InP HEMTs on silicon substrate based on a new integration technique

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***Abstract*—Current methods for transferring III-V technology onto silicon are based on wafer bonding techniques. Here we explore fabrication applicability of traditional InP-based High Electron Mobility Transistors (InP HEMTs) on InP-on-Si (InPoSi) wafers developed by Smart Cut, a method for transferring InP onto Si that reduces cost and fabrication complexity. We fabricated 100-nm gate length InP HEMTs, including test structures and Hall bars on both InPoSi and InP wafers. Transfer Length Method (TLM) measurements for InPoSi and InP bulk wafers showed comparable contact and sheet resistances. These preliminary results show that InP HEMTs can be fabricated on InPoSi.**

I. Introduction

For high-speed electronics, the integration of III-V's on silicon is a solution for mass production of monolithic millimeter-wave integrated circuits.

Previous studies on III-V transistors integrated on silicon have demonstrated preserved performance of III-V field effect transistors with the benefit of the silicon substrates [1, 2, 3], however, these approaches have an increased fabrication complexity that include back-etching and are limited to small wafer diameters.

In this work, we explore InP High-Electron-Mobility Transistors (HEMTs) on an InP-on-Si substrate (InPoSi) which is obtained by Smart Cut process, an approach which sustainably re-uses InP wafers multiple times, transferring a thin crystalline layer of InP onto a silicon substrate [4]. We present and analyze the contact and sheet resistances through the fabrication of TLM (Transfer Length Method) structures. HEMTs and Hall bars were also fabricated on the same chip and are undergoing full characterization. The TLM measurements show encouraging progress on the development of the InPoSi HEMTs.

II. Fabrication

Through the Smart Cut process, a SiO_2 layer is formed on a "receiver" Si substrate and a thin "donor" bulk InP is then bonded to the substrate through wafer bonding. Hydrogen ion implantation splits a thin InP layer from the donor, giving an InPoSi substrate and at the same time allowing the possibility to re-utilize the InP wafer [4].

A HEMT epitaxial structure was then grown by MOCVD (Metal-Organic Chemical Vapor Deposition) both on an InPoSi substrate fabricated through Smart Cut process and on a InP bulk substrate (see a schematic representation of the HEMT epitaxy on InPoSi in Fig. 1).

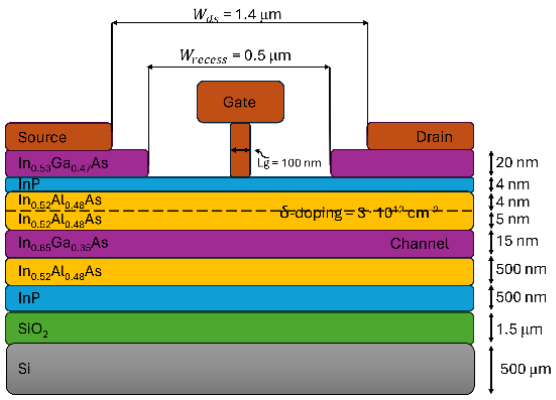

Fig. 1. Cross-sectional schematic of the HEMT on InPoSi substrate showing the epitaxial structure (not to scale).

HEMTs, TLM structures and Hall bars were fabricated side-by-side on InPoSi wafer and InP bulk, following the fabrication process previously reported here [5].

III. Results

No major challenges arose when applying our traditional InP HEMTs fabrication process to the InPoSi wafer. To account for the different substrate electrical and thermal properties, the exposure dose for electron-beam lithography and contact annealing needed to be adjusted for the InPoSi substrate. The TLM structures with different pad distances were analyzed assuming a linear relation between resistance and pad distance. The TLM measurements were performed using four-point Kelvin probes on two structures per sample, see Fig. 2. The results in Fig. 3 show comparable sheet resistance for InPoSi and InP wafers, with average values of 62 Ω/□ and 68 Ω/□ respectively. The contact resistance obtained on the InPoSi substrate was lower than the one on the InP bulk, with values of 0.02 Ω·mm and 0.06 Ω·mm, respectively. However, it must be noted that this difference lays within fabrication variability and that different annealing conditions were used for InP and InPoSi.

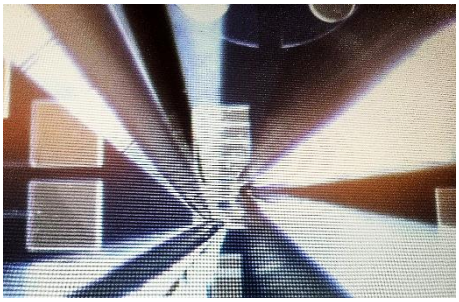

Fig. 2. Microscope picture of a fabricated TLM structure on InPoSi with the different pad distances under measurement.

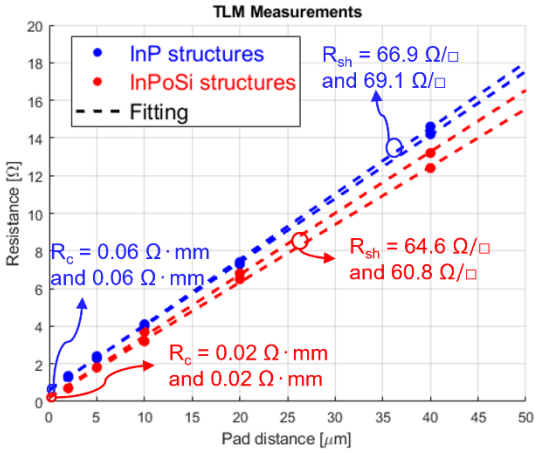

Fig. 3. TLM measurements of HEMT epitaxy on InP and InPoSi substrates. Two structures were measured for each substrate and extracted parameters are marked.

IV. Summary

In this work, we investigated the applicability of InPoSi wafers fabricated with a novel wafer transfer technique, Smart Cut, for the fabrication of InP HEMTs. Compared to the fabrication on InP substrate, only electron-beam lithography dose and annealing recipe of ohmic contacts needed to be calibrated for the InPoSi substrate. Moreover, TLM measurements showed comparable contact and sheet resistances for the InPoSi sample compared to InP bulk. While waiting for the on-going complete analysis of the fabricated Hall bars and HEMTs, shown in Fig. 4, the presented results show promising prospects of InP-based HEMTs fabricated on InPoSi wafers.

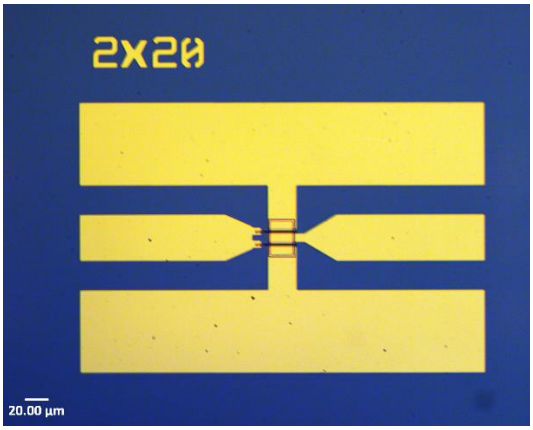

Fig. 4. Microscope picture of a fabricated 2x20 μm InPoSi HEMT showing the intrinsic two-finger device, together with pads for RF probing.

V. Acknowledgements

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References

[1]. J. Jeong et al., "Stackable InGaAs-on-Insulator HEMTs for Monolithic 3-D Integration", *IEEE Transactions on Electron Devices*, 68(5), 2205-2211, 2021.

[2] F. Heinz et al., "W-Band Low-Noise-Amplifier MMICs in InGaAs HEMT Technologies on Gallium-Arsenide and Silicon Substrates", *IEEE MTT-S IMS*, 2024.

[3]. A. Leuther et al., "InGaAs HEMT MMIC Technology on Silicon Substrate with Backside Field-Plate", *2020 50th European Microwave Conference*, 2020.

[4]. B. Ghyselen et al., "Large-Diameter III–V on Si Substrates by the Smart Cut Process: The 200 mm InP Film on Si Substrate Example", *Physica Status Solidi,* 2022.

[5]. E. Cha et al., "Two-Finger InP HEMT Design for Stable Cryogenic Operation of Ultra-Low-Noise Ka- and Q-Band LNAs", *IEEE T-MTT*, pp. 5171-5180, December 2017.