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***Abstract*—The Full-Bridge Double-Wye Modular Multilevel Converter (FB-YY-MMC) offers enhanced flexibility for grid applications, particularly in renewable energy integration. This paper investigates the effects of key degrees of freedom, including pole-to-pole DC voltage, second-order circulating current, and third-order zero-sequence voltage, on the converter's design. For this purpose, a cost function is introduced to combine all relevant design parameters, such as the number of submodules, power losses, semiconductor ratings, and submodule capacitor size, by assigning a weighting factor to each. The optimization process minimizes this cost function to determine the optimal design. As a result, it is shown that a 17% reduction in the overall cost of the MMC is achieved compared to a conventional design. Also, the proposed optimization approach is validated through time-domain simulation.**

***Index Terms*—modular multilevel converter (MMC), converter design optimization, full-bridge submodules, MMC circulating current injection, zero-sequence voltage injection**

I. Introduction

The Modular Multilevel Converter (MMC) is known for its high efficiency, excellent dynamic performance, and robustness in weak grid conditions [1]. The Energy Storage (ES)-connected double-wye MMC (YY-MMC) has been deployed in grid applications, particularly to support the integration of renewable energy sources [2]. In a YY-MMC, each phase-leg consists of upper and lower arms, with multiple series-connected submodules (SMs) in each arm. These SMs can be implemented as either half-bridge (HB) or full-bridge (FB) converters, resulting in HB-YY-MMC and FB-YY-MMC topologies, respectively.

The YY-MMC presents challenges due to its high number of components but offers some degrees of freedom depending on the SM type, and can be used for optimization in terms of cost or size. In the FB-YY-MMC, the pole-to-pole DC voltage can be freely selected, unlike in the HB-YY-MMC, where it is constrained by the AC grid voltage. This flexibility enables optimization of the FB-YY-MMC. For example, [3] investigated the optimization of the SM capacitor in the FB-YY-MMC by tuning the pole-to-pole DC voltage and concluded that the capacitor size can be reduced by up to 26% compared to the HB-YY-MMC.

Beyond the pole-to-pole DC voltage, other degrees of freedom in the YY-MMC design include the amplitude and phase of the second-order circulating current, as well as the amplitude and phase of the third-order zero-sequence voltage. These variables can be tuned to further optimize the converter's design. For instance, prior works [4]–[6] have explored the injection of circulating current and zero-sequence voltage to optimize specific design parameters, such as SM capacitor size or converter losses. However, these studies do not consider the pole-to-pole DC voltage as a tunable parameter. Similarly, while [7] includes both the pole-to-pole DC voltage and second-order circulating current as optimization variables, it does not treat third-order zero-sequence voltage as a tunable parameter and focuses only on individual design parameters, such as minimizing SM capacitor size. Moreover, existing research does not analyze the trade-offs between multiple key design parameters, such as the number of SMs, capacitor size, power losses, and semiconductor ratings, in a unified framework. Additionally, the literature provides limited analysis of the various approaches for incorporating third-order zero-sequence voltage into the upper and lower arms of the YY-MMC, which impacts the converter's internal current and voltage and will lead to different design requirements. A comprehensive optimization approach that captures these variables and their interactions is thus still needed.

This paper examines the impact of pole-to-pole DC voltage,

second-order circulating current, and zero-sequence voltage on the overall design of the FB-YY-MMC, considering key design parameters such as the number of SMs, losses, semiconductor rating, and SM capacitor size. It introduces a cost function that integrates these factors and optimizes it to achieve the most cost-effective FB-YY-MMC design.

The remainder of this paper is organized as follows. Section II presents the FB-YY-MMC topology and its dynamic behavior. Section III outlines the key design parameters considered in the study. Section IV introduces the proposed design optimization framework, including the formulation of the cost function and decision variables. Section V discusses the simulation results used to validate the optimization approach. Finally, conclusions are drawn in Section VI.

II. FB-YY-MMC TOPOLOGY AND DYNAMICS

The grid-connected FB-YY-MMC is depicted in Fig. 1. Since the FB-YY-MMC is intended for grid-connected Energy Storage (ES) applications, an ES unit with a pole-to-pole DC voltage V_{DC}, is connected to the converter's DC side. The FB-YY-MMC consists of three phase-legs, each containing an upper and a lower arm. Each arm includes N series-connected FB SMs along with a filter reactor characterized by an inductance L and resistance R. The voltages and currents of the upper and lower arms are represented by v_{u}, v_{l}, i_{u}, and i_{l}, respectively. The AC side is connected to a Δ/Y transformer, where the phase voltage on the Δ side is denoted as v_{g}.

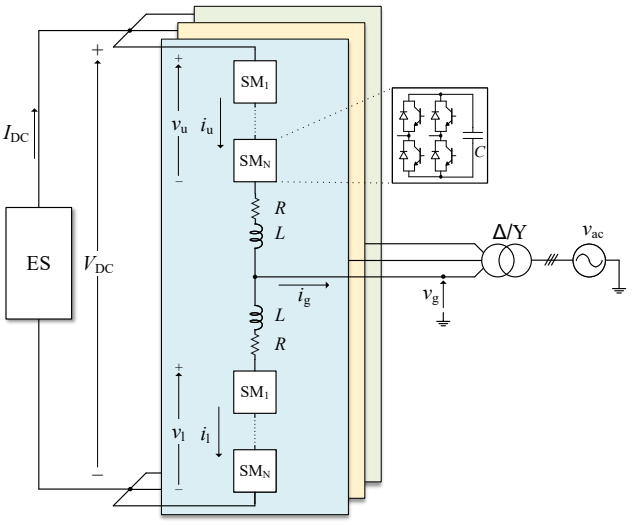

Fig. 1. Grid-connected FB-YY-MMC scheme.

The currents in the upper and lower arms of a generic phase can be expressed as:

$$i_{\mathrm{u,l}} = \pm\frac{i_{\mathrm{g}}}{2} + i_{\mathrm{cc}} \tag{1}$$

where i_{g} represents the current exchanged between the converter and the grid, while i_{cc} denotes the circulating current flowing between the phase-legs and the common DC link of the converter. Under steady-state operations, the circulating current consists of a DC component, which is one-third of the DC current supplied by the ES (I_{DC}), along with even-order harmonics arising from the phase difference between the voltage ripples of the upper and lower arm capacitors. The circulating current is primarily dominated by the second-order harmonic components, while other harmonics have significantly smaller amplitudes [8]. Therefore, this analysis considers only the DC component and the second-order harmonic. Assuming that i_{g} is a pure sinusoidal signal at fundamental frequency, with amplitude I_{g}, and phase φ_{ig}, the arm currents in (1) are given by:

$$i_{\mathrm{u,l}} = \pm\frac{I_{\mathrm{g}}}{2}\cos(\omega t + \varphi_{\mathrm{ig}}) + \frac{I_{\mathrm{DC}}}{3} + I_{\mathrm{c2}}\cos(2\omega t + \varphi_{\mathrm{c2}}) \tag{2}$$

where I_{c2} and φ_{c2} are the amplitude and phase of the second-order harmonic of the circulating current, respectively. The second-order circulating current is typically suppressed by a circulating current controller (CCC) to minimize losses and reduce the semiconductor rating. However, in this study, this current component will be treated as a controllable variable to optimize the design of the FB-YY-MMC.

The upper and lower arm voltages are also determined as:

$$v_{\mathrm{u,l}} = \frac{V_{\mathrm{DC}}}{2} \mp v_{\mathrm{s}} + v_{\mathrm{cc}} \tag{3}$$

where v_{s} is the converter's output AC voltage behind the filter, and v_{cc} is the voltage that drives the circulating current and its reference comes from the CCC. As v_{cc} is significantly lower than V_{DC} and v_{s} [8], it can be neglected in this analysis. From (3), the output voltage as a function of the upper and lower arm voltages is thus found to be:

$$v_{\mathrm{s}} = \frac{v_{\mathrm{l}} - v_{\mathrm{u}}}{2} \tag{4}$$

III. FB-YY-MMC DESIGN PARAMETERS

This section provides a brief introduction to the key design parameters that have the greatest impact on the per-unit cost of the converter [9], namely the number of SMs (N), power losses (P_{l}), semiconductor rating ($\hat{I}_{\mathrm{n}}$), and SM capacitor size (C).

A. Number of submodules

The number of SMs in the converter is determined by dividing the maximum value of the upper and lower arm voltages by the rated SM voltage ($V_{\mathrm{SM,n}}$), as follows:

$$N = \mathrm{ceil}\left(\frac{\max(v_{\mathrm{u,l}})}{V_{\mathrm{SM,n}}}\right) \tag{5}$$

B. Power losses

The total power losses in the FB-YY-MMC comprise of the conduction losses (P_{co}), switching losses (P_{sw}), filter losses (P_{fi}), and capacitance losses (P_{ca}). A more detailed breakdown, including explanations and equations for the losses, is provided in [7].

Conduction losses result from voltage drops and internal resistance in transistors and diodes, depending on current magnitude and SM operating state. Switching losses arise from state transitions in SM transistors and diodes, influenced by the current at the switching instant and modulation technique. Here, essential switching losses as defined in [10] under nearest level modulation are considered.

Filter losses are due to the resistance of the filter reactor (R) and depend on the arm current. Capacitance losses stem from the SM capacitor's Equivalent Series Resistance (ESR) and are found using averaging principle as explained in [9]. The total converter losses are:

$$P_{\mathrm{l}} = P_{\mathrm{co}} + P_{\mathrm{sw}} + P_{\mathrm{fi}} + P_{\mathrm{ca}} \tag{6}$$

C. Semiconductor rating

The semiconductor's rated current is defined by the absolute peak of the current flowing through the semiconductor, which is the arm current. As a result, it is determined to be:

$$\hat{I}_{\mathrm{n}} = \max\left(|i_{\mathrm{u,l}}|\right) \tag{7}$$

D. Submodule capacitor size

The size of the SM capacitor is determined by calculating the peak-to-peak variation of the arm energy and setting a limit on the allowed capacitor voltage ripple (ΔV). The arm energy variation is obtained by integrating the product of the arm voltage, given in (3), and the arm current, given in (2). For an output voltage of $v_{\mathrm{s}} = V_{\mathrm{s}}\cos(\omega t)$, the arm energy variation is expressed as:

$$w_{\mathrm{u,l}} = \int_T v_{\mathrm{u,l}} i_{\mathrm{u,l}}\, dt \tag{8}$$

Defining peak-to-peak value of the variation of the arm energy as:

$$W_{\mathrm{u,l}} = \max(w_{\mathrm{u,l}}) - \min(w_{\mathrm{u,l}}) \tag{9}$$

The SM capacitance is subsequently determined as:

$$C = \frac{W_{\mathrm{u,l}}}{N\Delta V V_{\mathrm{SM,n}}^2} \tag{10}$$

IV. FB-YY-MMC Design optimization

The FB-YY-MMC design involves a multi-objective optimization problem, where the objective functions are the number of SMs (N), power losses (P_{l}), semiconductor rating ($\hat{I}_{\mathrm{n}}$), and SM capacitor size ($W_{\mathrm{u,l}}$ or C). This section defines the decision variables for this optimization and presents the cost function along with its weighting factors.

A. Decision variables

As discussed in Section II, the second-order circulating current amplitude (I_{c2}) and phase (φ_{c2}) are considered decision variables. Additionally, as noted in [7], unlike the HB-YY-MMC, where the pole-to-pole DC voltage must be at least $2V_{\mathrm{s}}$ due to the inability of HB SMs to generate negative voltage, this constraint does not apply to the FB-YY-MMC. As a result, the pole-to-pole DC voltage (V_{DC}) can also be treated as a decision variable for optimization.

Another decision variable examined here is the third-order zero-sequence voltage amplitude (V_3) and phase (φ_{v3}), which can be introduced into the upper and lower arm voltages. Under steady-state operations, assuming the FB-YY-MMC output voltage is given by $v_{\mathrm{s}} = V_{\mathrm{s}}\cos(\omega t)$, this zero-sequence voltage can be incorporated into the arm voltages in two ways: either with the same sign or with opposite signs, as shown below.

$$v_{\mathrm{u,l}} = \frac{V_{\mathrm{DC}}}{2} \mp V_{\mathrm{s}}\cos(\omega t) + V_3\cos(3\omega t + \varphi_{\mathrm{v3}}) \tag{11}$$

$$v_{\mathrm{u,l}} = \frac{V_{\mathrm{DC}}}{2} \mp V_{\mathrm{s}}\cos(\omega t) \pm V_3\cos(3\omega t + \varphi_{\mathrm{v3}}) \tag{12}$$

If (11) is applied, according to KVL a third-order zero-sequence circulating current in the phase-legs will flow, resulting in the arm current to be:

$$\begin{aligned} i_{\mathrm{u,l}} = \pm\frac{I_{\mathrm{g}}}{2}\cos(\omega t + \varphi_{\mathrm{ig}}) + \frac{I_{\mathrm{DC}}}{3} + I_{\mathrm{c2}}\cos(2\omega t + \varphi_{\mathrm{c2}}) \\ + I_{\mathrm{c3}}\cos(3\omega t + \varphi_{\mathrm{c3}}) \end{aligned} \tag{13}$$

where I_{c3} and φ_{c3} are the amplitude and phase of the third-order circulating current. However, according to (4), the third-order zero-sequence voltage is canceled in the output. With (12), KVL dictates no third-order zero-sequence circulating current, but (4) shows the presence of a third-order zero-sequence harmonic component in the output voltage. However, since the FB-YY-MMC is connected to a Δ/Y transformer, no third-order zero-sequence current will be injected into the grid.

The choice between the two third-order zero-sequence voltage injection methods significantly impacts various converter design parameters. Using (11) results in asymmetrical upper and lower arm voltages, which in turn leads to an overestimation of the required number of SMs. This asymmetry also causes the arm currents to differ in terms of peak values, leading to the need for a higher semiconductor rating. Furthermore, the energy variations between the upper and lower arms become asymmetrical, resulting in an overestimation of the required SM capacitor size. In contrast, the method in (12) ensures symmetrical upper and lower arm voltages, with odd-order harmonics having opposite signs (i.e., a 180° phase shift). This symmetry results in equal peak voltages and arm currents in both arms, eliminating the need for unnecessary over-design in SM count, semiconductor ratings, and capacitor size. Moreover, (12) avoids the introduction of additional circulating currents, as seen in (13), making it a more efficient choice by reducing power losses.

Thus, zero-sequence voltage injection using (12) proves to be the more effective method, as it maintains symmetry across arm voltages and currents, minimizing over-design in multiple design parameters, including the number of SMs, power losses, semiconductor ratings, and capacitor size.

B. Cost function

To minimize the FB-YY-MMC's cost through optimization, a per-unit cost function is defined based on the introduced key design parameters. This function assigns weighting factors to each parameter, reflecting their impact on the total converter cost. The cost function is defined as:

$$J = \alpha_0 + (\alpha_1 + \alpha_2)N + \alpha_3 N I_{\mathrm{n}} + \alpha_4 W_{\mathrm{u,l}} + \alpha_5 P_{\mathrm{l}} \qquad (14)$$

where

- α_0 is the weighting factor for fixed costs of the switching devices' mechanical base and basic cooling infrastructure.
- α_1 is the weighting factor for costs of the mechanical structure and additional cooling for individual SMs.
- α_2 is the weighting factor for costs associated with the building area required for each SM.
- α_3 is the weighting factor for semiconductor costs.
- α_4 is the weighting factor for SM capacitor energy storage costs, based on total peak-to-peak arm energy.
- α_5 is the weighting factor for lifetime power loss costs, estimated over 25 years using a typical cost per kW and typical operational load profiles.

The per-unit cost function and its associated weighting factors are formulated based on key cost components identified in the literature [11], [12], which provide a breakdown of converter cost contributions. While the specific weighting values used in this paper are guided by these references, they have been refined to better align with practical considerations, as shown in Table I.

TABLE I
COST FUNCTION WEIGHTING FACTORS

α_0 [pu]	α_1 [pu]	α_2 [pu]	α_3 [$\frac{\text{pu}}{\text{kA}}$]	α_4 [$\frac{\text{pu}}{\text{MJ}}$]	α_5 [$\frac{\text{pu}}{\text{kW}}$]
0.72	0.014	0.0184	0.0099	2.28	0.004

The cost function in (14) is optimized using the Particle Swarm Optimization algorithm [13], incorporating the weighting factors from Table I, while constraining V_{DC}, I_{c2} and V_3 to 2 pu, 0.25 pu, and 0.3 pu (considering V_{s} and $I_{\mathrm{g}}/2$ as the voltage and current base values), respectively. This optimization is performed for a grid-connected FB-YY-MMC with the specifications outlined in Table II, and since the values are in per-unit, they can be adjusted for other converter ratings as well. As shown in Fig. 2, the per-unit value of the cost function as well as the share of the each design parameter are presented for various scenarios in which the cost function is optimized using different decision variables or a combination of them. For example, the second bar labeled as V_{DC} indicates that the cost function is optimized by the pole-to-pole DC voltage only; similarly the full optimization means that all the decision variables are used in the optimization. It is important to note that the cost function is normalized to the base case, where the pole-to-pole DC voltage is 2 pu, and both the second-order circulating current and third-order zero-sequence voltage are set to zero. It is evident that full optimization reduces the cost function by 17%. Notably, optimizing solely the pole-to-pole DC voltage allows for a 13% reduction, highlighting the significant impact of this parameter on the overall optimization of the MMC.

TABLE II
THE CONVERTER SPECIFICATIONS AND BASE VALUES

Parameter	Symbol	Value
Line to Line Grid Voltage	V_{g}	33 kV
Grid Frequency	f	50 Hz
Rated Apparent (Base) Power	S_{b}	112 MVA
ES Rated Active Power	P_{n}	50 MW
Rated Reactive Power	Q_{n}	100 MVar
Arm Filter Inductance	L	4.64 mH
Arm Filter Resistance	R	72.83 mΩ
SM's max voltage ripple	ΔV	10%
SM's Capacitor Resistance	R_{c}	20 $\mu\Omega$
Semiconductor Breakdown Voltage	V_{bk}	4500 V
Semiconductor 100V FIT*	V_{100FIT}	2500 V
Semiconductor Rated Current	I_{n}	3000 A
Transistor On-state Voltage Drop	V_{ce}	0.8 V
Transistor On-state Resistance	R_{ce}	0.7 mΩ
Diode Forward Voltage	V_{f0}	0.9 V
Diode Forward Resistance	R_{f0}	0.4 mΩ

*Nominal voltage is chosen as the voltage corresponding to 100 FIT (100 failures in 10^9 operating hours)

V. SIMULATION RESULTS

To verify the analysis, a time-domain simulation model has been developed. The simulation model includes an arm-level averaged model of the YY-MMC, along with a control system, illustrated in Fig. 3.

In the averaged model, each arm of the FB-YY-MMC is represented by a controllable voltage source, while the combined effect of the SM capacitors in each arm is modeled using a current source and an equivalent capacitance of C/N. The relevant notations are summarized as follows:

- $v_{\mathrm{av,u}}$ and $v_{\mathrm{av,l}}$: Averaged voltages of the upper and lower arms, respectively.
- $i_{\mathrm{av,u}}$ and $i_{\mathrm{av,l}}$: Averaged currents of the upper and lower arms, respectively.
- $v^{\Sigma}_{\mathrm{cm,u}}$ and $v^{\Sigma}_{\mathrm{cm,l}}$: Sum of the measured capacitor voltages in the upper and lower arms.
- $i_{\mathrm{m,u}}$ and $i_{\mathrm{m,l}}$: Measured currents of the upper and lower arms.
- n_{u} and n_{l}: Insertion indices of the upper and lower arms, representing the average number of inserted SMs per arm.
- $V_{\mathrm{m,dc}}$: Measured pole-to-pole DC voltage.
- v_{cc}: Voltage reference generated by the current controller (CC).
- v_{ccc}: Voltage reference for circulating current control, generated by the CCC.

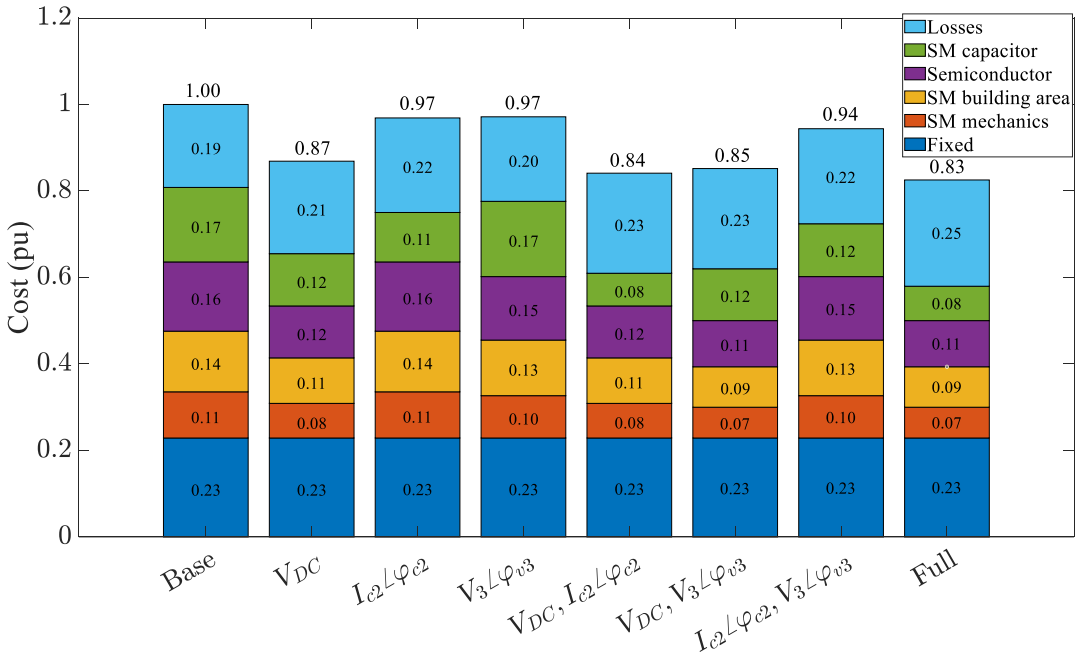

Fig. 2. Normalized cost function value for different scenarios and contribution of each design parameter in the total cost of the MMC.

- v_{cr}^{Σ}: Reference sum capacitor voltage, typically equal to NV_{n}, where V_{n} is the nominal voltage of each SM capacitor.

A full description of the model, including how the arm-averaged voltages and currents are calculated, as well as how the insertion indices are determined, can be found in [3].

The control system of the FB-YY-MMC comprises a reactive power controller (RPC), a DC-link voltage controller (DCVC), a CC, and a CCC. A detailed explanation of the control structure can be found in [3]. However, in contrast to [3], the reference value for the CCC is not set to zero but is determined through the proposed optimization process. Additionally, the third-order zero-sequence voltage is incorporated into the calculation of the insertion indices, which represents another difference from the control system presented in [3]. In this model, the number of SMs, the SM capacitor, and the pole-to-pole DC voltages are set to at 24, 20 mF, and 1 pu respectively, for all operating points. The remaining parameters are listed in Table II.

To assess the effectiveness of the proposed optimization approach, three key design parameters are analyzed: the number of SMs, determined by the arm peak voltage, the semiconductor rating, dictated by the arm peak current, and the SM capacitor size, which is closely related to the sum capacitor voltage ripple. Their relationships with the decision variables I_{c2}, φ_{c2}, V_3, and φ_{v3} are examined. However, their dependence on V_{DC} is not considered here, as it was previously investigated in [7]. It should be mentioned that as verifying all possible points is impractical, the simulations examine a few representative cases to compare the proposed approach's impact on design parameters.

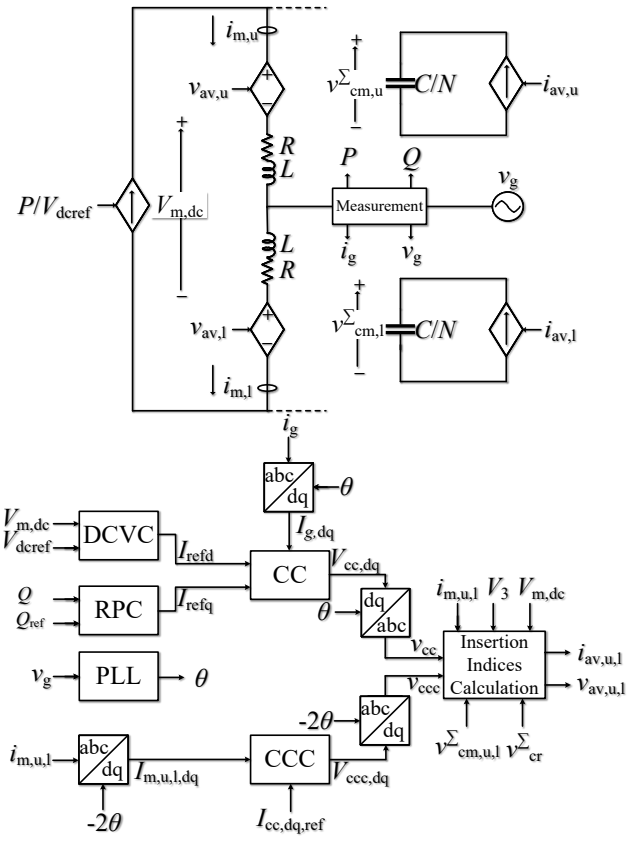

Fig. 3. The simulation model.

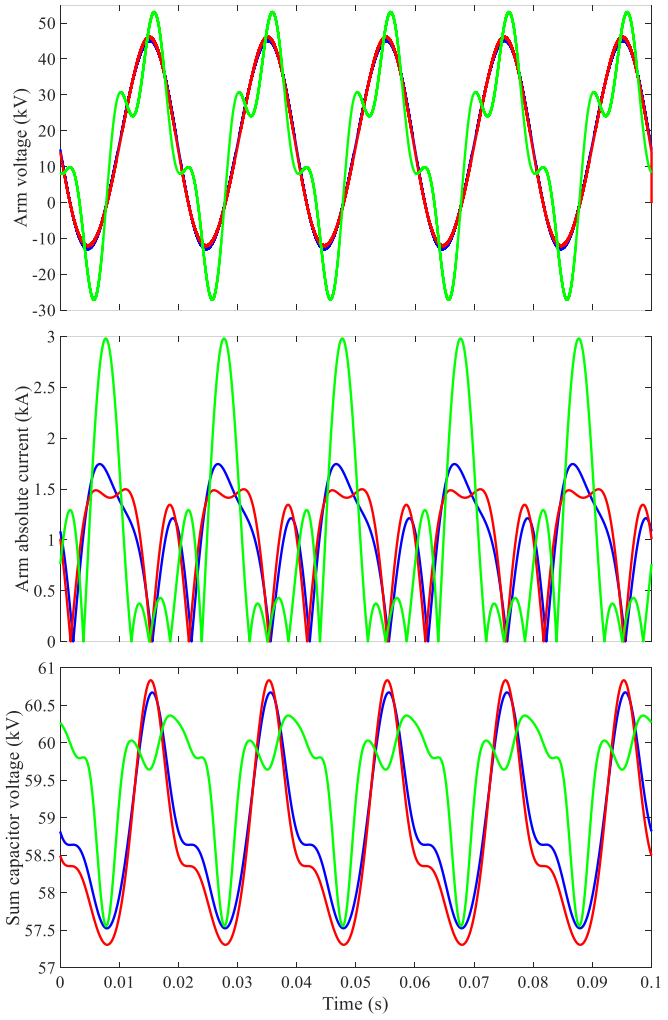

Fig. 4. Arm voltage (top), arm absolute current (middle), and sum capacitor voltage ripple (bottom) for optimization of N: $I_{c2}\angle\varphi_{c2} = 0$ $V_3\angle\varphi_{v3} = 0.17\angle 41°$ pu (blue), optimization of I_n: $I_{c2}\angle\varphi_{c2} = 0.23\angle 38°$ pu $V_3\angle\varphi_{v3} = 0$ (red), and optimization of C: $I_{c2}\angle\varphi_{c2} = 0.24\angle 273°$ pu $V_3\angle\varphi_{v3} = 0.29\angle 305°$ pu (green).

Fig. 4 illustrates the arm voltage, arm current, and the sum of the capacitor voltages for three different cases, where the number of SMs (N), the semiconductor rating ($\hat{I}_n$), and the SM capacitor (C) are optimized based on selection of I_{c2}, φ_{c2}, V_3, and φ_{v3}. From Fig. 4, it is evident that optimizing one design parameter can negatively impact others. For instance, minimizing the arm peak voltage (which reduces the required number of SMs) results in a higher sum capacitor voltage ripple, necessitating larger capacitors. Conversely, reducing the capacitor size leads to increased arm voltage, requiring more SMs. This trade-off highlights the need for a balanced optimization strategy as suggested by the cost function on (14).

VI. Conclusion

This paper has analyzed the impact of pole-to-pole DC voltage, second-order circulating current, and third-order zero-sequence voltage on the design an FB-YY-MMC. A detailed cost function was introduced to balance trade-offs between the number of SMs, losses, semiconductor rating, and capacitor size. The results indicate that optimizing these parameters achieves a 17% reduction in the overall converter cost. Notably, the pole-to-pole DC voltage alone contributes to a 13% cost reduction, highlighting its greater impact compared to the other two decision variables. Simulation results validate the optimization approach for the different design parameters.

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