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Bonding of micro LEDs using wet reflow process of indium bumps based on SU-8 solder mask

Shuangjia Bai [a], Taifu Lang [a], Xin Lin [a], Shuaishuai Wang [a], Zhihua Wang [a], Chang Lin [b], Qun Yan [a,*], Jie Sun [a,c,*]

[a] Fujian Science and Technology Innovation Laboratory for Optoelectronic Information of China, and College of Physics and Information Engineering, Fuzhou University, Fuzhou 350100, China

[b] Fujian Science and Technology Innovation Laboratory for Optoelectronic Information of China, Fuzhou 350100, China

[c] Quantum Device Physics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg 41296, Sweden

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ABSTRACT

This study proposes an innovative wet reflow process utilizing SU-8 photoresist as the solder mask for fabricating In bump arrays in Micro LED packaging. Conventional solder masks such as SiO_2 or metal layers involve complex processes, elevated temperatures, and limited compatibility with flexible substrates. In contrast, SU-8 enables mask patterning via single-step UV lithography, greatly simplifying fabrication and effectively reducing manufacturing complexity and cost. The optimized process achieved a 480 × 640 In bump array with excellent morphology: surface roughness (R_a) reduced from 0.65 μm to 0.126 μm, height non-uniformity improved from 4.8 % to 0.28 %, and shear strength increased nearly tenfold to 1.106 N. Using glycerol as an eco-friendly wet reflow medium facilitated oxide mitigation and enhanced bump uniformity and bonding reliability. The results demonstrate that this low-temperature, efficient, and scalable approach offers clear advantages for high-yield Micro LED integration, particularly in flexible and high-resolution display applications.

1. Introduction

With the rapid advancement of display technology, Micro LED has emerged as a core research focus for next-generation displays, owing to its notable advantages such as self-emissive properties, ultra-high brightness, exceptional contrast ratio, low power consumption, long lifespan, and compatibility with flexible displays [1–5]. Compared with LCD technology that relies on backlight modules and OLED technology limited by the degradation of organic materials [4,5], Micro LED exhibits irreplaceable advantages in pixel-independent driving, response speed, and device reliability. It exhibits broad application prospects particularly in high-end display fields such as virtual reality (VR)/augmented reality (AR) near-eye displays, automotive displays, and 8 K + ultra-high-definition large-screen splicing [6–10]. However, the large-scale industrialization of Micro LED still faces some technical bottlenecks. Due to the enormous quantity and minuscule size of Micro LEDs, as well as the thermal incompatibility between fabrication substrates and display backplanes, the so-called mass transfer technology, i.e. the mechanical transfer of numerous Micro LEDs to the driver substrate and accomplish bonding therein, encounters huge challenges [11,12]. Recently, researchers have developed various techniques with high-precision control capabilities, such as stamp transfer and laser transfer. These technologies enable the precise transfer of millions of Micro LEDs to driver backplanes, with a single transfer yield of over 99.999 % [13,14]. The primary function of the bonding process is to establish electrical connections and provide mechanical support between the Micro LEDs and the driver backplane [15]. Currently, flip-chip bonding utilizing micro-bump structures remains the most widely adopted packaging technology for Micro LED integration. To achieve high-density integration and reliable packaging, it is imperative to perform the bonding process at the lowest feasible temperature [10], thereby mitigating the adverse thermal effects on the optoelectronic properties of the devices. Owing to its low melting point (156.51°C) and high thermal conductivity, indium (In) has been recognized as a suitable and effective material for low-temperature flip-chip bonding [11,16]. This low melting temperature of pure indium (approximately 156 °C) allows low-temperature bonding, which substantially reduces the thermal budget required for the process and effectively prevents thermal

* Corresponding authors at: Fujian Science and Technology Innovation Laboratory for Optoelectronic Information of China, and College of Physics and Information Engineering, Fuzhou University, Fuzhou 350100, China (J. Sun).

E-mail addresses: qunfyan@fzu.edu.cn (Q. Yan), jiesu@chalmers.se (J. Sun).

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damage to sensitive components [12]. Nevertheless, the high oxidizability of indium presents a major challenge during fabrication: upon exposure to air, a high-melting-point (~1910 °C) indium oxide (In_2O_3) layer rapidly forms on the surface [13], which significantly inhibits atomic diffusion during the bonding and may result in defective interconnections or impaired bond strength [14,15]. Hence, the development of efficient reflow techniques capable of mitigating the surface oxide layer on In bumps is essential to enhancing the bonding reliability, representing a pivotal step toward robust manufacturing processes.

In contemporary reflow processes, while dry reflow techniques effectively eliminate surface oxide layers from bumps, their reliance on complex atmospheres (e.g., formic acid vapor) and specialized equipment introduces significant process costs and safety concerns [10,16]. Moreover, dry reflow necessitates precise coordination of multiple parameters-including temperature, gas concentration, pressure, and processing time, resulting in a narrow process window and challenges in achieving consistent yield stability [16]. By contrast, wet reflow can be conducted under ambient atmospheric conditions using liquid media such as fluxes or organic solutions to remove and prevent re-oxidation, offering a simpler and more easily controllable process [18]. Within this context, the solder mask serves as a critical functional layer whose design and fabrication quality directly determine the bump morphology, electrical connectivity, and overall packaging yield. Owing to the high fluidity and wettability of molten indium during reflow, inadequate confinement may lead to uncontrolled bump spreading, morphological instability, and electrical shorting between adjacent pads. The solder mask can confine the soldering region via precisely defined openings and leverages its low wettability against indium to restrict lateral flow, thereby promoting uniform bump formation and accurate positioning. Furthermore, it offers essential electrical insulation between bumps, ensuring independent bonding in high-density arrays and significantly enhancing the bonding uniformity and long-term reliability. Thus, the solder mask is not merely an auxiliary feature but a fundamental component for achieving high-yield and high-reliability Micro LED packaging. Conventional wet reflow processes typically employ silicon dioxide (SiO_2) or metallic layers (e.g., Ti/Cu) as solder mask. However, these materials exhibit considerable limitations: the SiO_2 is usually deposited by PECVD at temperatures around 300°C [19], which involves high complexity, elevated cost, and poor compatibility with flexible substrates. Although metallic barriers can provide physical confinement, they are prone to oxidation and introduce additional lithography, deposition, and etching steps, thereby increasing process complexity and manufacturing cost.

To address the aforementioned challenges, this study proposes an innovative wet reflow process for In bumps utilizing the negative-tone photoresist SU-8 as the solder mask. Compared to conventional SiO_2-based processes, the proposed approach offers the following significant advantages: (1) the need for complex multi-step sequences such as deposition, Inductively Coupled Plasma(ICP) etching, and post-etch cleaning. (2) The low-temperature processing characteristics of SU-8 provide broader compatibility, particularly with temperature-sensitive flexible substrates. (3) The use of a glycerol solution as the reflow medium offers enhanced environmental friendliness compared to traditional fluxes. Using this process, a 480 × 640 array of In bumps with a pitch of 222 μm was successfully fabricated on a driver substrate. Characterization results indicate that the fabricated In bumps exhibit smooth surfaces and excellent height uniformity. Bonding experiments conducted under optimized conditions demonstrated a significant improvement in the reliability of the reflowed In bumps compared to those without reflow treatment. The aim of this work is to develop a simplified and low thermal budget fabrication strategy for indium bump arrays by integrating an SU8 based solder mask with a glycerol assisted wet reflow process, and to validate its practical feasibility through Micro LED flip chip bonding demonstrations. This unified approach is designed to enhance bump morphology, improve height uniformity, and ensure reliable bonding performance while maintaining compatibility with temperature sensitive substrates, thereby providing a scalable pathway for advanced Micro LED packaging. In summary, the SU-8 solder mask-based wet reflow process developed in this study not only effectively addresses core issues of conventional solder masks, including such as process complexity, high cost, and poor compatibility, but also significantly enhances the quality and bonding reliability of In bumps. This technology provides a feasible and efficient pathway for low-cost manufacturing of Micro LEDs, particularly promising for emerging applications such as flexible wearable devices and curved automotive displays, indicating substantial potential for industrial adoption.

2. Method

2.1. Fabrication of the driving substrate

This experiment used a 5 × 5 cm^2 transparent glass substrate to mimic the actual driver backplane. We note that standard thin-film transistor (TFT) drivers are typically also made on glass substrate, and therefore our experiments may well verify the feasibility of the process, but at a much lower cost. First, preprocess the substrate: ultrasonically clean in acetone and isopropanol for 5 min each, blow dry with high-purity nitrogen gas, then bake at 100°C for 10 min to release stress, and cool to room temperature. Next, use photolithography to fabricate the metal structure to the glass substrate. The electrode material is a titanium (Ti)/aluminum (Al) metal system, which is consistent with the metal system of the TFT substrate circuit. A Ti/Al metal layer with a thickness of about 170 nm (total resistance about 0.5 Ω) is deposited by magnetron sputtering, The thickness of the Ti/Al/Ti electrodes was controlled using a time-calibrated sputtering process. Prior to fabrication, the deposition rate of each layer was experimentally calibrated so that the desired thickness could be accurately achieved by controlling the sputtering duration. After deposition, the film thickness was verified using a surface profilometer (DektakXT) on a lift-off test pattern. Multi-point measurements across the substrate confirmed a thickness variation within ± 5 %, which is sufficient for the subsequent lithography and bump-reflow step. The optical microscope photo of the prepared driver backplane is shown in Fig. 1(a).

2.2. Fabrication of indium bump array

The fabrication of the In bump array on the driving backplane was achieved using a dual-step photolithography process, as illustrated in Scheme 1. First, the initial photolithography step was performed to pattern the solder mask using SU-8 photoresist (Scheme 1(a)–(c)). This process involved spin-coating an approximately 1.5 μm thick layer of negative-tone SU-8 photoresist over the entire illuminated backplane surface. The array pattern of the solder mask (with a diameter of 5 μm, pitch of 222 μm, and array dimensions of 480 × 640) was transferred onto the backplane via photolithography. The driving substrate itself contains 160 × 160 pixels, each composed of three sub-pixels (red, green, and blue). Each sub-pixel has two electrodes (anode and cathode) and one compensation pad, leading to a total of 480 × 640 electrode openings that match the SU-8 solder mask and indium bump arrays. The pitch of 222 μm is maintained consistently across all arrays to ensure geometric compatibility. After exposure, a graded post-exposure bake was conducted: first at 65°C for 3 min to enable stress relaxation—ensuring that the solder mask would not detach from the backplane due to thermal stress during subsequent In bump reflow—followed by baking at 100 °C for 7 min to complete the cross-linking and curing of the SU-8 epoxy resin. After development, oxygen plasma treatment (100 W, 2 min) was applied to remove any residual SU-8 from the open windows. Finally, a hard bake was performed at 200 °C for 30 min, which significantly increased the glass transition temperature of SU-8 to 215°C [25,26], thereby enhancing its thermal stability to meet the temperature requirements of the subsequent reflow process (After this process step is completed, the result is shown in Fig. 1

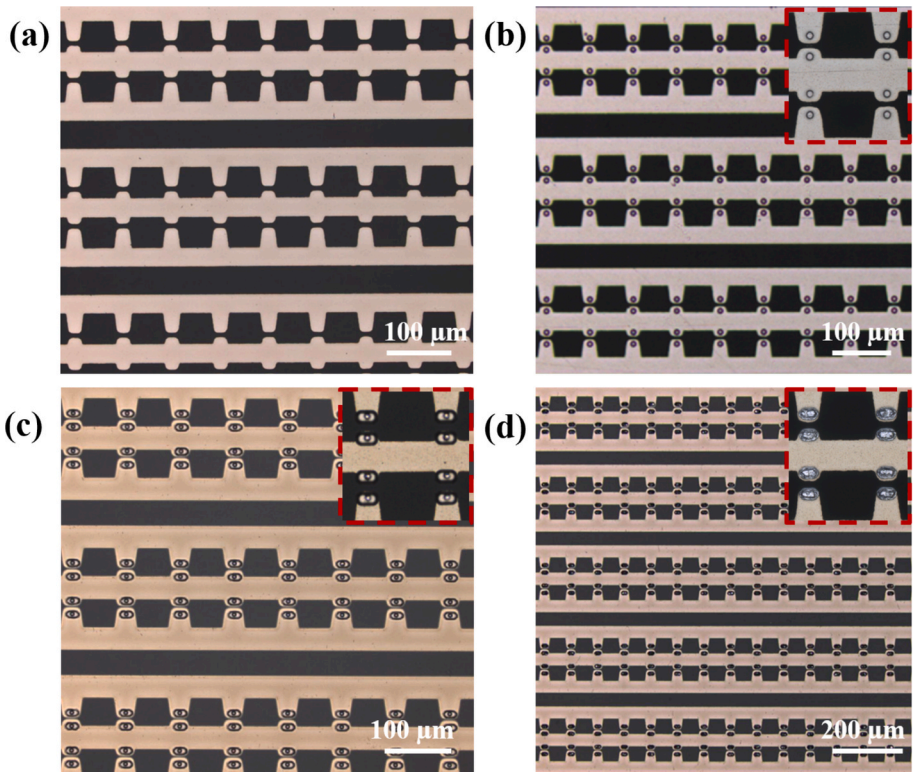
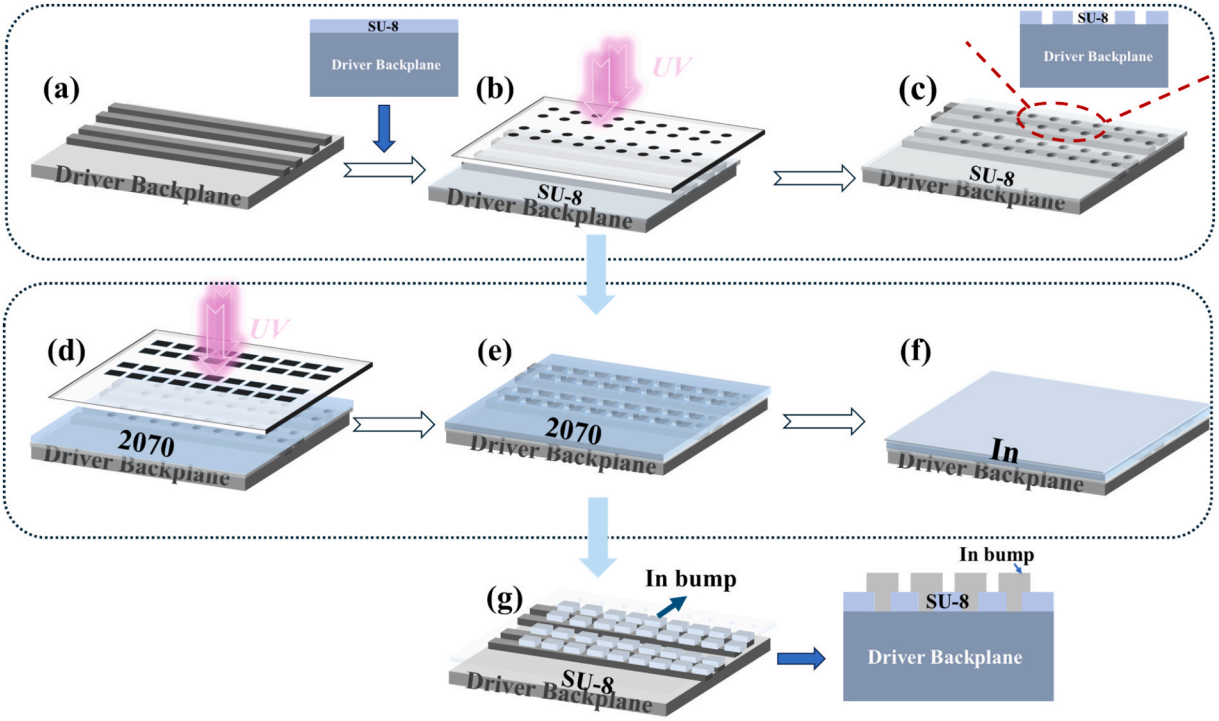


Fig. 1. Under an optical microscope: (a) Electrode structure of driver backplane, (b) Pad opening at the electrode, (c) Array of In bumps obtained by evaporation deposition, Photolithography for In bump evaporation, (d) Photolithography for In bump evaporation.



Scheme 1. In bump manufacturing process: (a) Structure of the driver backplane before SU-8 coating, (b) Ultraviolet lithography exposure, (c) Post-exposure bake with development and hard bake, (d) AZ 2070 photoresist coating followed by UV exposure, (e) Development process, (f) In thin-film evaporation deposition, (g) Metal lift-off patterning.

(b)). Subsequently, the second photolithography step was carried out to fabricate the arrayed In bumps (Scheme 1(d)–(g)), Fig. 1(c) shows the result of the bump photolithography process. An approximately 4.5 μm thick In film was deposited via thermal evaporation. After deposition, the sample was immersed in a stripper solution for lift-off processing, rinsed with deionized water, and dried with high-purity nitrogen gas. A

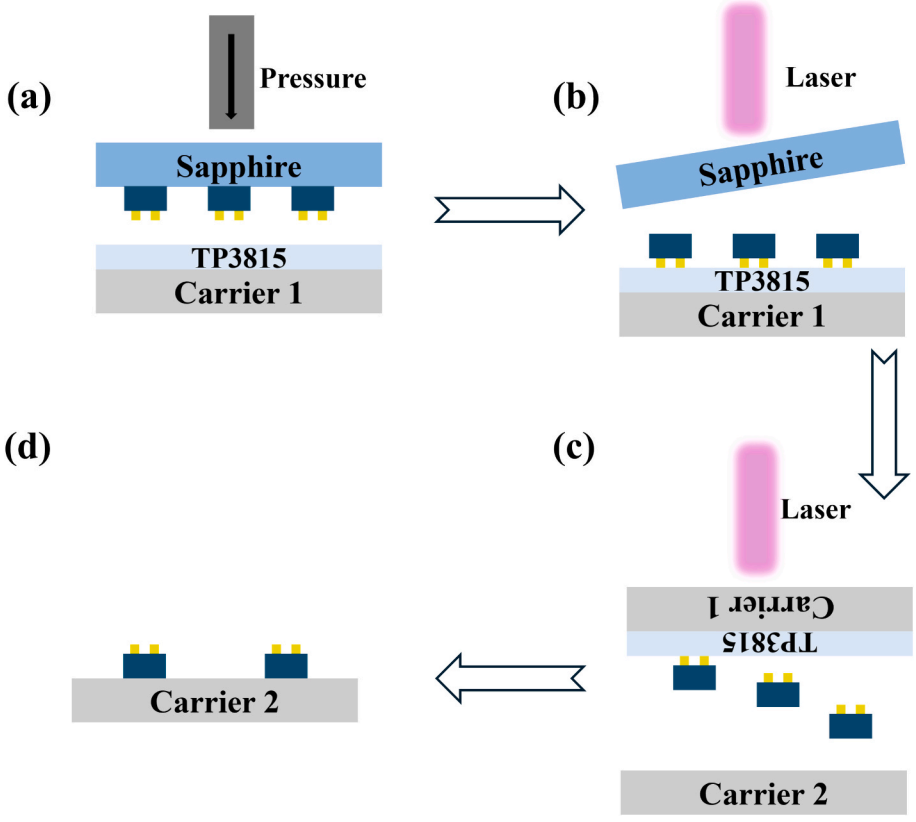
complete 480 × 640 In bump array was successfully obtained, as shown in the optical micrograph in the Fig. 1(d). During the flip-chip bonding process, a 40 × 40 LED array was used for segmented bonding. Each bonding operation connects approximately 160 LEDs at a time to ensure alignment accuracy and high yield, while maintaining full consistency with the 222 μm bump pitch.

2.3. Fabrication of micro LED arrays for bonding

The fabrication process of COC 2 (Chip-on-Carrier), intended for the subsequent bonding of Micro LEDs to the driver backplane, is illustrated in Scheme 2. First, the COW (Chip-on-Wafer) with a Micro LED array (unit size: 30 μm × 15 μm) was bonded to a temporary carrier (Carrier 1) via thermocompression bonding. Carrier1 was prepared by spin-coating TP3815, a commercial dynamic release polymer (TP3815, Micro LED Technology Co.), onto a quartz substrate. TP3815 is a bubble-induced dynamic release layer(DRL)material, that provides sufficient initial adhesion to fully receive the Micro LED array released from the sapphire substrate while maintaining the original array pitch, thereby enabling temporary fixation of the Micro LEDs, as shown in Scheme 2(a). The suitability of TP3815 for laser-assisted chip transfer has been demonstrated in previous work [29]. Subsequently, the sapphire substrate was removed using a laser lift-off system, transferring the Micro LED array onto Carrier 1 with the electrodes facing downward, as depicted in Scheme 2(b). we also clarify the key laser parameters used for lift-off, including a wavelength of 266 nm and an energy density of 0.12 J cm^{-2}, to ensure reproducibility of the process. To achieve flip-chip bonding between the Micro LED array and the driver backplane, it was necessary to flip the array so that the electrodes face upward, allowing precise alignment and reliable interconnection with the micro-bumps on the driver backplane. As shown in Scheme 2(c), a laser was used to transfer the Micro LEDs from Carrier 1 to a second temporary carrier (Carrier 2), whose adhesive layer primarily consists of Polydimethylsiloxane (PDMS). PDMS was selected due to its elasticity and low surface energy, which facilitate controlled chip release and repositioning during transfer [30]. The laser beam passed through the quartz substrate of Carrier 1 and reached the TP3815 interface, where a localized heating zone was formed, generating a "micro-gas-cushion" effect that promoted debonding and enabled controlled release of the Micro LEDs onto Carrier 2. Ultimately, a 40 × 40 array of Micro LEDs ready for bonding, referred to as COC 2, was formed on Carrier 2, as presented in Scheme 2(d). In the bonding configuration used in this study, the indium bumps deposited on the Ti/Al/Ti electrodes of the driver substrate form the bonding joint with the Au contact electrodes of the Micro LED chips. The dimensions of each Micro LED are 30 μm × 15 μm, with a pitch of 222 μm, matching the electrode spacing on the driver backplane.

2.4. Reflow of indium bumps and bonding of Micro LED arrays to driver backplane

To ensure efficient reflow of the In bumps, the peak reflow temperature was set to 175 °C, which is slightly above the melting point of indium (156.6 °C) and also falls within the typical industrial reflow range for indium bump processes (170–190 °C) as reported in previous studies [27,28]. This temperature setting ensures complete melting of In, facilitates oxide mitigation, and enables stable bump formation. Notably, the subsequent thermocompression bonding step in this work is performed at 180 °C, further confirming that the selected reflow temperature is appropriate and consistent with standard manufacturing conditions. Temperature control was achieved using an existing reflow system (shown in Fig. 2), glycerol solution employed as the wet reflow medium. To ensure reproducibility, the temperature settings, cooling method, and cleaning procedure were strictly standardized. The glycerol



Scheme 2. Preparation process of COC 2. (a) Bonding Micro LED chips from COW to Carrier 1, (b) Sapphire substrate removal using laser lift-off (LLO) system, (c) Transferring Micro-LED chips from Carrier 1 to Carrier 2 via laser, (d) Schematic of COC 2.

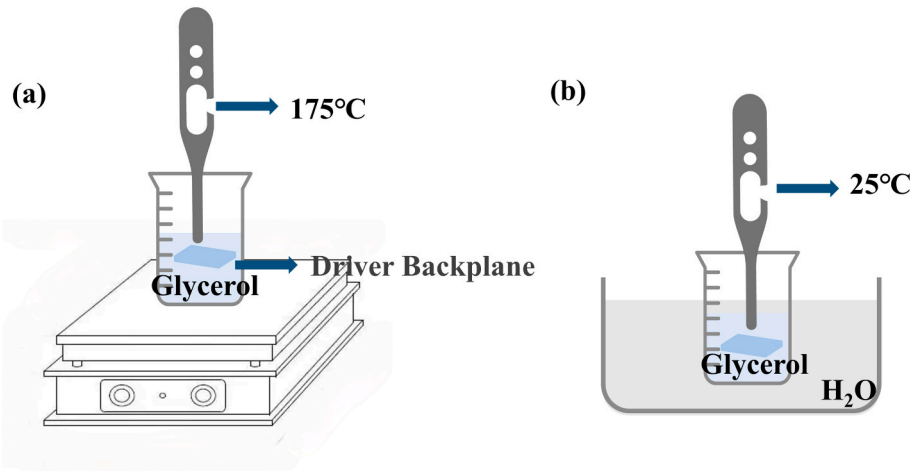


Fig. 2. Reflow of In Bumps and Bonding of Micro LED Arrays to Driver Backplane (a) Thermal treatment on heated stage, (b) Quench cooling in temperature-controlled water bath (25°C).

solution was first preheated to 175 °C, after which the substrate with In bumps was fully immersed and held at this temperature for 5 min to ensure complete melting of the bumps and mitigation of surface oxide (the reflow profile is shown in Fig. 3). During this process, the glycerol medium isolated the sample from air, facilitated oxide mitigation, and promoted interdiffusion of indium atoms. After reflow, the samples were immediately transferred to a room-temperature water bath for rapid cooling. All samples were cleaned following a unified protocol: they were rinsed thoroughly with deionized water to remove residual glycerol, then cleaned with isopropanol (IPA), and finally dried with high-purity nitrogen. It is worth noting that the glycerol-based wet reflow exhibits a broad process window and is insensitive to heating and cooling rates; repeated experiments confirmed that consistent reflow morphology could be achieved within a temperature fluctuation range of ± 5 °C. All reflowed samples in this study were processed using these standardized parameters. Following the reflow process, the Micro LEDs were bonded to the bumps on the driver substrate. To achieve high-precision alignment and reliable electrical interconnection, a high-accuracy transfer bonding system was used to align and bond the Micro LED array to the driver backplane. The bonding process is illustrated in Scheme 3.

2.5. Equipment and characterization methods

To ensure experimental reproducibility, all fabrication and characterization equipment used in this study are summarized as follows:

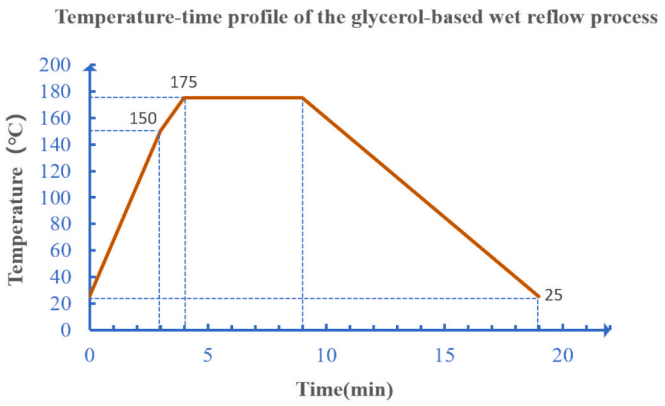


Fig. 3. Temperature-time profile of the glycerol-assisted indium bump reflow process, showing the heating stage, holding stage at 175 °C for 5 min, and subsequent rapid cooling in a room-temperature water bath.

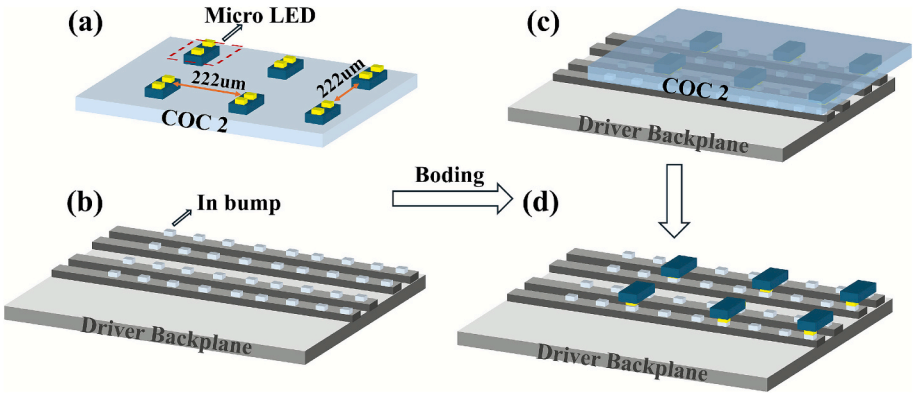
The photolithography process was performed using a Suss MA/BA6 Gen4 UV mask aligner. Flip-chip bonding of Micro LEDs was conducted on a FC3000MSF micro-transfer and bonding system, while laser lift-off of Micro LEDs from the sapphire substrate was carried out using a LMT-350TRF laser repair system. Metal electrodes were deposited using a magnetron sputtering system, and indium bumps were formed via thermal evaporation using the laboratory's thermal evaporation coater. For characterization, contact angle measurements were performed with an SL200KS optical contact angle/interfacial tension analyzer to evaluate the wettability of SU-8. Bump height and surface morphology were measured using a white-light interferometry 3D optical profilometer. Bonding reliability was assessed using an MFM1200 shear testing system. These details have been added to the corresponding sections to improve transparency and experimental reproducibility.

3. Results and discussion

3.1. Fabrication of SU-8 solder mask

The preparation of the solder mask and the opening of solder pads are critical preliminary steps in the reflow process, whose quality directly determines the success of In bump formation. In this study, we innovatively employed the negative photoresist SU-8 as the solder mask material. The patterning was achieved on the driver backplane through spin-coating, lithographic opening, and hard baking (Fig. 1(b)). The bump reflow process imposes strict requirements on the solder mask material: firstly, it must possess excellent thermal stability to withstand the high temperatures during reflow; secondly, the wettability difference between the solder mask and the metal layer plays a key regulatory role in the flow of molten In and bump formation. An ideal solder mask should exhibit poor wettability (high contact angle) to effectively constrain the spreading of In, while the metal layer requires good wettability; together they form an "invisible mold" that controls the bump shape [18–20]. Furthermore, good chemical stability and mechanical strength are necessary to maintain pattern integrity and protect the circuit in subsequent processes. SU-8, as a negative epoxy-based photoresist, offers excellent chemical corrosion resistance, good thermal stability, and high mechanical strength. After hard baking, its ability to withstand high temperatures exceeds 250°C [21,22].

Therefore, this study investigated the influence of hard baking conditions on the wettability of SU-8. The contact angle measurements were performed using an SL200KS optical contact-angle/interfacial-tension analyzer, with deionized water as the probe liquid, a droplet volume of 2 μL, and the measurement conducted at room temperature. By optimizing the process parameters, it was found that hard baking at



Scheme 3. Schematic of Flip-Chip Bonding Process for COC 2 and Driver Backplane: (a) Laser-transferred COC 2 substrate, (b) Driver backplane with In-bump array (pitch: 222 μm), (c) Flip-chip bonding, (d) Bonded Micro LED array on active matrix.

200°C for 30 min resulted in a contact angle of approximately 80°, as shown in Fig. 4. It should be noted that the DI-water contact angle measurement is used here only as a qualitative indicator of surface energy and surface condition changes of the SU-8 layer after hard baking, rather than a direct quantitative measure of molten indium wettability. An increased DI-water contact angle reflects a modification of the SU-8 surface state (e.g., reduced surface energy), which may qualitatively influence the spreading behavior of molten indium during reflow. However, this measurement is not intended to imply a direct or quantitative equivalence between water and indium wettability. Compared with conventional SiO_2 solder masks that require PECVD deposition, photolithography, ICP etching, and post-cleaning at elevated temperatures (~300 °C) [19], SU-8 enables simultaneous solder mask formation and pad opening through a single UV lithography step. This significantly simplifies the fabrication workflow, reduces equipment dependence, processing time, and manufacturing cost, while maintaining excellent compatibility with temperature-sensitive substrates due to its low-temperature processing characteristics [23]. Although SU-8 offers excellent thermal stability, chemical resistance, and mechanical robustness, potential drawbacks include long-term aging, moisture absorption, and property drift under prolonged environmental exposure. These factors should be considered when SU-8 is used in long-lifetime or high-humidity applications. This simple, low-temperature, and highly compatible process route makes SU-8 a suitable and promising solder mask material for In bump reflow applications. Overall, SU-8 satisfies the essential requirements for a solder mask in In bump wet reflow and provides a low-cost and process-efficient solution for microelectronic packaging applications.

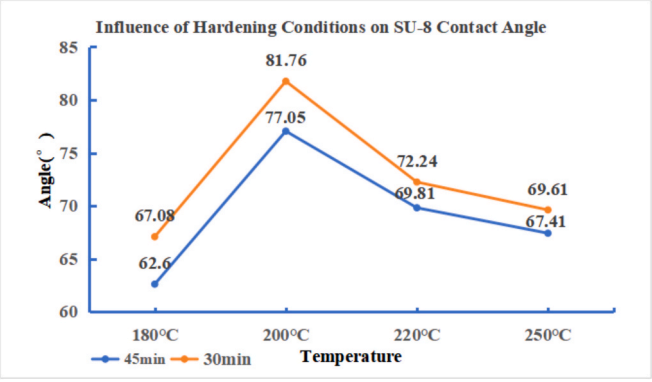


Fig. 4. Contact angle of SU-8 under different hard bake conditions (temperature and duration).

3.2. *Indium film deposition and wet reflow Balling of in bumps in ambient atmosphere*

This study employed a photolithography, evaporation, and lift-off process to fabricate In bump arrays for flip-chip bonding. The lithography window was designed to be 16 × 10 μm^2, Although this opening size is smaller than the Micro LED chip dimension (30 × 15 μm), this design is intentional and determined by the electrode configuration of the Micro LED. Each Micro LED spans two adjacent indium bumps corresponding to the anode and cathode electrodes, and the spacing between these electrodes on the backplane is 10 μm. Therefore, the bump-opening length was defined as 10 μm to match the electrode separation, while the opening width was set to 16 μm, which is slightly larger than the chip width (15 μm), to accommodate lithography tolerance and ensure accurate bonding alignment. During thermal evaporation, the total amount of evaporated In was 8.5 g, with a substrate temperature of 50°C, a vacuum level of 4 × 10^{-4} Pa, and an evaporation rate of 1.25 nm/s, resulting in an In film approximately 4.5 μm thick. This process successfully produced a bump array of 480 × 640 with a yield of 100 %. However, the as-evaporated In bump array exhibited a rough surface with burs and poor height uniformity, showing a height non-uniformity of 4.8 % in coefficient of variation (CV) and a surface roughness (R_a) of 0.65 μm. These morphological defects primarily originated from the directional variation of atomic deposition and film formation characteristics during thermal evaporation [24].

To improve the bump morphology, a wet reflow process based on an SU-8 solder mask was applied. The driver substrate was immersed in a glycerol solution and reflowed at 175°C for 5 min, followed by water cooling to room temperature; the reflow setup is shown in Fig. 2. Multiple experiments indicated that even with a reflow temperature fluctuation of ± 5°C, satisfactory results could still be achieved, demonstrating high process stability and a broad process window. In this work, glycerol was employed as a wet reflow medium based on experimental observations. The presence of glycerol may modify the surface condition of the indium surface and its native oxide layer through physical interactions, thereby facilitating oxide disruption during reflow. This interpretation is consistent with prior studies on indium oxidation behavior and wet reflow-assisted oxide mitigation [31], although the specific role of glycerol is evaluated here based on experimental evidence rather than directly derived from these references. This oxide-removal mechanism, combined with the ± 5 °C tolerance of the reflow process, ensures that minor temperature fluctuations do not significantly influence bump quality. Compared with conventional reflow methods, this approach reduces sensitivity to reflow parameters (such as time and temperature), improves process tolerance and operational simplicity, and effectively mitigates failure modes including bridging (short circuits) and irregular bump morphology (e.g., excessive height variation or undesirable solder shape) caused by uneven In

spreading or over-flow [24]. Moreover, using glycerol as the reflow medium facilitates oxide mitigation while offering improved cost effectiveness compared to conventional flux agents.

A systematic comparison and analysis of the morphology and performance of the bumps before and after reflow treatment were conducted. Preliminary characterization using 3D microscopy revealed that the initial evaporated In bumps had a rough surface with significant height variations across different regions (Fig. 5(a) and (c)). To further clarify the optical observations, it should be noted that the SU-8 solder mask remains on the sample surface in all optical microscopy images shown in Fig. 5(a–d). Because SU-8 is a transparent negative photoresist with low optical absorption, it does not appear as a distinct feature in the optical images. The colour variations observed on the Ti/Al/Ti electrode traces, especially in Fig. 5(b) and Fig. 5(d), originate from thin-film optical interference (Newton-ring effects) caused by slight differences in surface reflectance rather than delamination or adhesion failure. No peeling or cracking of either the SU-8 layer or the Ti/Al/Ti electrodes was observed during thermal cycling, confirming their adhesion stability at the reflow temperature. Further scanning electron microscopy (SEM) analysis confirmed that the as-deposited In bumps possessed a rough surface with burrs and poor height uniformity (Fig. 6(b)). In Fig. 6 (a–c), all SEM images were obtained from the same wafer. The Ti/Al/Ti electrode layer is not visible because a thin conductive metal coating (e.g., Au) was deposited on the surface prior to SEM imaging to prevent charging on the SU-8 layer. This coating masks the underlying Ti/Al/Ti electrodes and SU-8 structures. Additionally, the SU-8 solder mask is a transparent epoxy-based material with very low electron contrast, making it inherently difficult to observe under SEM. Only the morphology of the indium bumps is therefore visible in the images. In this work, glycerol was employed as the wet reflow medium. This choice is based on the general understanding that organic liquids and wet reflow media can assist in mitigating indium surface oxidation by physically isolating the molten metal from ambient oxygen and facilitating interfacial rearrangement during reflow [10,13]. Based on this established principle, glycerol, a representative polyol with good thermal stability and environmental compatibility, was selected for the present study. The specific improvements in bump spheroidization, surface smoothness, and bonding reliability are primarily derived from the optimized process conditions and experimental observations in this work. Recent review studies have also highlighted the potential of polyol-based and organic wet reflow media for low-temperature microbump fabrication [31]. This mechanism is consistent with the smoother and more uniform bump morphology observed in our reflowed samples. After reflow treatment, the bump uniformity improved significantly, transforming into smooth spherical structures (Fig. 6 (a) and (c)). The height non-uniformity decreased from 4.8 % to 0.28 %, an improvement of nearly 20 times (as calculated by eq.1). To quantitatively evaluate bump height uniformity, measurements were performed over nine regions, each containing nine bumps, resulting in a total of 81 data points used for calculating the coefficient of variation (CV). where x represents the height of the bump. The bump height uniformity was evaluated by averaging the results from nine regions, each containing nine bumps. The white-light interferometry image in Fig. 7 (a)&(b) was obtained from one randomly selected area to quantitatively illustrate the reduction in surface roughness, which is consistent with the SEM observations. Measurements using white light interferometry showed that the surface roughness (R_a) of the bumps decreased from 0.65 μm to 0.126 μm, the roughness values (R_a) reported in this work were obtained from nine individual bumps, each taken from one of the nine measured regions, and the final R_a values correspond to the average of these measurements (as shown in Fig. 7 (a)and(b)), meeting the general requirements for subsequent flip-chip bonding processes. To clearly illustrate the multilayer bonding structure, a schematic diagram has been added in Fig. 7 (c), showing that the Au contact of the Micro LED is bonded to the In bump, which is directly supported by the Ti/Al/Ti electrode on the driver substrate. A magnified bonded-region image is provided in Fig. 7 (d), and the revised FIB-SEM cross-sections in Fig. 7. now include corrected annotations identifying all structural layers. The overall process yield was 100 %, defined as the ratio of bumps that remained intact and uniformly spherical after reflow to the total bump count. No bumps detached or deformed during reflow, and all exhibited complete, well-shaped spherical morphology, indicating improved interfacial continuity and bonding quality after reflow treatment. Furthermore, the post-reflow bumps demonstrated enhanced mechanical properties, and the effectiveness of the process was further verified by shear test results after bonding. To avoid ambiguity in interpreting

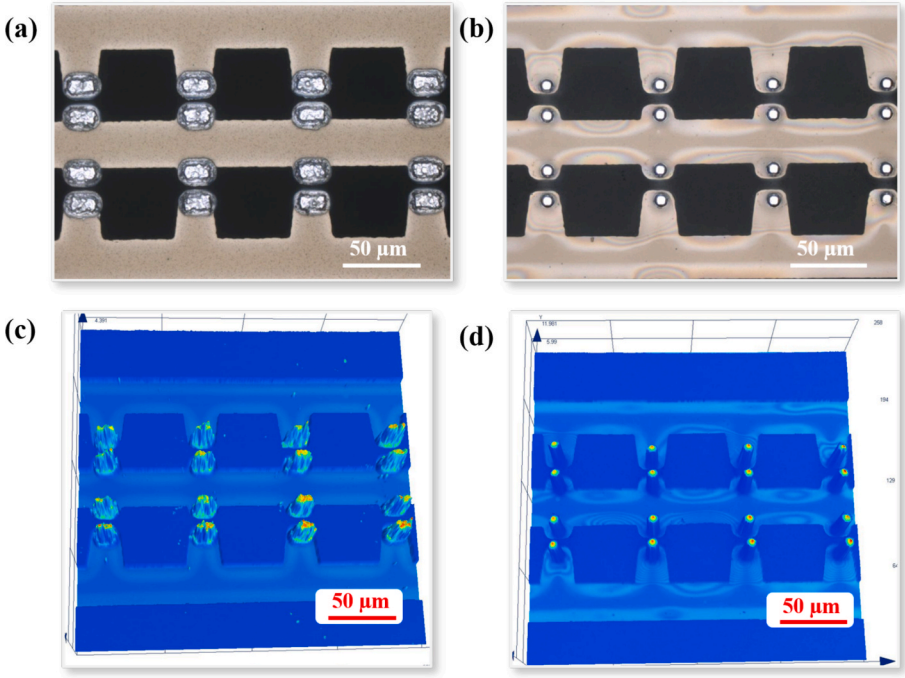


Fig. 5. Morphology of In bumps under optical microscope: (a) before reflow, (b) after reflow; under 3D microscope: (c) before reflow, (d) after reflow.

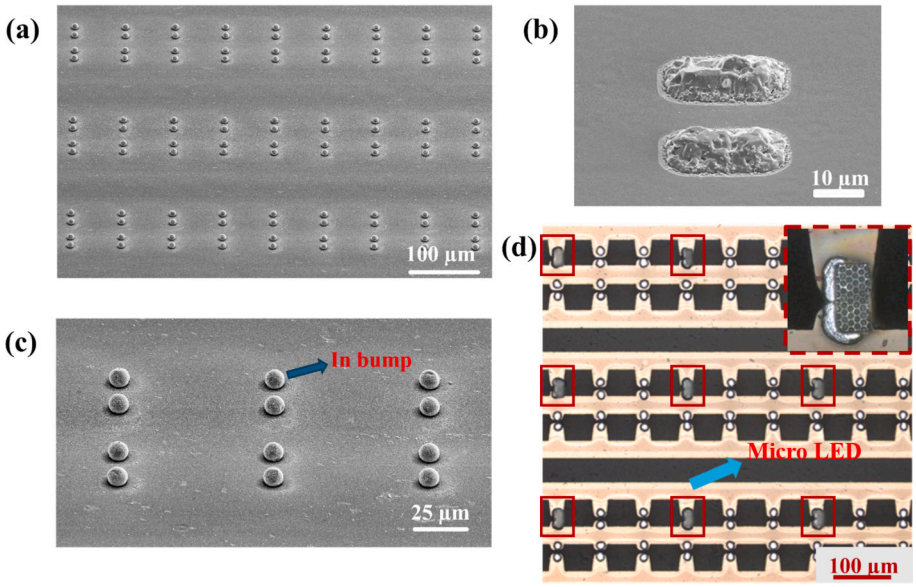


Fig. 6. (a) SEM image of In balls after reflow, (b) SEM image of In bumps before reflow, (c) SEM image of In balls after reflow at a higher magnification, (d) Bonding situation under an optical microscope.

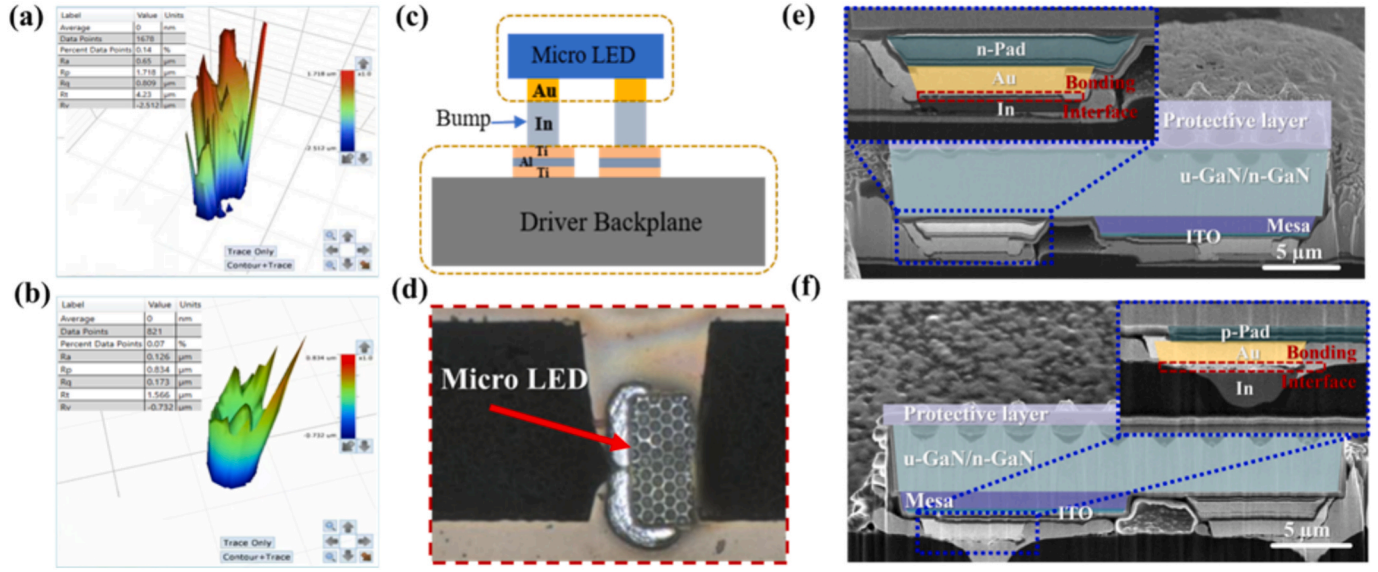


Fig. 7. (a)Surface roughness of as-deposited In bumps measured by white-light interferometry before reflow; (b) Surface roughness of In bumps after wet reflow treatment; (c) Structural schematic of the Micro LED flip-chip bonding interface. The driver Backplane employs a Ti/Al/Ti electrode, onto which indium bumps are evaporated. On the Micro LED chip, the metal contact electrode is Au. During flip-chip bonding, the Au electrode of the Micro LED bonds to the In bump, (d) Optical microscopy image showing the bonded region after flip-chip bonding; (e) Cross-sectional SEM image of the bonded Micro LED on the driver backplane without reflow treatment. All major structural layers, including the protective layer, GaN epilayer, Au contact, and In bump, are labeled. The bonded interface exhibits a discontinuous and locally limited Au/In contact region, resulting in a reduced effective contact area; (f) Cross-sectional SEM image of the bonded Micro LED after wet reflow treatment, with the same structural layers labeled as in (e). Compared with the non-reflowed case, the Au/In bonded interface becomes more continuous and uniform, indicating an enlarged effective contact area and improved interfacial bonding quality.

the SEM images, the detailed multilayer structure of the Micro LED/driver backplane assembly is primarily illustrated in the schematic shown in Fig. 7(c), while the SEM cross-sections in Fig. 7(e) and (f) are used mainly to compare the interfacial contact morphology before and after reflow treatment.

$$CV = \frac{\sigma}{\bar{x}} = \frac{\sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - \bar{x})^2}}{\frac{1}{n}\sum_{i=1}^{n} x_i} \quad (1)$$

3.3. Impact of in bump morphology on bonding reliability

To further investigate the influence of bump morphology on bonding reliability, this study systematically compared the performance differences between reflow-treated and untreated In bumps during the bonding process. After bonding, optical microscopy was first employed to examine the bonding alignment (Fig. 6(d)), followed by a comprehensive evaluation of the interfacial connection quality using scanning electron microscopy (SEM) and shear testing. The results indicate that the untreated In bumps exhibited significant reliability issues after

bonding with Micro LEDs. Shear test reliability evaluation was carried out to quantitatively assess the bonding strength of Micro LEDs bonded onto the In bump arrays. The shear tests were performed using an MFM1200 system under a test pressure of 0.5 MPa, equipped with a BS25G force sensor, and a shear speed of 100 μm/s. A total of nine bonded Micro LED chips were tested, and all reported shear strength values represent the average of these nine measurements. The average shear strength was 0.136 N with a standard deviation of 0.09 N, indicating poor mechanical connection performance. After bonding under identical conditions, the bonded interface structure was examined using focused ion beam (FIB) sectioning. The cross-sectional SEM image in Fig. 7(e) shows that, without reflow treatment, the bonded Au/In interface is discontinuous and locally confined, resulting in a limited effective contact area.

Combined with the pre-bonding bump morphology analysis, the failure mechanism was identified: the as-evaporated In bumps had a rough surface with local height variations exceeding 2 μm, leading to locally incomplete contact and interfacial gaps at the bonded interface. This resulted in a significantly reduced contact area, severely compromising connection stability. In contrast, the bonded interface of the samples subjected to reflow treatment prior to bonding (Fig. 7(f)) showed a notably larger contact area and a denser interconnection morphology. The reflow process resulted in In bumps with a smooth surface, uniform spherical profile, and excellent height consistency (height variation < 0.2 μm), while effectively mitigating the surface oxide layer. Shear test results further demonstrated that the average bonding strength of this group reached 1.106 N with a standard deviation of 0.327 N, nearly an order of magnitude higher than that of the untreated samples, showing its superior connection uniformity and reliability. It should be noted that shear strength benchmarks across the literature are highly dependent on specific bonding conditions, chip size, bump geometry, solder mask design, and measurement configuration, making direct numerical comparison unreliable. Therefore, this study focuses on an internally controlled comparison between reflowed and non-reflowed bumps under strictly identical processing conditions, ensuring that the observed differences in bonding reliability originate solely from the bump morphology and reflow treatment.

Overall, the results indicate that reflow treatment improves In bump morphology, increases effective interfacial contact area, and contributes to enhanced bonding reliability. This provides an experimental basis for its application in microelectronic packaging, particularly in Micro LED bonding processes.

4. Conclusion

This study developed and validated a novel and efficient wet reflow process for In bumps using SU-8 photoresist as the solder mask. Unlike conventional SiO_2 or metal solder masks, SU-8 patterning can be achieved with a single UV lithography step, eliminating the need for deposition, etching, and sputtering, thereby significantly reducing process complexity, cycle time, and cost. In addition, the low-temperature process of SU-8 ($\leq$ 200 °C) ensures excellent compatibility with various substrates, particularly temperature-sensitive flexible backplanes. The optimized SU-8/reflow In bump process demonstrated improved thermocompression bonding yield and enhanced reliability, as confirmed by shear testing. The proposed wet reflow technology based on SU-8 solder mask provides a cost-effective and versatile solution for reliable bonding in Micro LED packaging, effectively addressing the limitations of conventional solder mask and reflow approaches. Its simplicity, low thermal budget, and substrate compatibility make it highly attractive for next-generation applications such as high-resolution VR/AR displays, flexible and wearable electronics, and automotive curved screens. Future work will focus on further evaluating its performance in high-density devices and on flexible substrates. Overall, the process developed in this work provides a simplified and robust reflow route that significantly reduces the number of lithography and etching steps, reduces the thermal budget, and enables uniform, high-quality In bump formation. These features make the proposed method highly compatible with existing Micro LED manufacturing lines and suggest strong clear potential for large-scale industrial adoption.

CRediT authorship contribution statement

Shuangjia Bai: Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Taifu Lang:** Writing – review & editing, Supervision, Methodology, Formal analysis, Conceptualization. **Xin Lin:** Writing – review & editing, Supervision, Methodology. **Shuaishuai Wang:** Writing – review & editing, Supervision, Methodology. **Zhihua Wang:** Writing – review & editing, Supervision. **Chang Lin:** Supervision. **Qun Yan:** Supervision, Resources, Project administration, Methodology, Funding acquisition. **Jie Sun:** Writing – review & editing, Supervision, Resources, Project administration, Methodology, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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Further reading

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