Simulation of Quantum Computers: Review and Acceleration Opportunities

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REVIEW-ARTICLE

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Quantum computing has the potential to revolutionise multiple fields by solving complex problems that cannot be solved in reasonable time with current classical computers. Nevertheless, the development of quantum computers is still in its early stages and the available systems have still very limited resources. As such, currently, the most practical way to develop and test quantum algorithms is to use classical simulators of quantum computers. In addition, the development of new quantum computers and their components also depends on simulations.

Given the characteristics of a quantum computer, their simulation is a very demanding application in terms of both computation and memory. As such, simulations do not scale well in current classical systems. Thus different optimisation and approximation techniques need to be applied at different levels.

This review provides an overview of the components of a quantum computer, the levels at which these components and the whole quantum computer can be simulated, and an in-depth analysis of different state-of-the-art acceleration approaches. Besides the optimisations that can be performed at the algorithmic level, this review presents the most promising hardware-aware optimisations and future directions that can be explored for improving the performance and scalability of the simulations.

CCS Concepts: • **Hardware** → *Quantum computation*; • **Computing methodologies** → **Simulation types and techniques;**

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1 Introduction

As we try to solve more and more complex problems such as developing new chemical compounds [139] or evaluating the physical properties of new materials [11], the demand for computational resources continues to grow. Certain problem cases are so complex that no existing computer system can solve them within a reasonable time. For such cases, *Quantum Computing* [143] is a promising emerging computing paradigm that can provide solutions to these problems [11, 24, 25, 38, 139, 141, 157, 191].

As quantum computing is still in its early stages of development, real machines are scarce and the existing ones have limited compute resources. Although several quantum computing experiments have shown promising results and quantum computers are being scaled up to hundreds of qubits [5, 7, 17, 103, 131], full quantum advantage has yet to be achieved.

In order for algorithms to be executed in a quantum computer, they are represented as quantum circuits. The ability of quantum computers to solve increasingly complex problems is limited by the maximum size of the executable quantum circuit. This size is mainly bounded by two factors: (1) the number of available qubits (the fundamental unit of a quantum circuit) and (2) the circuit depth, which refers to the number of distinct timesteps at which quantum gates are applied [143]. In current quantum computer implementations, not only are qubits few but also the time they are stable (i.e., their value remains reliable) is limited. This stable time is limited by the qubit implementation technology and also their sensitivity to fluctuations in the environment (e.g., magnetic fields and temperature).

Quantum circuit execution is just one element of the *Quantum Computing Stack* [9]. Other elements include mapping an algorithm to a quantum circuit, generating pulses to execute gates on qubits, and reliably reading out the results. To develop and test the various parts of the quantum computing stack, accurate and fast simulation tools are essential. Similarly to classical computers, different simulation tools are needed at various design and verification steps, each with a specific focus and level of detail. A generic quantum computer system is composed of different parts, and the development of each part can be assisted by a different type of simulation.

This review work focuses in particular on the simulation of the execution of quantum circuits. Simulations of quantum circuit execution can be performed at different levels, from simulating the behaviour of the quantum hardware platform [91, 158], to simulating the interaction between a few qubits and a coupler forming a gate [31, 73, 155], and simulating entire circuits [14, 96, 100, 158, 173, 183, 205].

While several simulators have recently been deployed and made publicly available, the need to simulate more complex algorithms, circuit configurations, or more accurately model qubit behaviour leads to an exponential increase in computational and memory demand for the simulations. Even on a supercomputer such as Summit [57], we can only do algorithmic simulations of a quantum circuit up to 47 qubits, which requires 2.8PB of memory [198]. Scaling up the simulations without increasing exponentially the amount of necessary resources, requires optimisations or approximations at different levels. As such, several classical computer techniques, such as data compression or optimised parallel execution, have been applied to reduce the memory requirements and accelerate the computations [12, 130].

Several review works on classical simulation of quantum computers are available, but their focus is different from the acceleration of the simulation. Some works focus on the state-of-the-art numerical methods, such as the work by Xu et al. [199] which gives a general overview, and Jones et al. [97] which focuses on the full-state simulation techniques. Other works focus both on reporting the state of the art for simulators as well as giving a high-level overview of the acceleration approach as in the work by Young et al. [202]. The work by Heng et al. [84] focus on presenting optimisations for GPU execution, while the review by Jamadagni et al. [93] focuses on setting up a benchmark for multiple simulators available, and comparing their performance. In contrast to the previous works, our work addresses the topic in a different way, with a goal of focusing on the possible hardware-aware acceleration techniques. It provides up-to-date details about the available simulator approaches, tools and techniques, and focuses on the possible optimisations for a broader selection of hardware platforms.

First, this review work presents an overview of the different types of simulators for the execution of quantum circuits. The simulators are organised into different categories, to help navigate the landscape of the available tools. Second, it provides an overview of acceleration techniques described in the state of the art to improve the performance of the simulations. Having a global overview of the existing proposed solutions, we will infer what the most promising trends are and speculate on the future directions for the acceleration of the simulation of quantum computers. In this context, different works propose different approaches to optimise the simulation on different hardware platforms, such as **Central Processing Unit** (**CPU**), **Graphics Processing Unit** (**GPU**), **Field Programmable Gate Array** (**FPGA**), or more complex setups such as a hybrid CPU and **Quantum Processing Unit** (**QPU**) core. A summary of the hardware-aware techniques observed in the analysed works is presented and this is used as a basis to extrapolate what the future directions in hardware-aware acceleration for quantum computer simulation should be.

The organisation of this survey is as follows. Section 2 introduces the essential concepts in quantum computing necessary for understanding the rest of the sections. In Section 3, we give an overview of the various parts of a quantum computer. Section 4 covers simulations at different levels and provides an overview of the available simulators for each of them, also introducing the main bottlenecks for scaling up the number of simulated qubits. Section 5 details the most common hardware platforms used for simulation. The following sections cover different acceleration methods, sorted by platform: CPU in Section 6, GPU in Section 7, and FPGA in Section 8. A summary and indication of future directions for hardware-aware optimisation is presented in Section 9 and Section 10 concludes this work.

2 Background

This section presents a quick overview and introduction to the basic quantum computer concepts.

2.1 Qubits

The fundamental computational element for the quantum computer is the qubit (quantum bit). Differently from normal bits, qubits can be in a state different from just $|0\rangle$ and $|1\rangle$: they can form a linear combinations of states, usually called a superposition:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle = \begin{pmatrix}\alpha\\ \beta\end{pmatrix}. \tag{1}$$

It is possible to visualise the state of the qubit on the Bloch sphere in Figure 1 using the equivalences [143]:

$$\alpha = \cos\frac{\theta}{2},\ \beta = e^{i\varphi}\sin\frac{\theta}{2}. \tag{2}$$

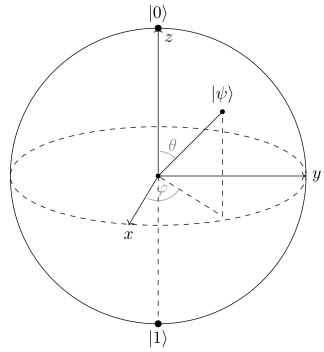


Fig. 1. Bloch-sphere representation of a qubit.

The vector is parametrised by two complex numbers, α and β, which are two probability amplitudes. As probability amplitudes they must satisfy the property $|\alpha|^2 + |\beta|^2 = 1$ [143]. In order to model the value of the qubits in a classical computer, for example for simulation purposes, it is necessary to store both α and β as complex values which requires a higher memory usage compared to storing the non-complex values in classical computers.

2.2 Quantum Gates

Quantum gates are the quantum equivalent of a logical gate. By applying a quantum gate to a qubit or multiple qubits, it is possible to control the probability amplitudes and thus change the state of the qubits.

2.2.1 Single-qubit Gates. Operations on qubits must preserve the norm $|\alpha|^2 + |\beta|^2 = 1$. therefore they are described by 2×2 unitary matrices. Some of the most important single-qubit gates are the Pauli gates:

$$X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \; Y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix} \; Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}. \tag{3}$$

These matrices correspond to the rotation of π radians around respectively the x, y, and z axes of the Bloch sphere.

Another important single-qubit gate is the identity matrix

$$I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}, \tag{4}$$

which does not affect the value of the qubit,

2.2.2 Multi-qubit Gates. Multi-qubit gates allow n qubits to interact together. The probability amplitudes required to represent an n-qubit system are 2^n. For instance, a 2-qubit system can be represented as:

$$|\psi\rangle = a_{00}\,|00\rangle + a_{01}\,|01\rangle + a_{10}\,|10\rangle + a_{11}\,|11\rangle\,. \tag{5}$$

Therefore, the matrix size for an operation on an n-qubit system is $2^n \times 2^n$. An important class of multi-qubit gates are the controlled gates. The control qubit values determine whether the controlled qubit's or qubits' value(s) will be controlled by the gate. An example of a 2-qubit gate in this class is the controlled-*NOT*, which applies a Pauli X gate on the target qubit if the control

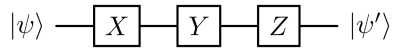


Fig. 2. A single-qubit circuit, which applies the Pauli gates X, Y, and Z in succession.

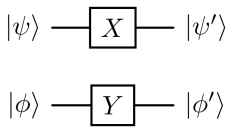


Fig. 3. A two-qubit circuit, which executes a Pauli X gate on the first qubit and a Pauli Y gate on the second qubit.

qubit is $|1\rangle$:

$$CNOT = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}. \tag{6}$$

Another example of multi-qubit gate is the Controlled-Z (CZ), which applies a Pauli Z gate on the controlled qubit in the case of a control qubit with state $|1\rangle$.

2.3 Quantum Circuit Execution

Quantum circuits are represented as in the diagram shown in Figure 2. Quantum gates are applied to a qubit in the time domain. Thus, the horizontal line connecting the different gates represent the time line (from left to right) of the different gates applied to the same qubit. In the case of a superconducting computer, this is done by controlling the single qubit with a specific pulse, and the gates are applied in successive instants of time. The circuit depth, as previously mentioned, is the longest path in the circuit, representing the maximum number of gates applied to a qubit. From a mathematical point of view, applying multiple gates can be represented as multiplying the gate matrices with the qubit state vector:

$$|\psi'\rangle = Z \cdot Y \cdot X \cdot |\psi\rangle\,. \tag{7}$$

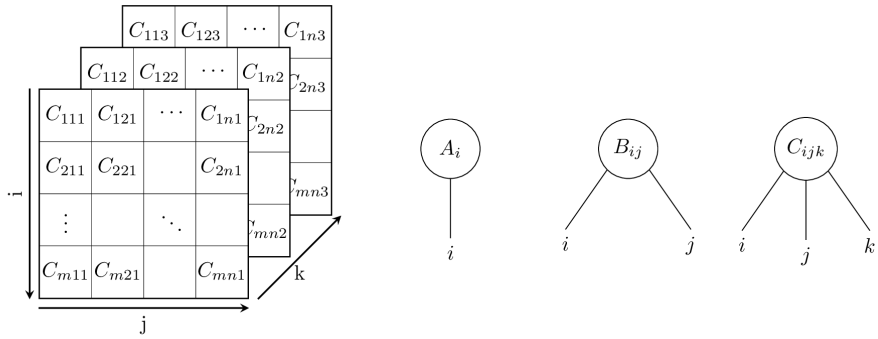
In case of circuits with multiple qubits and gates, the tensor product of two gates is equivalent to executing the gates in parallel. If we consider, for example, the circuit in Figure 3, it is possible to compute the gate matrices:

$$A = X \otimes Y. \tag{8}$$

The complexity of the classical model representation of a quantum circuit scales linearly with the circuit depth and exponentially with the number of qubits. This is because with n qubits there are 2^n possible states, and the size of the resulting matrix representing the parallel gates will be $2^n \times 2^n$. If there are j successive gates, there will be the need for $j \times 2^n \times 2^n$ matrices to represent the quantum circuit.

2.4 Tensor Networks

Some of the simulation methods are based on the representation and execution of the quantum circuit as a tensor network.



(a) (b)

Fig. 4. (a) Example of order-3 tensor, (b) An order-k tensor requires k-indices to be accessed.

For example, a vector A or a matrix B:

$$A = \begin{pmatrix} A_1 \\ A_2 \\ \vdots \\ A_m \end{pmatrix} \qquad B = \begin{pmatrix} B_{11} & B_{12} & \cdots & B_{1n} \\ B_{11} & B_{22} & \cdots & B_{2n} \\ \vdots & & \ddots & \vdots \\ B_{m1} & B_{m2} & \cdots & B_{mn} \end{pmatrix}, \tag{9}$$

are considered an order-1 tensor and an order-2 tensor, respectively while an order-3 tensor C is represented as shown in Figure 4(a).

A tensor network is a high-dimensional tensor that may be viewed as a graph where each node represents a tensor and the edges represent the connections between them.

A tensor of order-k is an object with k indices and can be represented with k legs [10, 56], as shown in Figure 4(b).

Quantum states can be represented through tensor networks, such as **matrix product states** (**MPS**) [163] or **project entangled pair states** (**PEPS**) [32]. In the simpler case of MPS, a quantum state can be represented by multiplying a tensor with the value of the individual states S_i:

$$|\psi\rangle = C_{S_1 \cdots S_n} |S_1 \cdots S_n\rangle . \tag{10}$$

The tensor C can be decomposed in multiple tensors A_i. We define the size of the tensor A_i with the bond dimension d_i, such that the dimension of the tensors A, i.e., in case of a even number of qubits (n), is $(1 \times 2), (2 \times 2^2), \ldots, (2^{\frac{n}{2}-1} \times 2^{\frac{n}{2}}), (2^{\frac{n}{2}} \times 2^{\frac{n}{2}-1}), \ldots, (2^2 \times 2), (2 \times 1)$. We can fully describe the tensor C such as

$$C_{S_1 \cdots S_n} = \sum_{d_1, \ldots, d_n} (A_1)^{d_1}_{S_1} (A_2)^{d_2}_{S_2 d_1} \cdots (A_n)_{S_n d_{n-1}}. \tag{11}$$

To compute the exact value of the states, we would need $\approx 2^n$ values to describe the MPS, equal to the number of values needed in case of the state-vector simulation. The maximum bond dimension needed to describe the exact value of the states is $2^{\frac{(n-1)}{2}}$ or $2^{\frac{n}{2}}$ depending on whether the number of qubits is odd or even, respectively. By choosing a smaller value for the maximum bond dimension, consequently pruning values in the bigger matrixes, we decrease the complexity of the problem but we introduce an approximation error which is proportional to the entanglement level of the described system [32].

Fig. 5. The tensors D and E are contracted into a single tensor F, with indices i and k.

In order to work with tensors, the main operation is the tensor contraction, shown in Figure 5. Contracting two tensors means performing a summation over an index, which contracts the internal indices between the two tensors, mathematically represented as

$$F_{ik} = \sum_j D_{ij} E_{jk}. \tag{12}$$

The usual approach to handle the tensor networks is to contract the network from order k to a single tensor. When the network contraction is divided in a sequence of binary contractions, the total computational cost is influenced by the choice of the contraction sequence. Working with pairwise contractions typically enables optimal computational performance, as they can be implemented as matrix-matrix multiplication [56].

3 Quantum Computers

Since the beginning of quantum research various algorithms [141] have been explored to verify if a quantum computer could solve some problems faster than classical machines. Examples of such quantum algorithms are Shor's algorithm [166], Grover's search algorithm [74], and quantum simulation [66, 143]. Shor's algorithm, based on the quantum Fourier transform [143], can be used to find the prime factors of an integer. Grover's search algorithm allows to speed up the search for an element which satisfies a certain known property. It allows in the case of a search space of size N to find an element with no prior knowledge about the structure of the information in $O(\sqrt{N})$ operations instead of the $O(N)$ operations required classically [143]. Quantum simulations are simulations of naturally occurring quantum mechanical systems, such as molecules, using quantum computers [143].

Quantum computers utilise different quantum chip technologies, including ion trap [21, 64, 102, 179], neutral atom [17, 85, 195, 201], semiconductor [40], and photonic [108, 131, 145, 160, 172, 210]. This work focuses on the currently most common technology used to build quantum computers: the superconducting architecture [65, 75, 191]. Figure 6 shows the generic structure of a superconducting quantum computer. The high-level scheme for the other quantum chip technologies is similar to the one shown, as there is always the need to control the chip through control signals and read out the output afterwards [160, 179, 195].

3.1 Quantum Chip

The quantum chip, which includes the physical qubits, is the main component of the quantum computer. Depending on the technology, they are controlled and connected in different ways. Connecting multiple qubits together allows for more complex circuits, comprising single- and multi-qubit gates.

As already mentioned in the introduction, one of the main limitations of current physical qubits is their short coherence time. This is the timescale of the exponential decay of the qubit superposition state [4]. The correctness of quantum computers is usually measured in terms of a fidelity for the operations or the output state.

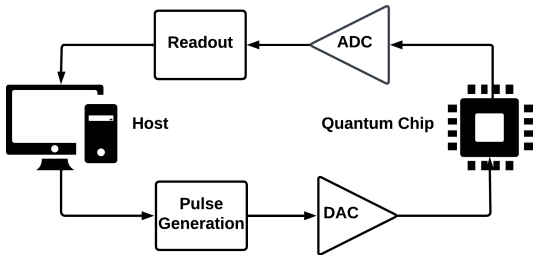


Fig. 6. Basic scheme for a superconducting quantum computer and its control electronics. The control pulses generated are converted from digital to analog through the DAC. The analog output of the quantum chip goes through an ADC and is then read.

Coherence times vary depending on the technology and the "quality" of the qubit. A different metric that allows to compare different technologies and different approaches is the amount of gates that can be executed during the coherence time of a single qubit. In the case of the current superconducting qubit implementations, they have a coherence time ranging from hundreds of microseconds [22, 159, 168], up to close to a millisecond [177]. Consequently, the control system, responsible for providing pulses to activate the qubits and read out their state, must be fast enough to be able to control thousands of gates during this time.

Although some technologies, such as photonics, allow the quantum chips to work at standard room temperature, most of the other approaches require the chips to be cooled down to a temperature close to absolute zero to avoid thermal noise. Therefore, the chips are usually are placed inside cryogenic chambers. This introduces additional challenges related to controlling and communicating with the chips from other components of the quantum computer. If placed inside, the components need to operate at the low temperatures of the chamber and are forced to dissipate minimal power, while if placed outside the chamber, they face a bottleneck in scaling due to the physical limit of input and output cables available. In additional to the physical number of cables, each cable also carries heat into the chamber, thus increasing the thermal noise [112].

3.2 Pulse Generation

The qubit driving mechanism may vary depending on the type of quantum computers we briefly discussed in the previous section. Independently of the chip technology, there is always the need to use control signals, which would be in form of some pulses [160, 179, 195]. In the case of the superconducting architecture, qubits are controlled by radio-frequency signals. Each qubit is characterised by a slightly different resonance frequency, which allows to drive them individually [109, 111, 150]. The specific resonance frequency can vary slightly in time due to interaction with impurities in the qubit environment, affecting the fidelity of operations on each qubit. Therefore, periodic recalibration of the system is necessary [22, 192, 196]. This recalibration process allows to update the correct resonance frequencies used to control the qubit by the pulse generation hardware. Scaling up the number of qubits requires additional inputs to the system, which, as previously mentioned, becomes a major challenge for technologies that require a cryogenic chamber for cooling.

3.3 Readout

After the execution of the quantum circuit, the value of all or some output qubit must be measured. The main challenge is that discrimination between zeros and ones is non-trivial, leading to the development of various readout techniques [8, 27, 46, 104, 111, 138, 156, 174]. The approaches range from improved amplification of the output at the analog level [8, 104, 156] to the introduction of

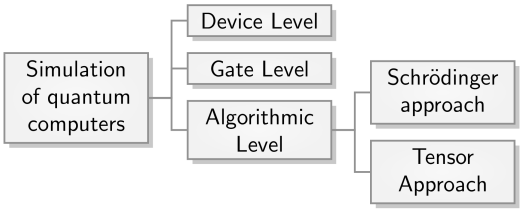


Fig. 7. Taxonomy of simulation of quantum computers.

error correction for fault-tolerant quantum computing using higher-abstraction level techniques such as machine learning [138]. The main issue, as in the case of the pulse generation, is related to managing the connection between the readout system and the quantum chip through the cryogenic chamber, which is one of the major bottlenecks in scaling up the system.

3.4 Compiler

Mapping an algorithm to a quantum circuit is a non-trivial task. To do this, we use specific tools such as a compiler, which must take multiple decisions. Ideally, the compiler would assign each qubit in the algorithm to a physical qubit in the quantum computer, without considering the different error probabilities of each qubit. In this case, all the multi-qubit gate operations would occur between neighbouring physical qubits, giving the compiler freedom to choose any quantum gate operation.

In a real quantum computer, this is not always possible. First, different qubits on the same chip could have different probabilities of error due to the influence of the external environment. When reading the output of a qubit, the output might not always be correct, due to factors such as drifts in calibration, temperature variations, or measurement errors. Therefore mapping the operations to qubits according to their probability of error might increase the fidelity. Additionally, in some architectures, such as superconducting circuits, qubits can only interact with neighbouring qubits, requiring the addition of SWAP operations when direct interaction is not possible [146, 170, 200, 204].

Not every gate might is available on every quantum computer, and the choice of gate can influence the output fidelity. Multiple approaches [29, 37, 39, 120, 126, 149, 171, 190, 197, 204, 211] have been proposed to address this issue, aiming at optimising the mapping of quantum circuit to the available qubits and gates. Thus, it is very important that the compiler considers all the characteristics of the available system as a sub-optimal compilation phase may result in resource under-utilisation, high error rate, and lower fidelity [126].

4 Simulations of Quantum Computers

In this section, we focus on how we can simulate, and optimise the simulation of, the execution of quantum computers. Simulations are becoming an increasingly valuable tool for evaluating and developing various components of the quantum computer stack. As in classical computing, each part of the system requires a distinct approach and level of detail.

Simulations of quantum computers can be classified into the following three main categories, as also shown in Figure 7.

— **Device level** — this is the lowest level of the system and focuses on the materials and the implementation of the qubit. This is comparable to the low-level classical hardware simulation.
— **Gate level** — this is the middle level, where gates are mapped to qubits. This is comparable to the micro-architecture-level classical simulation.

— **Algorithmic level** — this is the highest level of the system, where algorithms are mappped to quantum circuits. This is comparable to the functional-level classical simulation.

Although it is possible to simulate a complete quantum computer for a small number of qubits, this does not scale well for increasing number of qubits. This issue arises at every level and it is better described in each subsection. In general, the simulation execution is both memory- and compute-bound. With scalability in mind, simply trading one for the other is insufficient to achieve the desired performance, as beyond a certain number of qubits, one of the two limitations will become impossible to overcome.

We should notify the reader that in this work, we will not focus on the acceleration of device-level or gate-level simulations, as there are already plenty of solutions [53, 61, 161, 212]. Instead, we will focus on the research field of algorithmic-level simulation.

4.1 Device Level

Device-level simulations help address the mechanical, thermal, and electromagnetic aspects of the problem. In the case of superconducting circuits, some mainstream commercial tools are reported here:

— Ansys Electronic Desktop [90] solves 3D Maxwell equations, and eigen-equations with various boundary conditions, including the option for lumped-element boundary conditions. This is useful for nearly all problems in the electromagnetic domain at RF and microwave frequencies.
— COMSOL Multiphysics [3] is a **Finite Elements Method** (**FEM**) solver of many partial differential equations of physics. It is useful for simulating thermal, mechanical, and electromagnetic problems. London's equations can be solved to simulate the Meissner effect in packages, chips, resonators, as well as effects of kinetic inductance. Heating or cooling of circuits and the impact of mechanical strain on packages or **Printed Circuit Boards** (**PCBs**) can also be simulated.
— SolidWorks [36] can be used for designing of mechanical parts such as nuts and bolts, packages, fixtures, heat sinks, and connectors. Designs can be exported and re-imported in Ansys tools for electromagnetic simulations. It is also possible to export the FEM mesh for use in other FEM-based simulators. FreeCAD is an open-source (python-based) version of this tool.
— InductEX [92] from SunMagnetics Inc. solves London's equations using FEM and is primarily used for extracting inductances in the layout of superconducting circuits, such as **Rapid Single Flux Quantum** (**RSFQ**) logic gates.

Different types of simulators will be used in quantum dot technology, such as Intel Quantum Dot Simulator [100] and nanoHUB Quantum Dot Lab [105, 106]. Although related to different technologies, the simulators can be classified at the same device level. They evaluate the selected material and geometry and calculate information such as 3D visualisation of the confined wave functions, incident light angle and polarisation, and isotropic optical proprieties [105, 106].

4.2 Gate Level

Gate-level simulation focuses on the interaction between a few qubits connected by couplers, which are used to implement quantum gates. Evaluating different configurations is necessary to study and define the actual gates that will be used in quantum circuits.

An example circuit used for gate-level simulation is shown in Figure 8. Simulations at this level are based on solving differential equations derived from the Schrödinger equation [95].

There are different types of simulations at this level. Static gate-level simulation is useful for evaluating the energy levels of qubits and couplers, as well as assessing the interference between

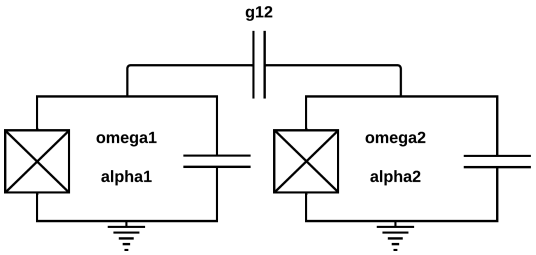


Fig. 8. Simple circuit used for gate-level simulations, composed of two qubits and one coupler to connect them. Each qubit is modelled as a Josephson junction and a capacitor. In the circuit simulations a capacitive coupling is used to connect the two qubits [63, 155].

them. Dynamic gate-level simulation helps evaluate the effects of a pulse used to control the gate. This is crucial for determining the type and frequency of pulse needed on the quantum chip to ensure each qubit responds as expected.

Examples of simulations at this level are CSQR [63, 155] and scQubits [31, 73]. The gate-level simulation acceleration is based on the optimisation of the differential equation solution. Other simulators, such as QuTiP [94, 95], allow for run-time optimisation of the type of solver and hardware configuration, enabling faster simulations or reduced memory usage. Dynamiqs [77] is another simulator that can run on CPU, GPU, and TPU, offering speedup through batching and parallelisation on CPUs and GPUs. Another simulator at this level is QuantumOptics.jl [110], but no information on the acceleration is available.

4.3 Algorithmic Level

Algorithmic-level simulation is useful for testing the correct functioning of potential quantum algorithms. Although we mentioned previously in Section 3 that this work focuses on superconducting architectures, simulation of algorithms is generally platform-independent.

One such algorithm is Shor's 9-qubit error-correction code [166] shown in Figure 9. Unlike device-level simulations, algorithmic-level simulations generally treat the quantum circuit as a sequence of matrix operations [143]. Simulations may include noise, which models external factors such as temperature, electrical interference and additionally device changes in time, that may affect the state of the qubits. Noisy quantum states are represented as a density matrix, which requires more storage than the vector of a pure quantum state. Consequently, including the noise model in the simulation leads to higher accuracy of the simulated system but results in increased problem complexity and thus higher demands on the computational resources [49]. In contrast, we can exploit the fact that a lower simulation accuracy would match the real output of the noisy quantum circuit, therefore leading to lower computational demands [135]. Consequently, noiseless simulations need less memory and compute time, but they are farther from real-world conditions. Nowadays, we are moving towards **Noisy Intermediate-Scale Quantum** (**NISQ**) computing [16, 157]. Introducing noise in the simulations can provide a better correlation between simulation and real-world results. Below is a list of some of the most common algorithmic-level quantum circuit simulation tools available for use:

— Intel Quantum SDK [100]: Provides two different simulators with two different modes of simulation, Generic Qubits and Intel Hardware. The Generic Qubits simulation is a state-vector-based simulation, which uses as a backend the Intel Quantum Simulator, allowing for a qubit-agnostic execution. The Intel Hardware mode uses as its core the Quantum Dot Simulator, which simulates the Intel quantum hardware, currently under development.

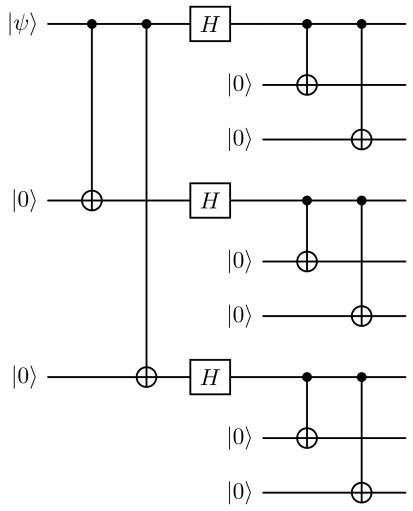


Fig. 9. 9-qubit Shor's code circuit for error correction [167]. Different gates are used in this circuit: multiple Hadamard gates which change the qubit state to the superposition state, and CNOT gates [143].

- QuEST [96]: Simulator using state vectors and density matrices [143] for quantum circuits, which uses multithreading, GPU acceleration, and distribution to optimise the execution on multiple types of devices such as laptops, desktops, and networked supercomputers.
- Qiskit [158]: Open-source SDK for working with quantum computers. Used as the core library for different types of simulations. It allows both for noiseless and exact noisy simulation with Qiskit Aer [158].
- HyQuas [205]: This is a hybrid partitioner-based quantum circuit simulator, optimised for GPUs. It selects the optimal simulation method for different parts of a given quantum circuit. It implements additional solving methods and makes use of distributed simulation.
- qTask [88]: Quantum circuit simulator that focuses on optimising the speed in case of modifications of a small part of the circuit, defined as incremental simulation. When this happens, the state amplitudes (probability amplitudes of the state) are incrementally updated, removing the need for simulating the whole circuit every time.
- PennyLane [14]: Open-source software framework for quantum machine learning, quantum chemistry, and quantum computing. Supports GPU acceleration by making use of NVIDIA cuQuantum SDK [12].
- QuTip-qip [119]: QuTiP quantum information processing package, which offers two approaches to quantum circuit simulation. The algorithmic-level approach is based on the circuit evolution under quantum gates by matrix multiplication, while another approach uses open system solvers in QuTiP [94, 95] to simulate noisy quantum devices.

While gate-level simulations focus on the full time evolution from the start to the end of the gate, algorithmic-level simulations consider only the changes that the gate's corresponding matrix applies to the state vector. Although these simulators provide less detail, they allow for faster simulations or alternatively an increased number of simulated qubits. However, they are also constrained by memory and time. The memory required to simulate a circuit is determined by the number of qubits, the number of gates, the data representation, and the number of times the circuit is executed, which, in the case of a real quantum circuit, corresponds to the number of measurements.

Most simulators are designed for algorithmic-level simulation, which is the furthest from actual physical implementation and allows for evaluating problems from a hardware-agnostic perspective. Quantum simulations at the algorithmic level can be categorised into four main types of approaches:

— Schrödinger-style simulation [143]
— Feynman-style simulation [15]
— Tensor-based simulation [136]
— Stabiliser simulation [2]

While the Schrödinger and Feynman approaches have been the primary methods in the past, there is now a greater focus on exploring the potential of the tensor-based approach.

4.3.1 Schrödinger-style Simulation. Schrödinger-style simulation, also known as state-vector-based simulation, is the mainstream technique for general-case simulation of quantum algorithms, circuits, and physical devices. As described earlier, a quantum state is represented by a vector of complex-valued amplitudes, and the primary approach in this simulation is to store the current state vector and iteratively multiply it by a state transformation matrix [88].

Schrödinger-style simulation resources scale linearly as a function of the circuit depth and exponentially as a function of the number of qubits. Additionally, it allows for relatively straightforward implementations that are commonly used for small and mid-size quantum circuits and device/technology simulations [60].

4.3.2 Feynman-style Simulation. Feynman-style path summation considers each gate connecting two or more qubits in a quantum circuit as a decision point from which the simulation branches. The final quantum state is obtained by summing up the contributions of the results of each branch, which are calculated independently. In comparison to Schrödinger-style simulations, traditional Feynman-style path summation [1] uses very small amounts of memory but doubles the runtime on every (branching) gate. This results in a much longer runtime and does not allow for optimal memory usage, as the number of paths grows exponentially as a function of the decision points. Unlike traditional Schrödinger-style simulation, Feynman's resulting algorithms are depth-limited, making them a good fit for near-term quantum computers that rely on noisy gates [135].

4.3.3 Schrödinger-Feynman Hybrids. A possible approach to leverage both Schrödinger and Feynman approach is Schrödinger-Feynman hybrids [1, 30], proposed in the work of Markov et al. [135]. In the context of nearest-neighbour quantum architectures [7, 18, 103], where the qubit array is partitioned into sub-arrays, the Schrödinger approach is applied to each sub-array. This reduces the memory requirements for k qubits from 2^k to $2^{\frac{k}{2}+1}$, although this introduces a dependency on the number of gates acting across the partition.

The gates are decomposed into a sum of separate terms to allow for independent simulation, but this also results in an increase in execution time. For example, in the case of a CZ gate, the gate can be decomposed into two terms, which results in doubling the run time. However, this increase in run time is still lower compared to the Feynman-style path summation described earlier.

4.3.4 Tensor-based Simulation. The Schrödinger approach typically stores the full state of the qubits, allowing for the simulation of arbitrary circuits. However, the downside is the exponential increase in memory requirements. For an n-qubit system, $O(2^n)$ space is needed.

When using the tensor-based approach, the quantum circuit is described as a tensor network, with each n-qubit gate represented as a rank-$2n$ tensor. This transforms the simulation into a problem of contracting the corresponding tensor network. Tensor network contraction is performed by convolving the tensors until only one vertex remains. For circuits with a large number of qubits and shallow depth (as complexity often grows exponentially with circuit depth), this method is

highly efficient. Thus, using tensor networks allows for the simulation of only one or a small batch of state amplitudes at the end of the circuit. The complexity of the tensor network is constrained by the largest tensor involved in the contraction process.

4.3.5 Stabiliser Simulation. Stabiliser simulations are used for Clifford circuit simulators, quantum circuits that are easy to simulate for classical computers since they only use Clifford gates, start in the computational basis state, and measure in the computational basis. Then Clifford gates can just take you between six points on the Bloch sphere (±1 on the x, y, and z axes). This is described in the Gottesman-Knill theorem [71]. Such circuits are easy to simulate for hundreds, thousands, or more qubits [13, 20, 33, 70, 134]. Qiskit [158] is one of the tools which allows for stabiliser simulations. Stim [68] is also a popular such simulator for studying error correction, made by Google's expert on the topic. IBM also proposed such type of simulation [19]. A famous early work on simulation with stabiliser circuits is presented in [2]. Some works also present a hybrid simulation that combines stabiliser simulation and tensor-network simulation [137]. While the stabiliser simulation is limited to Clifford circuits, several works present ways to modify generic circuits to be able to apply this simulation. This is done by extracting Clifford subcircuits [125, 175] or recompiling the circuit to Clifford gates entirely [68]. The acceleration of stabiliser simulations will not be covered by this survey, as it is limited to Clifford circuits only, while our focus is on accelerating the simulation of generic circuits.

5 Simulation Hardware Platforms

Based on the size of the problem, various hardware platforms with different computational power can be used to run the simulations. Nevertheless, all of them will eventually be limited by either the required memory or the simulation time. The exponential growth of memory and simulation time is the reason for the relevance of the simulation optimisation efforts, which will be discussed later in Sections 6 to 8. A diagram presenting the techniques discussed in this work is depicted in Figure 10.

5.1 Small-scale Quantum Simulation

Currently, an algorithmic-level simulation of 30 qubits with Intel quantum SDK [100] requires up to 34 GB of free RAM. Increasing this by just two additional qubits would require up to 135 GB. This means that with today's technology, even a common personal computer can be used for a moderately small number of qubits. A simulation with another algorithmic-level simulation tool, qTask [88] on a CentOS 64-bit machine with 16 Intel i7 cores at 2.50 GHz and 128 GB RAM, will take on average 991.4 ms to run a 26-qubit Ising model simulation, or 2209.7ms to run a 20-qubit Quantum Fourier transform, with respectively 114.3 GB and 91.2 GB RAM [88]. Personal computers are the most commonly available platform for running simulations, primarily using the CPU and, in some cases, the GPU. Personal computers can also be combined with an external FPGA, which allows off-loading some of the work. As described in Section IV-C, in state-vector simulations, the core operation is matrix multiplication, which, if properly handled due to the use of complex numbers, can be processed inside the FPGA and the results then transferred back to the CPU.

5.2 Medium-scale Quantum Simulation

Scaling is quite an issue in quantum computer simulations, as mentioned earlier. This increase in computational resources can be supported by better simulation hardware, such as workstations. These are typically equipped with state-of-the-art CPUs and one or more GPUs, offering more memory compared to a standard personal computer. This enables the simulation of a larger number of qubits, although still limited due to the exponential scaling of memory requirements. With current

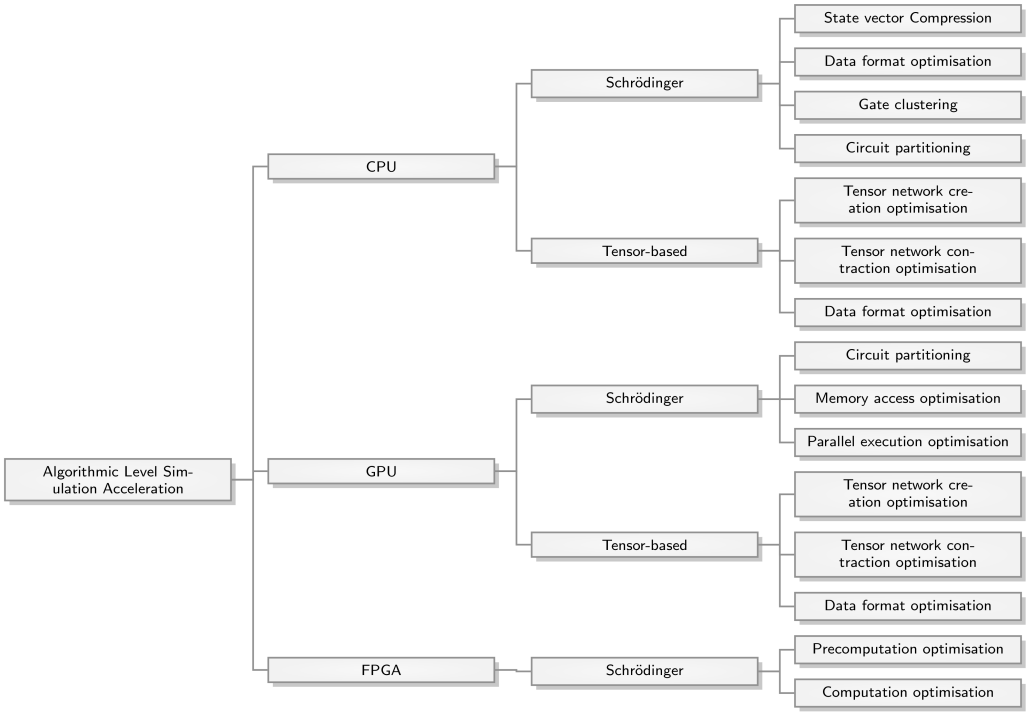


Fig. 10. Summary of acceleration methods.

technology, simulating up to 32 qubits is possible using commercially available workstations [100]. Another factor to consider is the simulation time. Upgrading to workstations, especially those equipped with multiple GPUs, generally enables faster execution if the simulator is optimised for parallel execution. Additional speedup can be achieved if the workstation has a processor with a matrix unit [176], which allows for quicker execution of core operations. The simulation of a quantum Fourier transform with 36 qubits on one node of Argonne [113] requires 192GB of memory and can be run in more than three days [198].

5.3 Simulation Beyond the Medium-scale

If the goal is to run simulations with the highest possible number of qubits or at the fastest speed possible, a high-performance computer is required. An example of this is the execution of 61-qubit quantum circuits [198] on Argonne Theta [113] using qHIPSTER [173], an earlier version of the Intel quantum simulator [100]. The simulation, although optimised, required 0.8 Pb of memory, a level of resources not available on standard laptops or workstations. The advantage of high-performance computers is that they are equipped with multiple nodes, each composed of multiple CPU cores or GPUs, allowing for significantly better performance compared to a single laptop or workstation. The simulation of a Grover search with 61 qubits on 4,096 nodes of Argonne [113] requires 768 TB of memory and can be run in more than 8h [198].

6 Acceleration using CPU

CPU simulation acceleration focuses mainly on scalability, and in particular, most of the work reported here tries to optimise the simulation on big clusters of CPUs, with high-performance computers such as Summit [57], Sierra [114] (Lawrence Livermore National Laboratory), or Theta [113]

Table 1. Summary of the most Important Acceleration Works Performances with CPU

Work	Simulation type	Baseline	Improvement (Scaleup / Speedup)	Benchmark Platform
[130]	Tensor-based	120-qubit QAOA [209]	210-qubit QAOA in 64 s	Argonne Theta Supercomputer
[127]	Tensor-based	81-qubit RQC, 40 depth [26]	100-qubit RQC, 42 depth in 304 s	Sunway Supercomputer
[58]	Schrödinger	30-37 qubits circuits in range range10100 s [76]	up to 5.67× speed-up	Workstation, Frontera Supercomputer
[135]	Schrödinger	45 qubits, 26 depth, 0.5PB mem [81]	45 qubits, 27 depth, 17.4GB mem in 1.4 h	Google Cloud
[60]	Schrödinger	36 qubits in 194.12 s [184]	36 qubits in 94.48 s	Linux Server
[121]	Schrödinger	49 qubits, 27 depth in ≥24 h [154]	49 qubits, 27 depth in 1.49 h	Sunway Supercomputer
[198]	Schrödinger	47 qubits, 2.8PB mem [143]	61-qubit Grover's search, 0.8PB mem	Argonne Theta Supercomputer
[43]	Schrödinger	45 qubits, JUQCS-E [43]	48 qubits in 300 min	K Computer (RIKEN)

For each work, the baseline simulated circuit is shown, as well as, the memory consumed and execution time, whenever reported. The Improvement shows each work's achievements, as presented by the authors, including scaling of the problem, speedup and/or memory reduction.

(Argonne National Laboratory). The optimisations presented are classified by their approach: Schrödinger or Tensor-based. Table 1 summarises all the results.

6.1 Schrödinger-style Simulation Acceleration

As described previously in Section 4.3, accelerating Schrödinger-style simulations consists of speeding up the core matrix multiplication. Different approaches have been taken to achieve improvements.

6.1.1 Baseline Simulation Algorithm. The most mathematically simple way to execute full state-vector simulations for an n-qubits circuit with quantum gates, reported in the work of Fatima and Markov [60], is to

(1) Order the gates left to right
(2) Execute each layer of gates in parallel. All qubits must go through either an actual gate or an identity matrix; therefore pad each gate with an identity matrix of an appropriate dimension via Kronecker products to obtain a $2^n \times 2^n$ matrix
(3) Multiply all matrices in order

This allows the entire circuit to be represented as a matrix, and multiplying it with the input state vector produces the output. Although it is a simple algorithm, it is not the most efficient method in terms of memory utilisation and parallelising computations. Another straightforward approach is to apply each gate directly to the input state vector. Generally, in most works, the simulations are performed in two main steps. The first step is to partition the circuit into multiple sub-circuits, which can be executed in parallel, eventually grouping or reordering gates within the same partition. The second step involves adopting various strategies to optimise the execution. Additional techniques, such as compression and optimising the data format, can further enhance performance.

6.1.2 State-vector Compression. One of the main issues of the Schrödinger simulation, mentioned already before, is memory usage. Storing the full state vectors during the simulation requires an exponentially increasing memory space. A possible solution, used already in other applications that handle vast volumes of data, is the use of data compression techniques.

There are mainly two types of compressions: lossless compression [47, 140, 185] and error-bounded lossy compression [34, 115, 122–124, 162]. Introducing a module in the simulation workflow that compresses the state vectors before storing them in memory and decompresses them when needed helps address the memory usage problem.

Lossless compression is an approach used in works such as Zhao et al. [208]. The authors report an incremental improvement by stacking multiple methods, and compared to the previous method is 13.29% better for the largest number of qubits (34), which can run on their platform. Their work focuses on reducing the data transfer between CPU and GPU, and one of their contribution is the

lossless data compression of non-zero amplitudes, achieved by observing how the state vector after each operation has similar amplitude values. Lossy compression of state vectors is the approach used in works such as Wu et al. [198]. That approach allows to simulate Grover's search algorithm, as well as other quantum algorithms such as **Quantum Approximate Optimisation Algorithm** (**QAOA**) [59] and random circuit proposed by Google [62], with up to 61 qubits. This is achieved by compressing the state vectors and reducing the memory size required from 32 EB to 768 TB. For the data compression, the authors implement an error-bounded lossy compressor, a technique that limits the compression ratio based on the corresponding fidelity loss. It is possible to select the optimal compression strategy during different parts of the simulation, using Zstd [140] alongside an error-bounded lossy compression method developed by the authors [198].

Another approach, presented in [43], is to use an adaptive encoding scheme based on the polar representation $z = re^{i\theta}$ of the complex number z for the state-vector elements. One byte is used to encode the angle $-\pi \leq \theta \leq \pi$ and the remaining bytes encode the value r, after scaling based on the maximum and minimum values of the state vector. This allows for a reduction in the amount of memory required to store the state by a factor of 8, but it requires additional time to perform the encoding and decoding procedure, up to a factor of 3-4.

6.1.3 Data Format Optimisation. While the 64-bit double representation is the most common approach to the data representation [43], there have been efforts to reduce the number of bits required to obtain results with a good enough fidelity. This allows for a lower memory footprint and higher throughput.

The work of Fatima and Markov [60] uses the 32-bit float type representation instead of the more common 64-bit double type, therefore reducing the total amount of necessary resources. The approximation error is controlled by globally keeping track of the changes in amplitude for changes bigger than $\frac{1}{2}$.

This is done because most of the gates do not significantly change the amplitude value. Gates more commonly act on the phase, so the result is not at risk of underflow. An underflow occurs when the result of an arithmetic operation is relatively so small that it cannot be stored in the input operand format without resulting in a rounding error that is larger than usual.

But some gates, such as the Hadamard gates, can change the amplitude by a factor of $\frac{1}{2}$ or $\frac{1}{\sqrt{2}}$, generating underflow issues with the 32-bit float representation. In this case, the change is tracked and included at the end of the quantum circuit, allowing the reduction of memory needed while still obtaining results with good fidelity.

The same research group published a follow-up work [135] where their simulation acceleration techniques are optimised in terms of parallelisation, with a focus on allowing the simulation to be run on generic hardware.

6.1.4 Gate Clustering and Circuit Partitioning. Simulating gates one at a time, as described in the baseline algorithm, is slow because it requires separate memory traversals [60]. A common technique to avoid this issue is to simulate gate clusters in batches. A gate cluster is obtained by combining the matrices representing the gate matrices acting on one or multiple qubits. The common approach is to cluster adjacent gates acting on the same qubit. Google QSim [184] merges each one-qubit gate to some nearby two-qubit gate. Another work [81] applies gate clustering to a larger amount of qubits, up to five, and then multiplies out the obtained gate matrices.

The work of Fatima and Markov [60] creates clusters of q qubits out of the total amount of n qubits that grows as $O(q^2)$. They apply gate clustering by reordering, a technique that loops over the circuit and clusters adjacent gates of the same type or reorders non-adjacent gates to form larger clusters, allowing for optimised algorithms for each type of cluster. The approach of qTask [88] is

to partition a state vector into a set of blocks, with each partition spawning one or multiple tasks performing gate operations on designated memory regions. This, as the previous techniques, allows to enable inter-gate operation parallelism due to the breaking down of the gate dependencies.

Another strategy presented in [121] is the technique named implicit decomposition. The target circuit is efficiently partitioned into different parts with a focus on balancing the memory requirements for each one of them. This efficient partitioning allows to save memory space compared to storing the entire state vector, because it is not necessary to have all the amplitudes after the individual calculations. They additionally propose a dynamic algorithm to select the optimal partition scheme.

6.1.5 Memory Access Optimisation. Given that the execution is dominated by matrix multiplication operations, an obvious optimisation is to do them in a cache-friendly way, resulting in improved performance [58]. Memory locality can be exploited with gate clustering. If paired-up gates act on qubits as closely as possible, it reduces memory strides (distance between two successive elements of an array in memory) when simulating gate pairs acting on less significant bits [60].

Another technique, described in [60], is cache blocking, where rather than applying pairs of qubit gates in separate passes, such pairs, acting on different qubits, are reordered and applied partially in different orders. Each state vector is divided into chunks, which fit in the L2 cache, and for each chunk, multiple non-overlapping pairs of one-qubit gates and an occasional unpaired gate are applied to it. This reduces the cache misses and improves the performance. The work of Fang et al. [58] tackles the memory locality with their hierarchical simulation framework. The authors consider that scaling up means the working set size of the simulation set would exceed the cache size of a modern CPU. To address this, the input circuit is executed as a sequence of sub-circuits, each containing a portion of the original gates, allowing for better locality.

6.1.6 Parallel Execution. Efficiently handling the parallel execution of different gates or tasks is crucial to capitalising on the advantages introduced by the circuit modifications mentioned earlier. Most works utilise a multi-CPU approach with OpenMP and MPI-based CPU simulations. The work of Fatima and Markov [60] explains in detail how to exploit CPU architecture to simulate different clusters, exploring data-level parallelism.

6.2 Tensor-based Simulation Acceleration

Tensor network-based simulations are divided into two main steps. The first one is to represent the quantum circuit as a tensor network. The second step is to apply the contraction to the tensors, as described previously in Section 2.4. We now present the different acceleration solutions for each step of the simulation.

6.2.1 Tensor Network Creation. For the first step of the simulation, different approaches can be taken depending on the type of algorithm and the structure of the quantum circuit. In the case of **Random Quantum Circuits** (**RQC**), a viable solution is using PEPS representation of quantum states from many-body quantum physics [127]. This representation, according to [127] works for $2N$ by $2N$ lattice types, but to work with different structures, the generation of the best contraction path (choice of which nodes to contract at different steps of the simulation) becomes a bigger issue. A possible approach is to use the CoTenGra software [72] to look for the best path. It uses a loss function that combines the considerations for both the computational complexity and the compute density, which are determinant factors for the performance on a many-core processor [127]. Another approach is to use ordering algorithms. There are several available ordering algorithms, classified as

— Greedy algorithm: usually used as a baseline, contracts the lowest-degree vertex in a graph.
— Randomised greedy algorithms: The computational cost of the contraction at each step is function of the maximum number of neighbours for a node. Minimising this by choosing the

optimal contraction order allows for a decreased computation cost. This approach can do so without prolonging the run time [130].
— Heuristic solvers: Attempt to use some global information in the ordering problems. Example of this are QuickBB [69] and Tamaki's heuristic solver [181].

6.2.2 Tensor-network Contraction. Depending on the optimisations done during the tensor creation step, the contraction can be more or less efficient. During the contraction phase, an optimal slicing method is required to divide the tensor network into different clusters. This allows an efficient parallelisation of the computations, to efficiently process all the sub-tasks of the circuit across all the available nodes. This is necessary to balance the compute and storage costs. In the graph representation, the contraction of the full expression is done by consecutive elimination of graph vertices. The consequence is that the vertex is removed from the graph and the neighbours are connected [130]. The slicing of a tensor over an index means evaluating many variables while keeping one of them constant. Finding the optimal index to slice is the focus of this process. An approach to this is to select the best index after each step of the slicing, a method known as step-dependent slicing [130].

Another approach is to divide the contraction into two steps, the index permutation of the tensors as a preparatory step and the second step is the following matrix multiplication to achieve the contraction results [127]. Permutation of indices is generally required to convert the tensor contractions into efficient matrix multiplications. In the case of tensor contraction on many-core processors with a high compute density of high-rank tensors, it is important to reduce the permutation cost to reduce the movement of data items with strides in between, which is unfriendly for current memory systems [127, 188]. A proposed approach is to use fused permutation and multiplication, which means using different compute processing elements in a collaborative way [127], where each CPU reads its corresponding data block in a regular, constant stride, pattern, thus achieving a high utilisation of the memory bandwidth. Parallelisation of the tensor computation is done after the slicing. A possible approach is to use a two-level parallelisation architecture. On a multi-node level, the partially contracted full expression is sliced over n indices and distributed to 2^n message-passing interface ranks. Node-level parallelism over CPU cores is done using system threads. For every tensor multiplication and summation, the input and output tensors are sliced over t indices. The contraction is then performed by 2^t threads writing results to a shared result tensor [130].

6.2.3 Data Format Optimisation. To achieve a high accuracy in the computation of the simulated output state compared to the actual output state it is necessary to represent the data with a correct amount of bits. The default approach is to use 64-bit double (floating-point) representation [43]. In the case of RQCs, the work of Yong et al. [127] proposes an adaptive precision scaling, which adjusts the data precision to single or half-precision dynamically depending on the degree of the sensitivity of different parts of the computation.

6.2.4 Maximum Bond Dimensions Truncation Optimisation. As described in Section 2.4, choosing a maximum bond dimension lower than the one required to compute exact results, allows a lower complexity of the simulation. The optimised maximum bond dimension is the minimum size which does not introduce an approximation error higher than the one allowed by the selected quantum circuit. The optimal maximum bond dimension is complicated to calculate, as the maximum accepted error depends heavily on the quantum algorithm being simulated, and the relationship between the maximum bond dimension and the approximation error is a function of the entanglement of the simulated circuit and of the algorithm used to generate the tensor representation [32]. Algorithms such as DMRG [163, 193] are one of the possible candidates for this optimisation.

Table 2. Summary of the most Important Acceleration Works Performances with GPU

Work	Simulation type	Baseline	Improvement (Speedup)	Benchmark Platform
[12]	Multiple	53-qubit RQC, depth 10 [148], GPU	4.05× on average	NVIDIA H100 GPU, NVIDIA A100 GPU
[12]	Multiple	53-qubit RQC, depth 10 [144], GPU	4× on average	NVIDIA H100 GPU, NVIDIA A100 GPU
[12]	Multiple	53-qubit RQC, depth 10 [82], CPU	547.35× on average	NVIDIA H100 GPU, NVIDIA A100 GPU
[194]	Tensor based	42 qubits in 1965.52 s [43], CPU	10.0×	NVIDIA A100 GPU
[129]	Tensor based	30 qubits, depth 4 in 246 *s* [82], CPU	175.7×	GPU
[48]	Schrödinger	35-qubit QFT [50], GPU	5×	6× NVIDIA V100 GPU
[118]	Schrödinger	26 qubits in less than 10ms [96, 178]	$\geq$ 10×	GPU Cluster
[49]	Schrödinger	22-qubit QFT [158]	up to 10×	GPU

For each work, the speedup reported by the authors is presented in the Improvement column.

6.3 Other Acceleration Approaches

Alternatively to what was described previously, some works exploit other approaches for optimisations, such as QPUs [182, 194] and different memory technologies. For example, CutQC [182] employ classical CPUs interacting with a small quantum computer. This hybrid computing approach enables the evaluation of larger quantum circuits that cannot be executed on a classical computer alone. It offers better fidelity and allows the simulation of larger circuits than either approach could achieve independently. SnuQS [147] focuses on the full utilisation of the storage device connected to the system. That work aims at achieving maximum I/O bandwidth by employing memory management and optimisation techniques, resulting in better performance compared to DDR4 DRAM main-memory-only systems. Other approaches that make use of multiple hardware platforms can be found in the literature [41, 50, 52, 54, 55, 117, 188, 203]

7 Acceleration using GPU

Accelerating quantum computer simulations using GPUs by offloading workloads partially or fully from the CPU to GPU has been an effective approach for many years. Early works, such as the one by Gutierrez et al. [79], attempted this over 10 years ago. Similar to CPU simulations, GPU simulations can also be classified according to the classification defined in Section 4. The results from the most relevant works are presented in Table 2.

7.1 Schrödinger-style Simulation Acceleration

As seen in Section 6, the core operations of quantum circuit simulation are small matrix multiplications. If the data dependencies between these operations are limited or nonexistent, and they can be parallelised, GPUs can perform them with much higher throughput compared to CPUs. It is still important, even for GPU execution, to focus on data locality to minimise memory access misses [205]. In GPU simulation acceleration, each work focuses on one or both of two steps: first, partitioning the circuit into sub-circuits or tasks; second, accelerating the computation.

7.1.1 Circuit Partitioning. As seen for the CPU in Section 6, also in the GPU approach the first step followed is to partition the circuit in order to enable a more efficient parallel execution. HyQuas [205] proposes a circuit-aware partition strategy and a high-accuracy performance model that guides the partitioning. This allows to obtain a near-optimal partition of a given quantum circuit into different groups and select an optimal method to compute each one. CuStateVec, a library of the cuQuantum SDK [12], which focuses on state-vector simulation acceleration for GPU, uses gate fusion [173]. Numerous small gate matrices are fused into a single multi-qubit gate matrix, which can then be computed in one shot instead of performing multiple computations. This allows for improved performance in cases where both the high compute performance and high memory bandwidth of the GPU are used.

7.1.2 Memory Access Optimisation. Different approaches can be used to address the data locality issue. ShareMem [78] method considers a circuit partitioned in several gate groups, which are applied only to a subset of k qubits out of the n total qubits. The total 2^n state vector values can be split into fragments of size 2^k, which can be stored in GPU shared memory, and each fragment can be mapped to one GPU thread block. The thread block can load the fragment from the global memory to the shared memory, apply the gates on it, and store back the fragment in the global memory. This method performs better than the following BatchMV approach in the case of a sparse part of the circuit [205].

The BatchMV [180] method is based on the idea that if all the target and control qubits of a gate group come from the same k qubits, it is possible to merge these gates into a k-qubit gate. This allows to divide the simulation into 2^{n-k} matrix-vector multiplication tasks, each one with a $2^k \times 2^k$ gate matrix to a state vector of 2^k values. The index of the values only differs on these k positions, improving the data locality. This method performs better than the previous in the dense part of the circuit. HyQuas [205] automatically selects the best approach depending on the part of the circuit between OShareMem, an improved version of ShareMem [78] and TransMM, which performs better than BatchMV in their framework. TransMM transposes the quantum state, allowing to treat the gate-applying operation into a standard **GEneral Matrix Multiplication** (**GEMM**) operation, which can be accelerated by highly optimised libraries such as cuBLAS and Tensor Cores.

7.1.3 Parallel Execution. As seen in Section 6, the main way to approach distributed computing is with OpenMP or MPI. It is important to maximise GPU usage while minimising data exchange between the CPU and GPU, as frequent amplitude exchanges between them introduce significant data movement and synchronisation overhead [208]. Qubit reordering [44] is also a technique used by cuStateVec [12] to address the challenge of applying a gate onto a global indexed qubit. The approach involves moving the qubit from a global index to a local index, allowing a single GPU to compute the state vector. On a more broad approach, there are even works proposing a novel multi-GPU programming methodology, such as the work from Li et al. [118], which constructs a virtual BSP machine on top of modern multi-GPU platforms.

7.2 Tensor-based Simulation Acceleration

As reported in the work of Vincent et al. [189] a major issue in quantum computer simulations is the under-utilisation of GPUs and CPUs in supercomputers. They further predict an increase in inefficiencies due to the increase of parallelism and heterogeneity in exascale computers, with billions of threads running concurrently [83, 107]. Future supercomputers will see an increase in on-node concurrency rather than the number of nodes, with large multi-core CPUs and multiple GPUs per node [51].

7.2.1 Tensor Network Creation. For this step of the simulation on GPUs, some works [189] also use CoTenGra [72], as already mentioned in Section 6, to compute high-quality paths and slices for tensor networks. Additionally, there is the possibility of reusing common calculations, as described in Ref. [189], which avoids adding duplicate tasks during the slicing, therefore leading to a task graph with shared nodes.

7.2.2 Tensor Network Contraction. A possible approach, presented for Jet [189] is to use the transpose-transpose-matrix-multiply method. The basic building block of the task-dependency graph is the pairwise contraction of two tensors. This can be decomposed into two independent (partial) tensor transposes and a single matrix multiplication [128]. While for the CPU they use the qFlex [7, 187, 188] transpose method, for the GPU they use cuTENSOR [12], used also in the work of Shah et al. [164].

Another approach to tensor contraction is the bucket contraction algorithm by Dechter [45], as described in QTensor [129] and used also by Shah et al. [164], where an ordered list of tensor buckets (collection of tensors) is created to contract the tensor network. Each bucket corresponds to a tensor index, the bucket index. Buckets are then contracted one by one. The contraction of a bucket is performed by summing over the bucket index, and the resulting tensor is then appended to the appropriate bucket. The number of unique indices in aggregate indices of all bucket tensors is called a bucket width. Memory and computational resources of a bucket contraction scale exponentially with the associated bucket width. It is possible to improve this method by ordering the buckets first and then finding the indices that can be merged before performing the contraction. This allows for a smaller output size and larger arithmetic intensity as presented by Lykov et al. [129]. An issue with the bucket elimination algorithm is that tensors can grow too large to fit in memory, so a solution proposed by Shah et al. [164] is to introduce data compression. Their work proposes a GPU-based lossy compression framework that can compress floating-point data stored in quantum circuit tensors with optimised speed while keeping the simulation result within a reasonable error bound after decompression. The compressed data can be decompressed when the tensors are needed during the computation.

An additional approach is to use a partitioning method, which is optimal for each part of the circuit, depending on if it is sparse or dense, as mentioned already in the Schrödinger approach in the same work of Zhang et al. [205]. OShareMem method [205], an optimised version of the ShareMem method [78], deletes redundant computation, reduces data indexing overhead, and uses a new layout to access the shared memory faster. Another approach is the TransMM method [205], which converts a set of special matrix-vector multiplications in quantum circuit simulation into GEMM to take advantage of highly optimised GEMM libraries and hardware-level GEMM compute units like Tensor Cores. The work of Zhang et al. [205], as mentioned before, introduces an automatic selection method for the approach to be used, by using OShareMem for sparse parts of the circuit, and TransMM method for the dense parts of the circuit, allowing for further speedup.

7.2.3 Data Format Optimisation. As already mentioned for the CPU optimisations, using smaller precision for the data and calculations leads to improved performance. Although the works that try to accelerate the tensor-based acceleration on GPU do not try to propose any optimisation regarding the data format, they pick slightly different configurations. Most of the works use double (64-bit) floating-point precision [164, 194, 205], while other works, such as Jet [189], use different precision such as single (32-bit) floating-point precision.

7.3 Other Acceleration Approaches

Some simulation tools allow for the acceleration of quantum circuit simulation on GPU by focusing more on the optimal usage of the available hardware. An example of this is cuQuantum [12], which provides composable primitives for GPU-accelerated quantum circuit simulation, including distributed computing on multiple GPUs. TensorLy-Quantum [152] is a quantum library with direct support for tensor decomposition, regression, and algebra. It additionally provides built-in support for Multi-Basis Encoding for MaxCut problems [151] and was used to develop Markov chain Monte Carlo-based variational quantum algorithms [153].

8 Acceleration using FPGA

Although FPGAs are more limited in terms of resources and frequency when compared to CPUs and GPUs [35], they allow for more flexibility, leading to architectures better fitted to the problem [206]. While less scalable compared to the implementations with the previous hardware platforms, FPGAs

excel when working with very limited resources, such as simulations running on an off-the-shelf personal computer.

It is worth noting that some of the reported work, especially early efforts, focused on emulating quantum hardware rather than serving as an acceleration platform for quantum computer simulation, where only a few core operations are offloaded to the FPGA.

In the former case, the FPGA acts as a quantum computer itself, with which the host system must interface. Some example of this emulation approach include the early works of Khalid et al. [101] and Aminian et al. [6]. This same approach has been followed more recently in terms of work of Zhang et al. [207]. These approaches are interesting but can only be applied for problems requiring only a very limited number of qubits.

More recent works focus on running only the most compute-heavy operations on the FPGA. FPGA-accelerated simulation mainly focuses on the previously discussed Schrödinger approach. The two main steps of the acceleration are the pre-computation of the circuit matrix and the matrix computation.

8.1 Pre-computation Optimisation

In the pre-computation step, various optimisations have been proposed. The work of Jungjarassub and Piromsopa [99] introduces an algorithm that does not directly multiply all the gates, but first checks for special cases. Depending on the combination of gate types and the transformation they apply, they can avoid executing certain multiplications in certain specific cases.

A similar approach is used in the work of Hong et al. [87], which checks for the matrix values before multiplication, and in the case where ones or zeros are present, avoids processing through the actual multiplication module. This work focuses on the computation of a 2×2 gate regardless of the circuit. It first groups multiple gates into a single one when possible, then simulates the resulting gates one by one. Although this approach does not prioritise parallel execution, it allows for the execution of larger circuits on hardware with limited resources.

8.2 Computation Optimisation

Different approaches have been proposed to speed up the actual calculation. In the case of gates that generate phase rotation, it is possible to use a look-up table to collect sine and cosine values instead of calculating them directly [99]. Look-up tables are also evaluated in the work of Mahmud and El-Araby [132], which replaces any complex calculations with a simpler array-indexed operation. This is further optimised by storing only the value relative to the actual input vectors which are necessary for the simulation.

Another optimisation to save memory operations is to check whether the state vector changes after a gate is applied before saving it back to memory. If no changes are detected, the memory-write can be avoided as is done in the work of Hong et al. [87]. The work of Mahmud and El-Araby [132] evaluates different hardware architectures to identify the best-performing one for the **Complex Multiply and ACcumulate** (**CMAC**) operation, which is the core of simulation. They evaluate a single CMAC unit which processes all the operations (optimised for area but with low throughput), N-concurrent-CMAC units (optimised for throughput but requires a higher number of CMAC instances) and a dual-sequential-CMAC architecture (two CMAC instances connected sequentially, with computation and data write operations overlapped). Lastly, they also propose a kernel-based emulation model useful in case of a repeated set of core operations. The follow-up work by Mahmud et al. [133] proposes an additional approach that improves the scalability of the emulation. Instead of using a look-up table, which sacrifices area for speed, or using dynamic generation (generation of the algorithm matrix elements at compile-time), which sacrifices speed for area, they propose a stream-based CMAC. They stream the algorithm matrix elements at run-time, meaning the

Table 3. Hardware-aware Optimisation Techniques

Technique	Improves	Hardware support
Mixed-precision operations	compute and data storage	CPU [80], GPU [86]
Arbitrary-precision operations	compute and data storage	FPGA [42]
Lossy data compression	data storage	CPU (software), GPU (software), FPGA (compression engine) [28]
Thread-/Task-level parallelism	compute	CPU, GPU
Vector (SIMD) instructions	compute	CPU with vector support [116]
Matrix operations	compute	CPU with MMU [142], GPU tensor cores [89], FPGA Systolic Array [165], AI engines [98]

operation's cost is typically the I/O channel latency between the control processor and the FPGA, which is negligible compared to the time required for processing the algorithm matrix.

9 Summary and Future Directions

In this work, we examined different approaches to speeding up and reducing the memory usage for the simulation of quantum computers. The most important results, reported in Table 1 for the CPU-related works and in Table 2 for the GPU-related works, show how this is possible with multiple different approaches.

Focusing on the hardware-aware optimisations for the simulation problem and challenges, we present in Table 3 a summary of the different techniques, what they aim at improving, and which hardware support is best for that purpose. For each hardware support we also include a reference to a sample work showing a representative implementation of the technique in domains other than quantum computing.

The first group of optimisations aim at improving both the computation and data storage by changing the data and operations to use reduced precision. This has obvious benefits, but the challenge is to control the error introduced, since it is an optimisation that loses information from the original 64-bit double floating-point precision. For these optimisations, FPGAs can offer the benefit to implement hardware that can operate on data of arbitrary precision (not necessarily conforming to standard sizes). Using reduced-precision data and operations is an optimisation that is successfully being exploited in the **Machine Learning** (**ML**) domain currently by applying quantisation of the data values [67].

The second group of optimisations are those focusing on reducing the data storage and are based on data compression techniques. In this case, since the goal is to reduce the data size considerably, lossless techniques are not enough and thus a lossy technique needs to be explored. This technique again comes with the price of reduced accuracy since there is a reduction of information after compressing the data. Several techniques have been applied in the past for scientific applications [23] and in order for the techniques to be applicable with reduced latency, it is important to have a hardware compression module, implemented via a dedicated FPGA [28, 186] or GPU kernel [208].

The third group of optimisations focus on lowering the execution time by leveraging parallel processing and/or using hybrid configurations with dedicated hardware units for some demanding operations. Thread and task parallelism is an effective technique to reduce the execution time by exploiting the existing parallel hardware resources in CPUs and GPUs. **Single-Instruction-Multiple-Data** (**SIMD**) instructions are used to exploit parallelism at a finer-grained scale, at the instruction level. When using SIMD instructions we are using multiple computational units to perform multiple operations in the same cycle. SIMD support is now common in most commodity processors, but the other operations that are very relevant to these simulations are matrix operations, which usually require dedicated matrix units for acceleration. Since matrix operations are also very relevant for AI, there has been a recent increase in products providing hardware support for these operations [169]. Namely, some CPUs and GPUs now have dedicated matrix units and/or neural

acceleration units. Also, the Google TPU [98] used for both ML training and inference is basically a hardware accelerator for the matrix-matrix operations. The use of FPGAs in this case is also very relevant as they can be used to implement matrix-matrix operations for certain non-standard matrix dimensions. Also, as mentioned previously, FPGAs could be exploited to directly implement matrix-matrix operations for complex numbers [132].

Considering all of the above, we believe that in the future there is a need to invest in the development of more effective data compression techniques, a more flexible use of data precision, and hybrid approaches. Since the market share for the simulation of quantum computers is much smaller than for AI applications, we do not expect an explosion of accelerators as has been observed in the recent years for the ML domain. As such, it is unlikely that we will see many hardware accelerators dedicated to the simulation of quantum computers. But the developments in the ML domain can be leveraged to deliver benefits to this domain too, since the critical operations are basically the same: matrix-matrix operations. As such, we expect in the future to see the use of ML accelerators for improving the performance of quantum computer simulations. Lastly, it is very interesting to already see some development using FPGAs and we expect the trend will be to see more and more FPGA-based dedicated hardware to solve specific operations on specific data types in a very efficient way.

10 Conclusions

Quantum computer simulators play an extremely important role in helping the development of new algorithms and hardware for the promising quantum computing paradigm. While several approaches and simulators have been proposed, the characteristics of the problem make it extremely hard to scale to systems with larger number of resources, required for solving more complex problems. The main challenges of quantum computer simulations are the large amount of data that must be stored in memory, with sufficient precision to produce results with acceptable accuracy, and the execution time, which grows exponentially with the increased number of qubits. In this work, we presented a review of existing tools and approaches for systems with CPUs, GPUs, and FPGAs, with a focus on how hardware-aware optimisations can help address the challenges. CPU-based works mainly focused on reducing the memory requirements, thus increasing the number of simulated qubits, while the GPU-based ones focused mainly on the speed-up. Based on this study, we showed the future directions for hardware-aware optimisations, including the use of accelerators designed for other domains but addressing similar problems and the development of FPGA-based hardware accelerators for quantum computer simulation.

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