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A Compact 40 dBm GaN/SiC MMIC Doherty Power Amplifier at FR3 Band for 6G Applications

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***Abstract*— In this paper a Doherty power amplifier (DPA) on a 120 nm GaN on SiC monolithic microwave integrated circuit (MMIC) process is presented. The measurement results show a peak power added efficiency (PAE) of 27–43% and 6 dB backoff PAE of 19–37% with a peak delivered output power of 37–41 dBm across the operational band of 13–16 GHz. This performance is achieved in a compact active area of 2.6 × 1.7 mm^2, which makes it an efficient and scalable solution for the high power and bandwidth requirements of 6G networks.**

***Keywords*— Doherty, gallium nitride, load modulation, power amplifiers.**

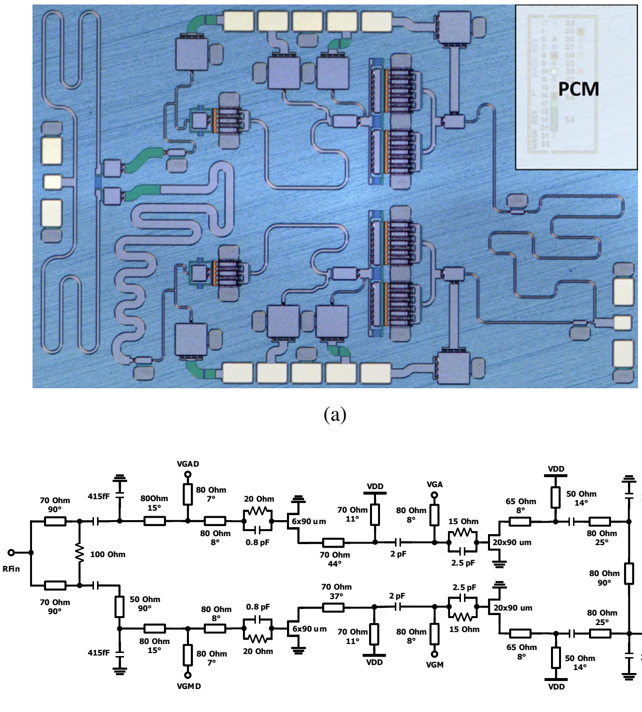
I. INTRODUCTION

The frequency range 3 (FR3) being a compromise between the bandwidth and propagation requirements of sixth-generation (6G) wireless networks, has recently been investigated for power amplifier (PA) design [1], [2], [3]. Advanced wireless communication systems employ spectrally efficient signals that lead to high peak-to-average power ratio (PAPR), which, together with the strict need for energy efficiency, demands power amplifiers with high efficiency under significant power back-off conditions.

Gallium Nitride (GaN) DPAs are able to deliver high output power at the band of interest while achieving high efficiency at large back-off ranges through load modulation, which makes them particularly well suited for 6G base stations. The compactness and simplicity of DPAs make them compatible with MIMO architectures that enable the integration of multiple RF chains while maintaining performance, addressing the high data rate demands expected in future 6G networks [4].

This paper introduces a 40 dBm Doherty power amplifier (DPA), designed specifically for efficient operation at the 15 GHz band on WIN Semiconductor's NP12-01 GaN/SiC process. This 0.12 µm gate process is manufactured on 100 mm SiC substrates and uses a source-coupled field plate design to provide high breakdown voltage required for reliable operation at a drain voltage of 28 V. Using the high efficiency and thermal stability of GaN on SiC, this DPA addresses the bandwidth and power challenges faced by 6G base stations. Traditional Doherty amplifiers suffer from inherent bandwidth limitations due to the quarter-wavelength transmission line impedance transformer. But a higher bandwidth of the Doherty combiner is achieved by merging it into an output matching T-network of transmission lines [5].

The following sections discuss the theory, design, and experimental validation of the presented DPA, highlighting its advantages in bandwidth extension and efficiency enhancement, which position it as a promising solution for high-frequency 6G applications.



(a)

(b)

Fig. 1. Die photograph (a) and the schematic (b) of the two stage Doherty power amplifier with area of 2.6 × 1.7mm^2. The transmission lines in the schematic are shown with the characteristic impedance and the electrical length at 15 GHz.

II. DESIGN

The presented DPA (Fig.1) is a two-way symmetrical design with 6 × 90 μm devices for the driver stages in each path, after splitting the input power using a symmetrical Wilkinson divider. For the power stage, two devices of 10 × 90 μm are combined for each path with a shared via in between for thermal and space considerations. The optimum load for each path is 50 Ω which can deliver an output power of more than 10 W after effective combination of output powers from main and auxiliary branches.

In a traditional Doherty combiner design, an impedance of $R_{\mathrm{opt}}/2$ is used as the load of DPA, R_{opt} being the optimum load for each device. Then using a quarter-wavelength transmission line with a characteristic impedance of $Z_{\mathrm{c}} = R_{\mathrm{opt}}$, it is transformed into $2 \times R_{\mathrm{opt}}$ at backoff while the auxiliary output is considered as open. At the peak power, with the auxiliary current modulating the $R_{\mathrm{opt}}/2$ load into R_{opt}, both devices will see R_{opt} [6].

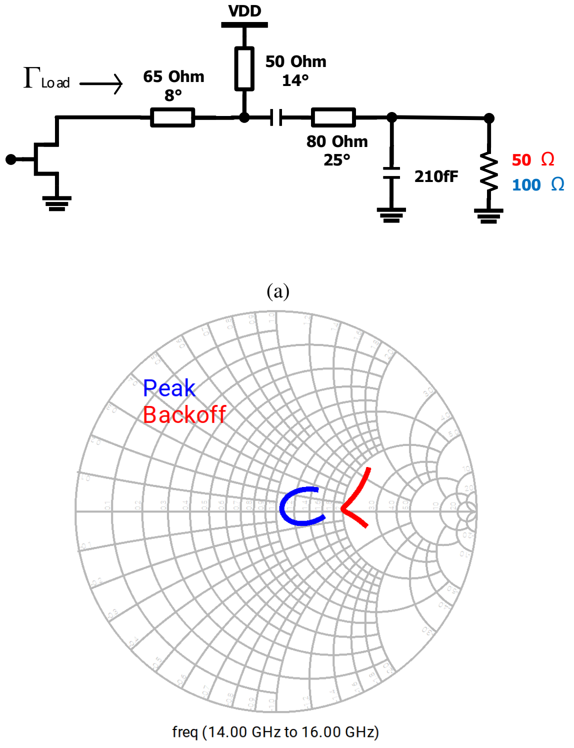
Modified Doherty amplifier presented in [7] in a comparable approach, uses $2 \times R_{\mathrm{opt}}$ as the load, and $Z_{\mathrm{c}} = 2 \times R_{\mathrm{opt}}$ for the impedance transformer. The $R_{\mathrm{L}} = 2 \times R_{\mathrm{opt}}$ is then applied to the main amplifier with no bandwidth limitation from the impedance transformer at the backoff level. The impedance transformation happens at the peak power level, however, not extremely dropping the bandwidth at the peak. Implementing a transmission line with a high characteristic impedance of $2 \times R_{\mathrm{opt}}$ is challenging in some processes. In [5] it is shown that a T-network can replace conventional high-characteristic impedance quarter-wavelength transmission lines to overcome DC current density restrictions and the process limitations due to the required narrow lines.

In this design, extending the continuity of the choice of load resistance between $R_{\mathrm{opt}}/2$ in traditional and $R_{\mathrm{opt}} \times 2$ in the modified Doherty, we choose a load resistance of R_{opt} (equal to 50 Ω for the devices mentioned) which eliminates the need for a post-matching network. Then using an impedance transformer with characteristic impedance of $\sqrt{2} \times R_{\mathrm{opt}}$, the load is transformed to $2 \times R_{\mathrm{opt}}$ at the backoff, and the modulated load of $2 \times R_{\mathrm{opt}}$ at peak is transformed into R_{opt} as desired. And to overcome the inherent bandwidth limitation of the conventional Doherty combiner, the impedance transformation is merged into the matching network (Fig. 2a). The impedance seen from the device (after canceling out the output parasitic capacitance) is shown in the Smith chart in Fig. 2b, which shows the proper impedance transformation from 50 Ω to 100 Ω at the backoff, and from 100 Ω to 50 Ω at peak power level.

To maintain a good bandwidth at peak, the same network is used for the auxiliary load matching, making the design completely symmetrical. However, it results in transforming the desired open-circuit at the backoff from the auxiliary branch into an unwanted short circuit, which is alleviated by a quarter-wavelength transmission line on the auxiliary path. This makes it necessary to use a 90° delay line at the main path's input to compensate the phase difference.

III. RESULTS

Fig. 3 shows the small-signal results from measurement and simulation of the DPA with an operating point centered at 14.5 GHz. The reflection coefficient reaches a high maximum value of -6 dB at the input, because of the deep class-C biasing of the auxiliary driver amplifier. However, this reflection is improved under large-signal drive.



(a)

(b)

Fig. 2. Main amplifier output matching network: (a) Schematic and (b) The impedance seen from the matched network with the two loads of 50Ω, and 100Ω (meandered lines and the combining structures used in the final layout).

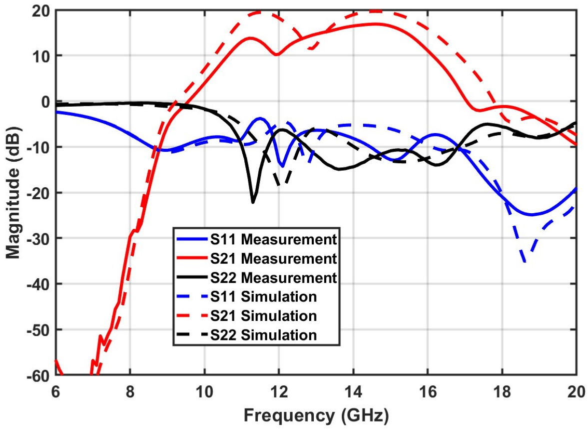


Fig. 3. Measured and simulated S-parameters of the presented DPA.

Delivering such a high output power in a very small area can raise heating issues. For the large signal measurements, the chip was mounted on a heatsink, and to evaluate the circuit's performance in a condition similar to practical application, pulsed-RF measurements with a pulse period of 200 μs and a range of duty cycles of 5–20% were performed. The drain of the driver stages were biased at 15 V to maintain good efficiency, and the drain of power stages at 28 V to reach their highest output power. Fig. 4 and Fig. 5 show the measured PAE of 27–43% at peak output power and 19–37% and 15–31% at the 6 dB and 8 dB backoff levels respectively across the 13–16 GHz frequency band. The saturation output power of

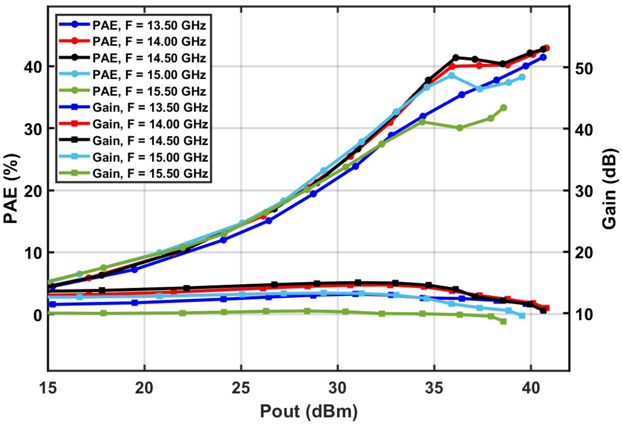


Fig. 4. Measured PAE and Gain at different frequencies vs. output power.

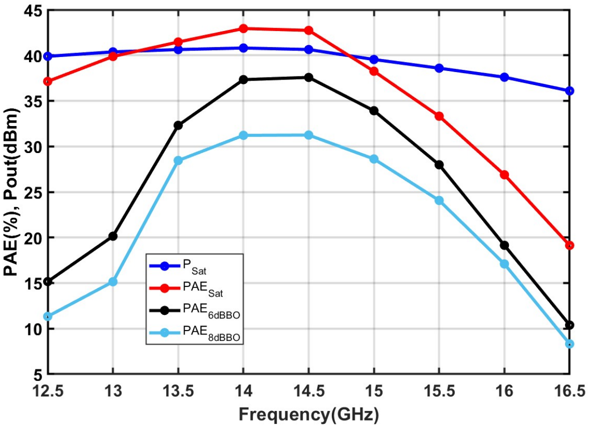


Fig. 5. Measured PAE and saturation power vs. frequency.

37–41 dBm and a power gain of 16 dB was also achieved.

Table 1 compares the results of this work with state of the art backoff-efficient power amplifiers on GaN. Compared to other designs, this work is the most compact MMIC in the table, while delivering the 41 dBm output power with comparable efficiency.

IV. CONCLUSION

The presented GaN/SiC-based Doherty Power Amplifier (DPA) delivers maximum power of 41 dBm across 13–16 GHz band in a very compact area of 4.42 mm^2, enabling the possibility of integration into a massive MIMO system for future 6G base stations. The design achieves peak, 6 dB backoff, and 8 dB backoff efficiencies of 27–43%, 19–37%, and 15-31% respectively, over a 3 GHz bandwidth. A modified T-network Doherty combiner merged into output matching network was used to improve the inherent bandwidth limit of traditional DPAs. The comparison with the state of the art show that this DPA effectively meets both power and efficiency requirements, positioning it as a competitive solution for next-generation wireless infrastructure.

Table 1. Comparison with the other backoff-efficient GaN power amplifiers.

Ref.	**Freq. (GHz)**	P_{sat} **(dBm)**	**PAE$_{\text{peak}}$ (%)**	**PAE$_{\text{6dB}}$ (%)**	**PAE$_{\text{8dB}}$ (%)**	**Gain (dB)**	**Area (mm^2)**
[8]	17.3–20.3	38	34–36	22–27†	19–24†	25	–
[9]	13.7–15.3	36	19–25†,‡	13–21†,‡	–	4–7	4.96
[2]	10–14	34	28–38	21–31	–	15	10.64
[10]	14.5–17.25	34	20–25	20–26	18†	15	10.44
[11]	10.7–12.75	43.3	35–45	25–33	–	25	19.6
[3]$^{\#}$	14–16	40	30–37	22–27	22–27	10	7.92
[12]	14.5–15.5	35.9	20–26†,‡	13–18†,‡	–	5.1–6.5	11.2
T.W.*	13–16	41	27–43	19–37	15–31	16	4.42

$^{\#}$Simulation data, *this work, †read from graph, ‡calculated from DE.

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