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An 8-Way E-Band GaAs Power Amplifier Utilizing Shared-Ground Vias

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***Abstract*—In this paper, an 8-way 3-stage E-band gallium arsenide (GaAs) power amplifier utilizing shared-ground vias is presented. To save area, the ground vias of neighboring transistors are shared, while keeping the gate and drain connections separate. This requires careful de-embedding of the via influence in the transistor model as is outlined in this paper. In measurements, the PA has more than 10 dB small signal gain covering from 60 to 81.4 GHz and at 78 GHz produces 28 dBm of output power with a maximum PAE of 27.1%.**

***Index Terms*—power amplifier, E-band, MMIC, gallium arsenide, shared-ground transistor, compact size**

I. Introduction

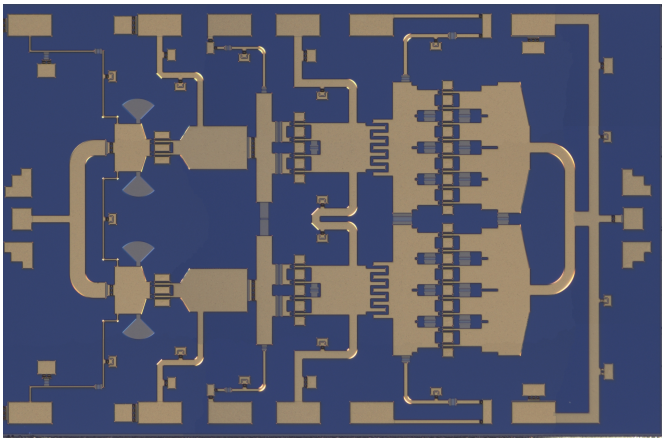
The application of E-band frequencies (71-76 GHz, 81-86 GHz) for point-to-point communication by the Federal Communications Commission (FCC) is a significant part of wireless communication technologies. These frequencies can provide wider bandwidth, which enables high-speed, long-range wireless communications[1].

While current CMOS technology offers drastic price reductions, and large-scale integration compared to III-V technologies, it cannot develop high output power and competing noise figures at mm-wave frequencies like GaAs pHEMT/mHEMT[2] or GaN.

In this paper, an 8-way compact E-band GaAs PA using shared-ground vias is presented. Since the commercial foundry model does include ground vias, we demonstrate a simulation approach that can build an appropriate custom model by de-embedding the vias of the foundry model. We show how to design a matching network utilizing multiple ports of this custom transistor, maintaining amplitude and phase balance between the ports using slots in the wide output matching network to reduce loss.

II. Design and Analysis

Fig. 1 shows the schematic and layout structure of the circuit. The PA consists of 3 stages, where the first driver-stage transistors are biased with 2 V drain voltage for high transconductance to achieve high gain while the last two-stages transistors are biased with 4 V drain voltage for high output power. To achieve higher gain, all the transistors are biased with gate voltage at the highest transconductance point. Sixteen 2 $\times$ 50 μm transistors are combined at the last stage while eight 2 $\times$ 50 μm and two 4 $\times$ 75 μm transistors are used in the second and first stages, respectively. The



(a)

(b)

Fig. 1. Implemented E-band PA MMIC: (a) schematic; (b) chip photo

circuit is fabricated on 150mm GaAs wafers using the WIN Semiconductors PP10-20 pHEMT platform. The core of this technology is a 160 GHz ft, 0.1 μm-gate D-mode transistor and is qualified for 4 V operation.

A. Shared ground via modeling

Ground vias in Monolithic Microwave Integrated Circuits (MMICs) design cannot be placed too close to each other due to design rules, which lead to a large chip area. Therefore, to minimize the chip area, overlapping vias or allowing transistors to share ground vias can be an effective solution.

However, the Process Design Kit (PDK) does not provide for a transistor without source vias so a custom configuration

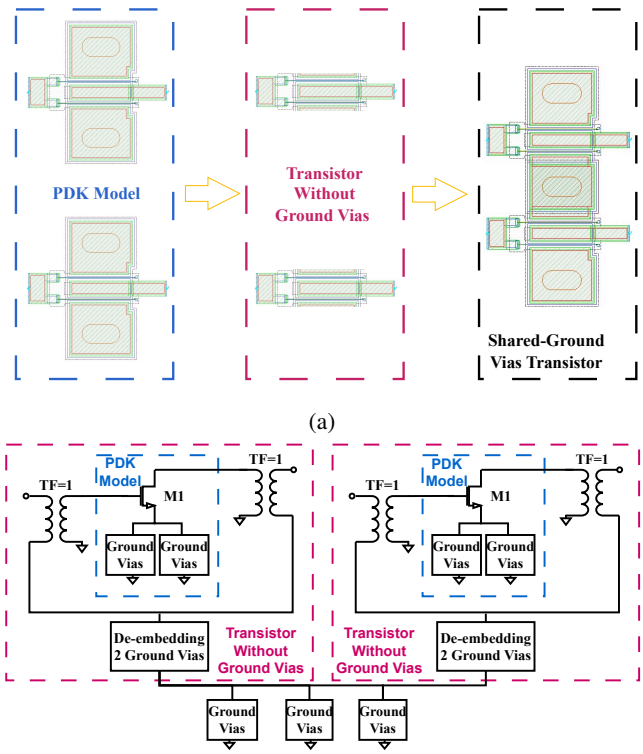


Fig. 2. Shared-ground via transistor model. (a) The layout of the shared-ground transistor. (b) transformer-based de-embedding

cannot simply be constructed from via-free two-finger transistors and source via pads. Instead, we here use an approach solely based on simulations in Advanced Design System (ADS) to obtain a workable model, as is exemplified in Fig. 2b: 1). To create a model for a 4-finger transistor with two gate and two drain ports we start with two standard 2-finger transistors. To create a third port to allow for de-embedding of the source via, we use ideal 1:1 transformers components in ADS, which due to their ideal Y-parameter implementation also allow for dc-bias to pass. 2) We then de-embed the effect of the source vias with the ADS de-embedding component. The effect of the vias is simulated based on ADS Momentum. 3) Then we connect those source-via-free transistors to three joint vias.

In this approach we construct eight 2 $\times$ 50 μm transistors with internal source vias to be used in the final stage of this PA while still having four individual gate and drain bias ports to verify amplitude and phase balance within the transistor, as discussed next.

With the new model of transistors supporting individual gate and drain ports in simulation, it becomes easier to observe the current distribution compared to using a large transistor from the foundry model. This is particularly beneficial at very high frequency where the gate width can no longer be neglected in terms of wavelength. In this design, a very wide transmission

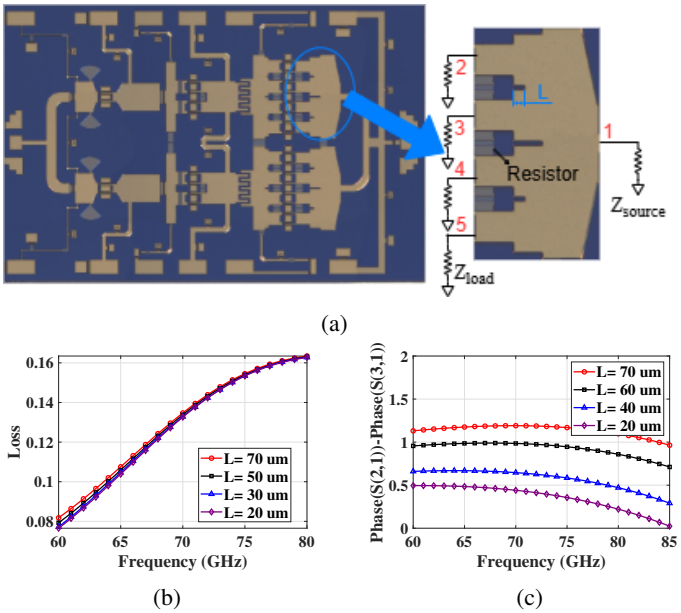


Fig. 3. The influence of balancing slots on the transmission coefficients of the output power combiner. (a) combiner unit. (b) Loss of combiner. (c) phase imbalance.

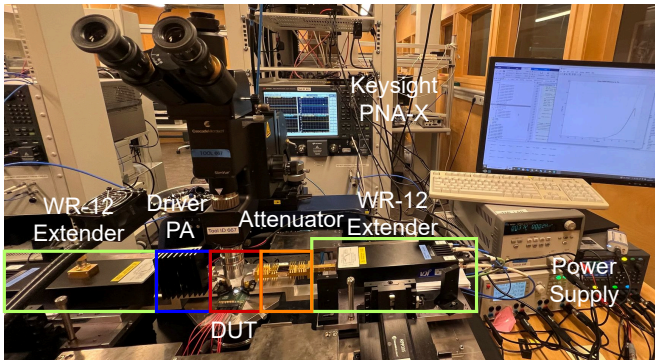


Fig. 4. Measurement setup

line (W = 600 um) is used in both the inter-stage matching network and output matching network (OMN), where the width is larger than a quarter wavelength, resulting in different current between the edge and middle transistors. Therefore, observing the current distribution when doing the simulation helps check the stability and bias status of the transistors in the design process.

B. Output matching network balancing

The OMN is primarily designed for load impedance matching based on load pull analysis. Since sixteen 2 $\times$ 50 μm transistors are used in the final stage, the load impedance becomes very small. In this case, a low-impedance transmission line is implemented for impedance matching, which results in a very wide transmission line. Due to the asymmetrical structure of the edge-neighboring port, the trace paths from the combining port (Port 1) to Ports 2–3, as

TABLE I
COMPARISON OF GaAs PAS

Reference	Topology	Frequency (GHz)	Gain (dB)	Psat (dBm)	PAE$_{max}$ (%)	Chip size (mm^2)
[3]	GaAs 6-way power combining	71-76	18.1 (3-stage)*	28	15	2.5×1.7
[4]	InGaAs 4-way balanced power combining	60-90	35 (3-stage)	14.5	7.4	4.5×2
[5]	GaAs stacked structure	55-64	22 (3-stage)	25	15	2×1.6
[6]	GaAs 8-way power combining	92-102	27 (5-stage)	27	12.5	3×3
[7]	GaAs 4-way power combining	71-76	18 (4-stage)	27	22	2×3
This work	**GaAs 8-way power combining**	**60-81.4**	**13.2 (3-stage)**	**28**	**27.1**	3×1.9

* estimate from the paper

shown in Fig.3a, are unequal. This asymmetry introduces phase and amplitude imbalance across the transistors, leading to increased loss and potential instability. To solve the instability issues, odd-mode stability resistors are added between neighboring ports. To improve the phase imbalance, slots are designed between the ports to equalize the electrical length. Since the whole branch structure is symmetrical, the slots between Port 2-3 and port 4-5 are tuned. The loss of the network is calculated by

$$Loss = 1 - \sum_{i=2}^{5} |S_{i1}|^2 \quad (1)$$

, where port1-5 are terminated with effective load impedance to minimize the reflection coefficient in the simulation. As shown in Fig. 3b, using slots of different lengths helps reduce network loss. As illustrated in Fig. 3c, this approach also improves phase imbalance across the frequency range. In this design, a slot length of $L = 20\mu m$ is used.

III. MEASUREMENT RESULTS

Fig. 5 presents the small signal simulation and measurement results. In the small-signal measurement setup, the S-parameters are calibrated using a probe calibration substrate, and a 20-dB attenuator is connected in series at the output to protect the measurement instrument. The measured small signal gain can reach 13.2 dB with both input and output reflection coefficients below -7 dB. The small signal bandwidth can cover from 60 - 81.4 GHz, maintaining a gain above 10 dB. A ripple is observed in measured S_{22}, which is attributed to the 20 dB attenuator which influence the calibration accuracy. The deviation in S_{11} between simulation and measurement may be due to the inaccuracy of the first-stage 4×75 transistor model.

The large signal measurement setup in WR-12 is shown in Fig. 4. The continuous wave (CW) signal is generated by a Keysight N5242b PNA-X which drives an external E-band source extender that multiplies the input signal frequency by a factor of six. To provide adequate input power for a saturated operation of the PA, a commercial E-band PA, SBP-6038533026-1212-E1, with a 22dBm 1dB compression point, is used in the setup. The input power of the device under test (DUT) is calibrated by a power sensor at the output of the driver while de-embedding the loss of the probe. A 20 dB attenuator is used at the output of the DUT to protect the

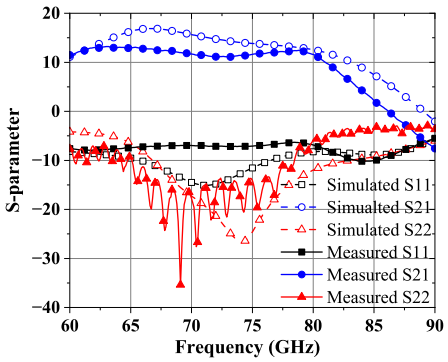
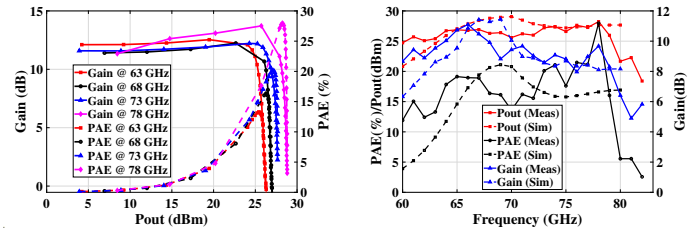


Fig. 5. Simulation and measurement of S-parameter



(a) (b)

Fig. 6. Large signal measurement. (a) Gain and PAE vs. output power at different frequencies. (b) Output power, gain and PAE at peak PAE point.

extender. The PA is mounted on a printed circuit board (PCB) and connected to the DC supply via wire bonding and cable.

The PA delivers 28 dBm output power with a peak PAE of 27.1% @78 GHz as shown in Fig. 6. Table 1 shows the comparison of GaAs PAs. Although the gain of this PA is lower than other designs, it still provides good performance on output power and PAE.

IV. CONCLUSION

In this paper, an 8-way 3-stage compact E-band gallium arsenide (GaAs) power amplifier utilizing shared-ground vias is presented. A compact output matching network is used to combine 8 shared-ground-vias transistors. A method to obtain a custom transistor model with multiple gate and drain ports from PDK data is presented and balancing slots are

used to improve the loss and phase imbalance in the output matching networks. The small signal gain is above 10 dB with a bandwidth of 60-81 GHz and the size of the core circuit is 3.0×1.9 mm^2. Based on the large signal measurement results, this PA can deliver 28 dBm output power with a peak PAE of 27.1% @78 GHz.

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