CHALMERS
UNIVERSITY OF TECHNOLOGY

A 16 W, 8 dB Output Back-Off Doherty Power Amplifier in GaN on Si MMIC Technology for FR3

Downloaded from: https://research.chalmers.se, 2026-10-07 22:39 UTC

Citation for the original published paper (version of record):
Noori, A., Zaheri, H., Schuberth, C. et al (2026). A 16 W, 8 dB Output Back-Off Doherty Power Amplifier in GaN on Si MMIC Technology for FR3. 2026 IEEE Topical Conference on RF Microwave Power Amplifiers for Radio and Wireless Applications Pawr 2026: 9-12. http://dx.doi.org/10.1109/PAWR69496.2026.11408585

N.B. When citing this work, cite the original published paper.

© 2026 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, or reuse of any copyrighted component of this work in other works.

(article starts on next page)

A 16 W, 8 dB Output Back-Off Doherty Power Amplifier in GaN on Si MMIC Technology for FR3

Abdolhamid Noori[$#1], Hossein Zaheri[#2], Christian Schuberth[*3], Helmut Brech[*4], Christoph Wagner[$5], Christian Fager[#6], Gregor Lasser[#7]

[$]Millimeter Wave Technologies (mmW), Intelligent Wireless Systems, Silicon Austria Labs GmbH, Austria

[#]Department of Microtechnology and Nanoscience, Microwave Electronics Laboratory, Chalmers University, Sweden

[*]Infineon Technologies AG, Germany

{[1]abdolhamid.noori, [5]christoph.wagner}@silicon-austria.com, {[2]zaheri,[6]christian.fager, [7]gregor.lasser}@chalmers.se, {[3]Christian.Schuberth, [4]Helmut.Brech}@infineon.com

***Abstract*—This paper presents a fully monolithically integrated compact asymmetrical Doherty power amplifier (DPA). The output combiner absorbs the intrinsic output capacitance C_{out}, of the devices with parallel inductors to resonate with C_{out}. Furthermore, output back-off (OBO) performance is improved by more than 8 dB thanks to asymmetric architecture, making the DPA suitable for handling high peak-to-average power ratio (PAPR) signals in 6G applications. The DPA implemented in novel Infineon 250 nm RF GaN on Si HEMT technology and was characterized under pulsed-RF measurement conditions, and demonstrates a maximum small signal gain of 9 dB at 7.2 GHz, an output power of 40 – 41.8 dBm at saturation, a saturation power added efficiency (PAE) of 20.9 - 32.7 % and a 8 dB back-off PAE of 15.5 - 26 % across a BW from 7 to 8 GHz, which is equal to 13.3 % fractional bandwidth (FBW), with a compact size of 4 mm $\times$ 4 mm, power density 1 W/mm^2.**

***Index Terms*—Doherty power amplifier, fully integrated MMIC, GaN on Si HEMT, output back-off, peak-to-average power ratio, 6G**

I. Introduction

In 6G mobile communications, the upper mid-band spectrum known as FR3 is located between the current FR1 and FR2 ranges. It gains advantages from both bands, offering much wider bandwidths than FR1 and experiencing lower propagation losses than FR2. This balance between coverage and capacity establishes FR3 as a key enabler for 6G networks. Modern wireless communication systems rely on advanced modulation schemes that produce signals with high PAPR, aiming to boost data rates. Efficient handling of high PAPR signals has led to the adoption of various PA architectures, such as envelope tracking [1], dynamic load modulation [2], outphasing [3], and the DPA [4]. Among them, the DPA stands out due to its use of load modulation concept and its balance between performance and design complexity [5] and [6]. The combination of high gain, power density, and transition frequency from S- to Ka-Bands has made GaN on SiC the dominant RF PA technology since the late 2010s. Infineon's first-generation, 28 V, 250 nm RF GaN on Si, introduced in 2021, enables MMIC integration on 8 inch silicon wafers using existing CMOS fabrication facilities. It uses cheaper, more accessible silicon substrates and supports scalable, shared-volume production for cost-effective massive MIMO deployments above 6 GHz.

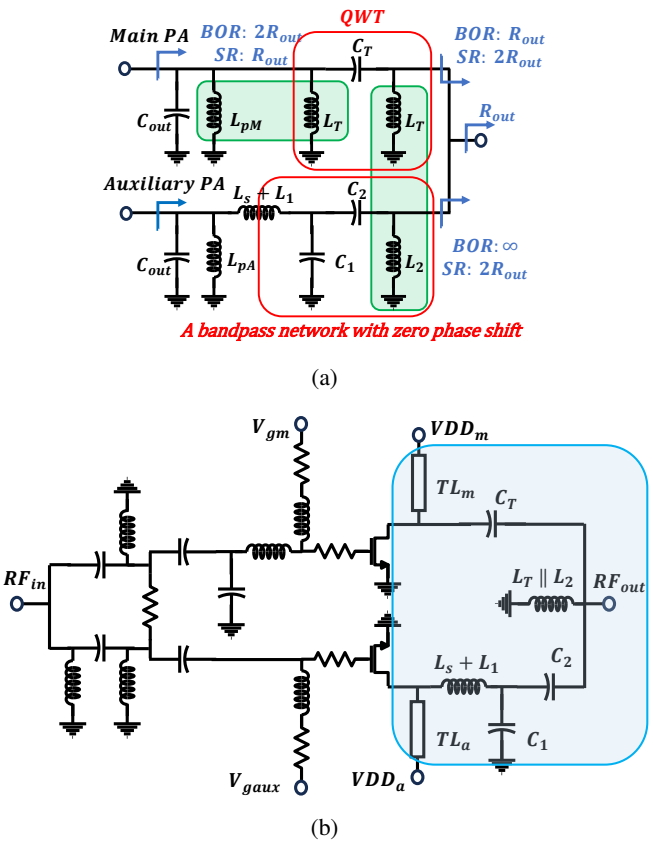

Fig. 1: (a) Initial lumped-element design of the output combiner. (b) Top schematic of asymmetrical DPA with output combiner circuit evolution from initial lumped element design to final implementation.

This work presents the design and measurement of high power MMIC DPA targeting the emerging FR3 band, implemented in GaN on Si technology. The paper is organized as follows. Section II presents the RF GaN on Si process and outlines the technology development. Section III details the DPA design approach, which includes a Low-Q output network with C_{out} compensation, as well as an input network implementing a power splitter. Section IV describes

the measurement setup and summarized measurement results, including the characterization of both small and large signals, with comparison to other MMIC DPAs fabricated in GaN on Si and GaN on SiC technologies operating in both FR1 and FR3 bands. Finally, concluding remarks are provided in the conclusion section.

II. RF GaN on Silicon Technology

This work uses an improved version of the novel RF GaN on silicon technology developed by Infineon [7]. The technology has been developed on high resistivity 8-inch substrates and processed in an advanced silicon fabrication facilities compatible with all other technologies. Special care has been taken to maintain a high substrate resistivity in the kΩ·cm range, even after epitaxial growth and wafer processing, to ensure low substrate RF losses for both active and passive devices. Optical lithography has been used to define the gate length of $L_{\mathrm{g}} = 250\,\mathrm{nm}$. To maximize the gain of the transistor, a scaled source-connected field plate has been employed, resulting in low feedback and output capacitances of $C_{\mathrm{gd}} = 20\,\mathrm{fF/mm}$ and $270\,\mathrm{fF/mm}$, respectively, at $V_{\mathrm{ds}} = 28\,\mathrm{V}$. To minimize thermal resistance, the silicon substrate has been thinned to $60\,\mu\mathrm{m}$ with high density of through silicon vias providing a low loss electrical connection to the common source on the backside of the chip. Designing high performance circuits with this technology requires a validated EM stack-up that accurately represents dielectric constants and losses, substrate losses, and models individual layer losses precisely. The Design Kit, verified through measurements, ensures that simulated results closely reflect the actual behavior of the passive network. This enables designers to confidently develop high-performance circuits and fully exploit the capabilities of the technology [8].

III. Compact Doherty Power Amplifier Design

The DPA schematic with circuit evolution from initial lumped design to final implementation is presented in Fig. 1. In DPA design, the main transistor size was selected so that its optimal load, R_{opt}, is close to 50 Ω, simplifying the matching network by eliminating the post matching network and minimizing passive network losses to enhance overall performance and reduce the DPA size. Using I–V characteristic plots for different device sizes and corresponding load-line analysis, the optimal load of 50 Ω was identified for a device size of 8×240 μm. To ensure an OBO greater than 6 dB, the auxiliary device was sized at 12×240 μm, allowing it to handle approximately 1.4 times the maximum current of the main device.

The transistor can be represented by a current source in parallel with a nonlinear parasitic output capacitance, C_{out} which can degrade performance. While conventional low-Q designs typically assume this C_{out} to be constant, in GaN-HEMT devices, it varies with output power [9] and [10]. The C_{out} value of the the auxiliary transistor differs between the back-off region (BOR) and the saturation region (SR), making it difficult to simultaneously satisfy the open-circuit condition in BOR and ensure optimal power matching in SR. As illustrated in Fig. 1a, C_{out} is compensated by a shunt inductor, L_p, while an additional small series inductor L_s is placed after the auxiliary PA, helps mitigate the impact of power dependency of nonlinear average C_{out} and prevents output power degradation in SR. The impedance of L_s should be much smaller than R_{opt} as defined in Equ. 1, [11], which ω is angular frequency.

$$\omega L_s < R_{opt}/5. \tag{1}$$

As depicted in detailed representation of load modulation networks in Fig. 1a, the equivalent inductor of L_{pM} parallel with L_T from lumped quarter-wavelength transformer (QWT) network in the main path and L_{pA} in auxiliary path are realized by on-chip transmission lines. This approach is chosen due to the limited DC current handling capability of the on-chip inductors and lower Q-factor of on-chip inductors compared to on-chip transmission lines. The QWT in the main path of the DPA is implemented by a high-pass lumped π-type network with a characteristic impedance of $\sqrt{2}\,R_{\mathrm{out}}$. The auxiliary path operates as an impedance transformer in saturation and maintains the open circuit of the output impedance in the back-off region at the same time. A bandpass network with zero phase shift composed of L_1, C_1, L_2, and C_2 is used to implement the auxiliary path network. In Fig. 1a, L_s is in series with L_1 and L_T in the QWT network of the main path and L_2 in the bandpass network of the auxiliary path are in parallel. The equivalent inductors of these components are used in the final implementation of the DPA, as shown in Fig. 1b. The main PA plays the dominant role in the small signal stability of the DPA because the auxiliary PA does not provide gain in the BOR. Asymmetric stabilizing networks are implemented by adding resistors of 5 Ω and 3 Ω to the gates of the main and auxiliary PA, respectively. A reversed uneven power splitter is adopted to deliver more power to the main PA. Consequently, the overall gain of the DPA improved. However, it still suffers in the SR due to class-C operation of the auxiliary PA, and in the BOR due to insufficient input power delivered to the main PA.

IV. Characterization Results

The fabricated MMIC DPA was attached to an aluminum heatsink using a conductive epoxy for thermal and electrical conduction. The DC pads were wirebonded to a PCB with a cutout designed to accommodate the heatsink's mounting step, ensuring proper mechanical alignment, Fig. 2. DC bias has been provided with external bypass capacitors to enhance low-frequency stability and isolation. The bias point has been set for a drain voltage 28 V, with a drain quiescent current $I_{DD} = 48$ mA, and auxiliary stage biased at $V_{gaux} = -5$ V. Direct probing of the RF pads minimizes load mismatch and signal loss by eliminating the need for wirebonding to the PCB. No oscillation issues have been experienced, both at small- and large-input drive.

The scattering parameter was measured under continuous wave (CW). The comparison of measured and simulated S-

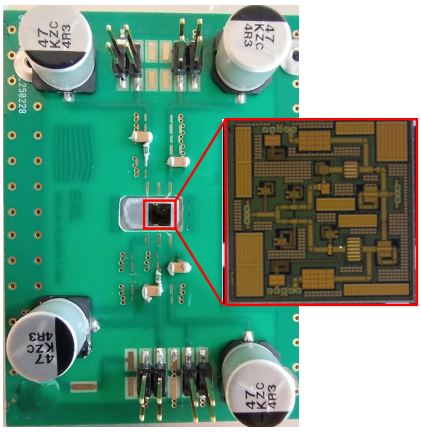

Fig. 2: Fabricated MMIC DPA mounted on test Jig, including MMIC chip photograph, Chip size is 4 mm × 4 mm.

parameter between 4 to 11 GHz are reported in Fig. 3. The accurate definition of the EM stack-up provides very good agreement between simulated and measured S-parameters, except for minor differences observed in the input and output return loss, S_{11} and S_{22}. S_{11} remains below -10 dB from 6.3 to 8 GHz and DPA achievs a peak linear gain of 9 dB at 7.2 GHz.

The thermal conductivity of GaN on Si in comparison to GaN on SiC technology introduces higher thermal resistance between the transistors and the chip bottom side in large signal CW measurement for 16 W MMIC DPA even if the chip is mounted directly on the heatsink. To mitigate overheating and avoid device failure, a pulsed-RF measurement method is crucial. A dual RF-pulse width technique was employed to accurately measure the DC current. Two different pulse widths were applied to device under test, and the corresponding drain current for each pulse was measured. Using these measurements, the corrected DC current at each input power level was calculated according to the following equation:

$$I_{\mathrm{DC}}(P_{in}) = (I_2(P_{in}) - I_1(P_{in})) \cdot \frac{T_{\mathrm{pulse}}}{W_2(P_{in}) - W_1(P_{in})} + I_q(P_{in}) \tag{2}$$

Where T_{pulse} is the pulse period and set to 200 μs, the measured currents with pulse widths W_2 and W_1 are I_2 and I_1, respectively, and I_q is the quiescent current. Precise current measurement at lower input power levels requires a wider pulse width, as the DC current in this region is very close to the quiescent point. Therefore, the pulse widths of W_2 and W_1 were set to 150 μs and 100 μs, respectively. To prevent excessive heating at higher power levels, the pulse widths of W_2 and W_1 were decreased to 10 μs and 5 μs, respectively at maximum input power. For all intermediate power levels, the pulse widths were linearly scaled between the two limits to balance measurement accuracy and thermal load.

Single tone power sweep RF-pulsed measurement have been carried out in the 7 to 8 GHz frequency band. The results are depicted in Fig. 4. The shape of the efficiency

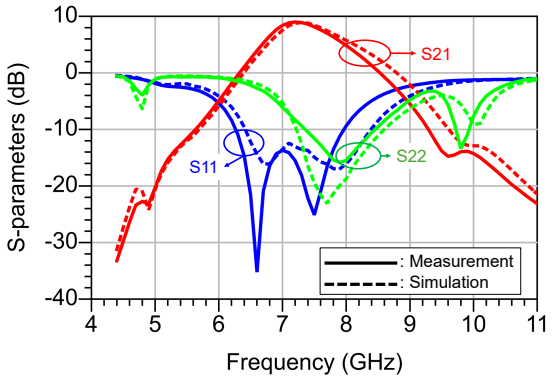

Fig. 3: Comparison between simulated (dash lines) and on wafer CW S-parameter measurement (solid lines).

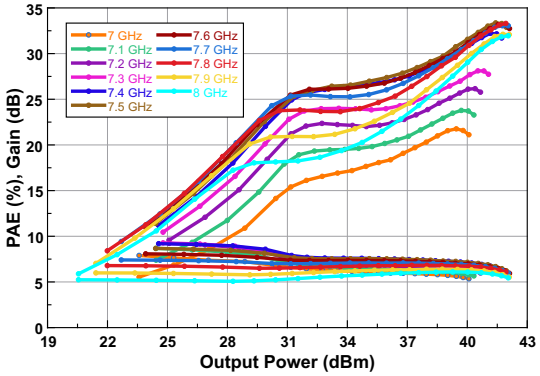

Fig. 4: Measured PAE (%) and Gain (dB) versus output power (dBm) at different frequencies from 7 to 8 GHz.

curve across the entire frequency range confirms the proper Doherty load modulation. Fig. 5 shows the measured RF-pulse output power, PAE and gain at saturation and 8 dB OBO versus frequency. Good agreement is also maintained on the large signal characterization. An output power of 40 to 42 dBm is achieved across the entire BW, accompanied by

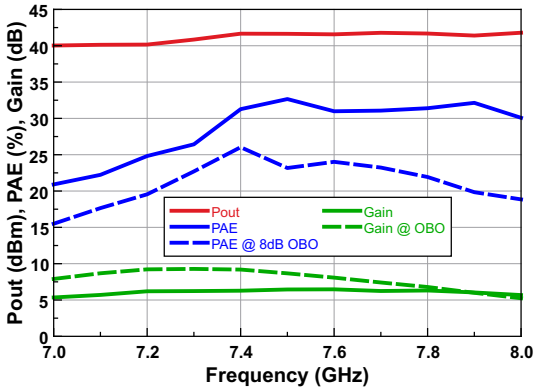

Fig. 5: Measured Output power at saturation (dBm), PAE (%), and gain (dB) versus frequency (GHz).

TABLE I: Comparison with GaN on Si and GaN on SiC MMIC DPAs in FR1 and FR3 bands.

	[12], 2022	[13], 2021	[14], 2024	[15], 2014	[16], 2025	This Work
Technology	GaN/Si 300 nm	GaN/SiC 250 nm	GaN/SiC 120 nm	GaN/SiC 250 nm	GaN/Si 100 nm	**GaN/Si 250 nm**
Architecture	DPA	Unbalanced DPA	DPA	DPA	DPA	**asymmetrical DPA**
Supply Voltage (V)	9	28	28	28	9	**28**
Frequency (GHz)	3.2 - 4.7	4.5 - 6.5	9.6 - 10.4	5.8 - 8.8	17.3 - 20.3	**7 - 8**
Fractional BW (%)	38	37	8	41	16	**13.3**
Stages	Single	Single	Double	Single	Three	**Single**
Linear Gain (dB)	10.9	11	11.5	9.2	-	**9**
P_{sat} (dBm)	30 - 28.9	32.2 - 34.3	35.3 - 36	38	37.3	**40 - 41.6**
PAE_{sat} (%)	44.7 - 43.5	18 - 33	33 - 40	31 - 39	22 - 30	**20.9 - 32.6**
PAE (%) @ OBO (dB)	39.2 - 39.1 @ 6	18 - 28 @ 7.2	23 - 29 @ 6	32 - 41 @ 8.5	23 - 28 @ 6	**15.5 - 26 @ 8**
Chip Size (mm^2)	1.66	7.84	10.95	8.41	30	**16**
Power Density (W/mm^2)	0.6	0.34	0.36	0.75	0.18	**1**

PAE exceeding 20.9 % and gain more than 5.3 dB. The best performance is observed at 7.5 GHz, where the PAE and gain reach 32.7 % and 6.5 dB, respectively. At an OBO of 8 dB, the efficiency ranges from 15.5 % to 26 % throughout the full BW. A comparison with recent MMIC PA designs in GaN on Si and GaN on SiC technologies operating in the FR1 and FR3 bands is summarized in Table I. This work leverages the novel Infineon GaN on Si technology to achieve significantly higher power density compared to recent DPA MMIC designs.

Conclusion

This paper presents a 16 W asymmetrical DPA, designed in Infineon 250 nm GaN on Si technology. The design is targeted for FR3 mid-band in 6G applications and achieves a 32.7 % PEA at peak output power of 41.6 dBm and 26 % at 8 dB OBO with 13.3 % fractional bandwidth from 7 to 8 GHz in compact size 4 mm $\times$ 4 mm, power density 1 W/mm^2. This work demonstrates a peak output power of 41.6 dBm with record power density in a novel GaN on Si technology.

Acknowledgment

This work was supported by the ALL2GaN Project through the EU Chips Joint Undertaking and its members, including the top-up funding by Austria, Belgium, Czech Republic, Denmark, Germany, Greece, The Netherlands, Norway, Slovakia, Spain, Sweden, and Switzerland, under Grant 101111890.

References

[1] F. Wang, A. Yang, D. Kimball, L. Larson, and P. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," IEEE Trans. Microw. Theory Tech., vol. 53, no. 4, pp. 1244–1255, Apr. 2005.

[2] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," IEEE Trans. Microw. Theory Techn., vol. 57, no. 5, pp. 1110–1118, May 2009.

[3] M. P. van der Heijden, M. Acar, J. S. Vromans, and D. A. Calvillo-Cortes, "A 19 W high efficiency wideband CMOS-GaN class-E Chireix RF outphasing power amplifier," in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2011, pp. 1–4.

[4] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," in Proceedings of the Institute of Radio Engineers, vol. 24, no. 9, pp. 1163-1182, Sept. 1936, doi: 10.1109/JRPROC.1936.228468.

[5] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho and B. Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 559-571, Feb. 2015, doi: 10.1109/TMTT.2014.2387061.

[6] W. Chen, G. Lv, X. Liu, D. Wang and F. M. Ghannouchi, "Doherty PAs for 5G Massive MIMO: Energy-Efficient Integrated DPA MMICs for Sub-6-GHz and mm-Wave 5G Massive MIMO Systems," in IEEE Microwave Magazine, vol. 21, no. 5, pp. 78-93, May 2020, doi: 10.1109/MMM.2020.2971183.

[7] J. Schulze and P. Singerl, "RF GaN-on-Si technology powers the future of wireless," Microwave Journal, 2024.

[8] D. D. Pandya, C. Schuberth, S. Ghosh, M. Koh, H. Brech and R. Quay, "Design of a 3.5 GHz Symmetric Doherty PA in an 8-inch GaN on Silicon MMIC Technology for Base Station Applications," 2025 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), Torino, Italy, 2025, pp. 1-4, doi: 10.1109/INMMIC64198.2025.10975382.

[9] N. Tuffy, L. Guan, A. Zhu and T. J. Brazil, "A Simplified Broadband Design Methodology for Linearized High-Efficiency Continuous Class-F Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 6, pp. 1952-1963, June 2012, doi: 10.1109/TMTT.2012.2187534.

[10] J. Moon, J. Kim and B. Kim, "Investigation of a Class-J Power Amplifier With a Nonlinear $C_{\rm out}$ for Optimized Operation," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 11, pp. 2800-2811, Nov. 2010, doi: 10.1109/TMTT.2010.2077970.

[11] G. Lv, W. Chen, X. Liu, F. M. Ghannouchi and Z. Feng, "A Fully Integrated C-Band GaN MMIC Doherty Power Amplifier With High Efficiency and Compact Size for 5G Application," in IEEE Access, vol. 7, pp. 71665-71674, 2019, doi: 10.1109/ACCESS.2019.2919603.

[12] Q. Yu et al., "A Fully Integrated 3.2-4.7GHz Doherty Power Amplifier in 300mm GaN-on-Si Technology," 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Phoenix, AZ, USA, 2022, pp. 144-147, doi: 10.1109/BCICTS53451.2022.10051762.

[13] G. R. Nikandish, R. B. Staszewski and A. Zhu, "Unbalanced Power Amplifier: An Architecture for Broadband Back-Off Efficiency Enhancement," in IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 367-381, Feb. 2021, doi: 10.1109/JSSC.2020.3014244.

[14] F. Manni, R. Giofre, V. Camarchia, A. Piacibello, F. Giannini and P. Colantonio, "A GaN-Based MMIC Doherty Power Amplifier with Class F Peaking Branch," 2024 IEEE/MTT-S International Microwave Symposium - IMS 2024, Washington, DC, USA, 2024, pp. 477-480, doi: 10.1109/IMS40175.2024.10600303.

[15] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov and C. Fager, "A GaN MMIC Modified Doherty PA With Large Bandwidth and Reconfigurable Efficiency," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 12, pp. 3006-3016, Dec. 2014, doi: 10.1109/TMTT.2014.2362136.

[16] A. Piacibello et al., "Design and Extensive NPR Characterization of a Highly Linear SatCom GaN MMIC Doherty PA," in IEEE Transactions on Microwave Theory and Techniques, vol. 73, no. 1, pp. 156-166, Jan. 2025, doi: 10.1109/TMTT.2024.3474092.