THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Wide-Scan Patch Antenna Arrays in Triangular Lattice for K-/Ka-Band 6G SATCOM

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Gothenburg, Sweden, 2026

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Acknowledgements, dedications, and similar personal statements in this thesis, reflect the author's own views.

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Abstract

Satellite communications (SATCOM)-on-the-move (SOTM) user terminals require low-profile, dual-polarized phased arrays with grating-lobe-free 2-D scanning up to $\pm 60^\circ$, while also requiring printed circuit board (PCB) solutions that enable co-location of radiating elements and front-end electronics and scalable measurement setups for connectorized phased-array prototypes. This thesis addresses these requirements through a shared-aperture phased array antenna on a triangular lattice and through a scalable measurement setup for PCB-based dual-polarized wide-scanning phased arrays operating up to the SATCOM Ka-band (27.5–31 GHz).

The antenna design co-integrates a wide-angle impedance matching dielectric layer above the aperture, realized with an air gap, and broadband coaxial microstrip-to-stripline interconnects embedded in the PCB. In an infinite array, Active VSWR < 2 is maintained over 17.9–21.2 GHz and 28.1–30.6 GHz for $\theta_s \leq 60^\circ$ E-/H-plane scan. The measurement setup uses surface-mount device (SMD) SMPM connectors and compact terminations implemented with SMD resistors, eliminating the need for additional fixtures and/or PCB conductor layers. The connector pad is shaped to mitigate the resonance caused by the limited number of pad-grounding vias, and the terminations are designed by co-simulating transmission lines, grounding vias, and resistor equivalent models.

Measurements of 19-element and 127-element prototypes validate the Active VSWR and radiation characteristics of the array, while measurements of test boards validate the repeatable performance of the designed transition and terminations. The results show a PCB-compatible solution for compact K-/Ka-band SATCOM phased arrays and for the characterization of PCB-based dual-polarized wide-scanning phased arrays operating up to the Ka-band.

Keywords: K-band, Ka-band, microstrip antenna arrays, phased arrays, satellite communications, shared-aperture, triangular lattice.

List of Papers

This thesis is based on the following publications:

[A] **Theodoros Pavlidis**, Thomas Schäfer, Artem R. Vilenskiy, Lukas Nyström, Ahmed A. Kishk, Marianna V. Ivashina, "Low-Profile, K-/Ka-Band ±60° 2-D-Scanning Dual-Polarized Patch Antenna Array on a Triangular Lattice for SATCOM-on-the-Move Applications". Submitted to the IEEE Antennas and Wireless Propagation Letters.

[B] **Theodoros Pavlidis**, Thomas Schäfer, Ahmed A. Kishk, Marianna V. Ivashina, "Design Challenges and Solutions for Characterizing Mutual Coupling Coefficients in PCB-based Ka-band Dual-polarized Wide-scan Phased Arrays". Accepted in 20th European Conference on Antennas and Propagation.

Contents

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Acronyms

6G:	Sixth generation (of mobile networks)
PA:	Phased array

SAPA:	Shared-aperture phased array
SATCOM:	Satellite communications
SOTM:	SATCOM-on-the-move
UC:	Unit cell
PCB:	Printed circuit board
AVSWR:	Active VSWR
WAIM:	Wide-angle impedance matching
CATR:	Compact antenna test range
SMD:	Surface-mount device
PBC:	Periodic boundary condition
PPW:	Parallel-plate waveguide
EPIG:	Electroless palladium immersion gold
RL:	Return loss
IL:	Insertion loss
VNA:	Vector Network Analyzer
LEO:	Low Earth orbit
GEO:	Geostationary orbit
BFIC:	Beamforming integrated circuit
mmWave:	Millimeter-wave
FEM:	Finite element method
PEC:	Perfect electric conductor
BFN:	Beamforming network
UT:	User terminal

Tx:	Transmit
Rx:	Receive
EDM:	Electric discharge machining

Part I

Overview

CHAPTER 1

Introduction

1.1 Motivation

Satellite communications (SATCOM) are considered a vital component of future 6G networks, essential for realizing global coverage [1]. Global coverage will be enabled by low Earth orbit (LEO) [2] and geostationary orbit (GEO) [3] satellites. To connect to these satellites in the SATCOM Ku-, K-, and Ka-bands, user terminals (UTs) featuring high gain antennas are typically used [4]. Furthermore, the UT must support two polarizations in both transmit (Tx) and receive (Rx) bands for robust connectivity [5] and increased system capacity [3]. UTs for SATCOM-on-the-move (SOTM) face additional constraints, since user mobility necessitates rapid 2-D beamsteering over a large scan volume ($\theta_s \leq 60°$). Simultaneously, SOTM scenarios impose strict volume constraints on UT equipment to avoid degrading vehicle performance.

An attractive solution for SOTM scenarios is the planar phased array (PA) [7], [8], [9], due to its rapid electronic beamsteering and low profile. PA profile can be further reduced via an integrated PA [10] architecture, with radiators and beamforming integrated circuits (BFICs) co-located in a single low-cost printed circuit board (PCB), as shown in Fig. 1.1. Further compactness

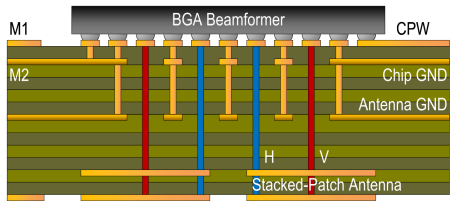


Figure 1.1: PCB stackup of integrated phased array [6].

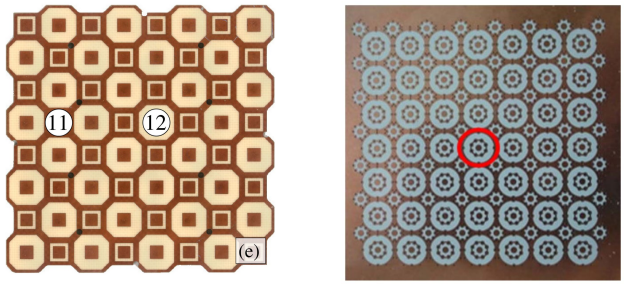
can be achieved by a shared-aperture PA (SAPA) configuration, where the Tx and Rx paths operate through one common antenna, as demonstrated for dual-polarized PAs in the Ku-band [11].

However, K-/Ka-band operation introduces challenges for integrated SAPA design not encountered in the Ku-band. Specifically, K-/Ka-band SATCOM SAPAs require a larger frequency ratio ($f_{high}/f_{low} > 1.75:1$) compared to the Ku-band ($f_{high}/f_{low} > 1.36:1$) for full band coverage [5], [12]. Furthermore, K-/Ka-band operation results in increased material losses and interconnect parasitic reactances as well as thermal and routing problems due to the physically smaller element spacing necessary to avoid grating lobes [13].

1.2 State-of-the-Art mmWave Wide-Scanning Dual-Polarized SAPA Design and Challenges

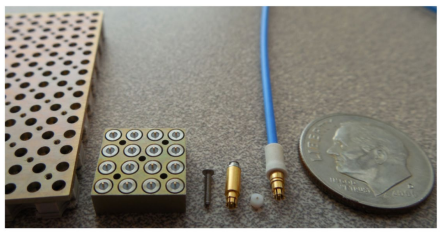
SAPAs with Interleaved Dual-Band and Single-Band Elements

To relax element-spacing constraints, several recent works adopt an interleaved lattice of dual-band and single-band elements [14], [15], [16], [17], [18]. Examples of reported K-/Ka-band SAPAs are shown in Fig. 1.2. Interleaving allows two different element spacings for the two bands, and thus reduces the number of lower-frequency BFIC channels required for a given aperture area. On the other hand, to accommodate two different element types, interleaved lattice SAPAs need to sample the array aperture very densely. As a consequence, interleaved architectures sacrifice dual-polarization [14], [15], [16] or feature limited ($\theta_s < 60°$) scan range in one of the bands [17], [18].



(a) (b)

Figure 1.2: Examples of dual-polarized SAPA antennas with two types of elements interleaved. (a) in [18], and (b) in [14].



(a)

(b)

Figure 1.3: Examples of dual-polarized SAPA antennas with a single element type and non-PCB features. (a) Aluminum plate with coaxial interconnects and measurement equipment [19], and (b) additively manufactured Vivaldi array [20].

SAPAs with a Single Element Type

In lieu of interleaving two types of elements, a single wideband or dual-band element can be used. The additional design freedom afforded by a uniform array lattice can then be leveraged to simultaneously achieve dual polarization and wide-angle scanning in several frequency bands [19], [20], [21], [22], [23]. A key challenge lies in implementing both the radiators and the radiator-BFIC interconnects with PCB technology. As an alternative, either the radiators or the interconnects can be implemented using fabrication technologies other than PCB [Fig. 1.3]. Examples include radiators fabricated via additive manufacturing [20], milling and electric discharge machining (EDM) [24], as well as coaxial interconnects realized with metal pins in dielectric [19], [21]. Although these alternative technologies offer additional degrees of freedom, competitive performance, and simplify PCB stackups, they require precise assembly for BFIC–radiator integration that can be complicated and costly in millimeter-wave (mmWave) applications. Some pioneering works have proposed fully-metallic mmWave PAs with tightly integrated electronics and radiators [25], [26], but the experimentally validated concepts have so far been limited to one polarization and $f_{high}/f_{low} < 1.25 : 1$.

Arrays with PCB-compatible interconnects and radiators, on the other hand, are further restricted by the design rules of the PCB process. Design rule restrictions can result in some shortcomings, specifically

- Limited element area and inter-element separation, exacerbated when elements are arranged in a rectangular lattice, as commonly done in dual-polarized, wideband, wide-scanning arrays of connected and tightly coupled elements [22], [23], [24], [27]. While a triangular lattice [28] enables a $\approx 15.5\,\%$ larger element footprint versus a rectangular lattice for the same scan volume, most implementations of connected or tightly coupled arrays in triangular lattices are limited to operation < 21 GHz [29], [30], [31].
- Narrow scan impedance bandwidth, caused by constraints in radiator or interconnect design and their co-location, or non-radiating resonances [32] (scan blindness) manifesting in the PCB dielectric layers.
- Fabrication difficulties due to complex PCB stackups, resulting in limited experimental validation with prototype measurements [33]. Experimental validation is essential for mmWave PA antennas, as it assesses

their robustness against manufacturing tolerances, material loss and design rule constraints.

Table 1.1 summarizes the state-of-the-art K-/Ka-band wide-scanning, dual-polarized PAs with a large frequency ratio ($f_{high}/f_{low} > 1.4:1$) that have been experimentally validated. As seen, DP PCB-integrated arrays with embedded interconnects are uncommon, particularly when wide-angle scanning with low Active VSWR (AVSWR < 2) and a triangular lattice configuration are required.

1.3 Wideband and Wide-scanning Patch Array Antennas

The microstrip patch has long been a popular antenna array element owing to its usually low profile, ease of fabrication, and strong potential for integration [34]. Patch-based PAs are commonly implemented on triangular lattices [8], [9], [11], [12], which allow larger inter-element spacings compared to rectangular lattices for the same scan volume. For frequencies up to the X-band (8–12 GHz), PAs based on multilayer PCBs with patches supported by low-permittivity substrates have demonstrated measured broadside impedance bandwidths exceeding one octave ($f_{\text{high}}/f_{\text{low}} > 2{:}1$) [35]. Patch PAs with $f_{\text{high}}/f_{\text{low}} = 3{:}1$ at broadside have been explored theoretically [36]. For beyond-octave bandwidth patch PAs, 2-D beam scanning up to $\pm 55^\circ$ has been reported, albeit in an undisclosed frequency band [37].

Despite these promising results, several limitations remain. Patch PAs with beyond-octave broadside bandwidth are often single-polarized [35], [38] and do not address the mmWave operation challenges mentioned in the previous section. An alternative approach [39], uses patches etched on very thick (approximately one-wavelength) low-cost laminates combined with ground plane apertures to mitigate scan blindness, achieving simulated scanning up to $\pm 60^\circ$ with AVSWR < 3 over the Ka-band. However, the back radiation from the ground plane apertures [39] significantly complicates radiator–BFIC integration, limiting the practical applicability of this solution. Up to this point, 2-D wide-scanning, dual-polarized patch PAs suitable for integration with BFICs for K-/Ka-band SATCOM are limited to single-band implementations, typically with $f_{\text{high}}/f_{\text{low}} < 1.25{:}1$ [6], [7], [9].

Table 1.1: Comparison of experimentally validated wide-angle scanning dual-band and wideband K-/Ka-band phased arrays with dual polarization. The highlighted columns correspond to PA antennas with both radiators and interconnects realized in PCB.

Ref.		[20]	[21]	[18]	[23]	[22]
Polarization		Dual linear	Dual linear	Dual linear	Dual circular	Dual linear
Lattice		Rectangular	Triangular	Interleaved	Rectangular	Rectangular
UC footprint		$0.25\lambda^2_{\text{high}}$	$0.334\lambda^2_{\text{high}}$	$0.613\lambda^2_{\text{high}}$ (K) $0.307\lambda^2_{\text{high}}$ (Ka)	$0.226\lambda^2_{\text{high}}$	$0.176\lambda^2_{\text{high}}$
Element type		Vivaldi	E-dipole	Patch	E-dipole	M/E-dipole
Manu-facturing		PCB + 3-D printed	PCB + Al. plate	PCB	PCB	PCB
Feed		PCB + 3-D printed	Plate-mounted coax	PCB	PCB	PCB
Profile		$1.85\lambda_{\text{high}}$	$0.47\lambda_{\text{high}}$	$0.09\lambda_{\text{high}}$	$0.26\lambda_{\text{high}}$	$0.15\lambda_{\text{high}}$
$f_{\text{high}}/f_{\text{low}}$ (sim.)[2]		1.67:1	3.31:1	1.57:1	1.75:1	1.42:1
Scan B/W (sim.)[1]	Broad-side	18–30 (50%)	13–43 (107%)	19.2–19.8 (3.1%) 28.7–30.2 (5.1%)	17.7–21.2 (18%)* 27.5–31 (12%)*	26–37 (34.9%)
	E-60°	18–30 (50%)	7–38 (138%)	N/A[3]	N/A[4]	26–38 (37.5%)
	H-60°	18.5–29.5 (45.8%)	0%	N/A[3]	N/A[4]	26–27.2 (4.5%) 33–37 (11.4%)

[1]in GHz, AVSWR < 2. [2]Defined for AVSWR < 2 at broadside. [3]Not available - radiating grating lobes for 60° scanning beyond 29.2 GHz. [4]Not available - AVSWR versus scan not reported. *Return loss in 1×8 array configuration, for other works infinite array results are reported. E-60° - E-plane, $\theta_s = 60°$, H-60° - H-plane, $\theta_s = 60°$.

1.4 Scientific Contributions

In this thesis, we focus on the design of a PA in PCB technology for the SATCOM K-/Ka-bands (17.7–21.2 GHz and 27.5–31 GHz) as well as addressing the challenges of experimentally validating a dual-polarized PCB-based PA in these high frequencies. Specifically, the novel contributions include:

1. A low-profile, dual-polarized SAPA antenna operating over 17.9–21.2 GHz and 28.1–30.6 GHz with a 2-D ±60° scan range and Active VSWR < 2, targeting compact SOTM user terminals. The main contribution is the resolution of the conflicting requirements of dual-band wide-angle scanning operation, and radiator–interconnect co-location in a single PCB. In contrast to recent SAPAs that compromise dual polarization or bandwidth–scan performance, and solutions that rely on non-PCB fabrication or lack PCB-compatible feeds, the proposed design enables co-location of radiating elements and front-end electronics on a single low-cost PCB.

   This is achieved by:

   a) Co-integrating a broadband coaxial microstrip-to-stripline interconnect and a dual-band dual-polarized patch antenna in one PCB,

   b) introducing a high-permittivity dielectric sheet above the aperture, realized with an air gap, and

   c) leveraging a triangular lattice to alleviate routing and packaging constraints while preserving grating-lobe-free operation for wide-angle scanning.

   Measurements of 19-element and 127-element prototypes validate the Active VSWR versus scan for 2-D scanning as well as the radiation characteristics. (**Paper A**).

2. A scalable measurement setup for PCB-based, dual-polarized, wide-scanning phased arrays operating up to the Ka-band frequencies, addressing challenges related to dense element spacing and the non-ideal performance of commercial surface-mount device (SMD) resistors at mmWave, without resorting to additional fixtures or conductor layers.

   The contribution lies in enabling a measurement approach that:

a) Minimizes the footprint of the connector transition by shaping the connector pad, reducing the number of pad-grounding vias required for mmWave operation and increasing flexibility in connector placement. As a result, all ports corresponding to one polarization can be connectorized.

b) In addition, miniaturized terminations using SMD resistors are designed by co-simulating transmission lines, grounding vias, and resistor equivalent models. The impact of resistor behavior at mmWave frequencies is addressed by evaluating off-the-shelf components using commercially available equivalent models to design two termination solutions.

Test boards for the coaxial-to-microstrip transition and terminations are fabricated, and their S-parameters are measured, demonstrating repeatable performance. The developed setup supports the fabrication and measurement of PA prototypes and is compatible with PCB-based implementations. (**Paper B**)

1.5 Outline

Following the introduction in **Chapter 1**, **Chapter 2** presents the design of the proposed K-/Ka-band SAPA antenna. The wide-angle impedance matching (WAIM) with a high-permittivity dielectric sheet and the interconnect integration are described. Experimental validation of AVSWR and radiation characteristics is demonstrated. **Chapter 3** focuses on the measurement setup for PCB-based wide-scanning, dual-polarized K-/Ka-band PAs. First, the connector pad is shaped to increase pad placement flexibility. Then, off-the-shelf SMD resistors are evaluated for mmWave operation and two compact terminations are designed. The connector pad and termination designs are validated with test board measurements. **Chapter 4** provides a summary of the included papers. Finally, concluding remarks are made in **Chapter 5** and plans for future work are discussed.

CHAPTER 2

K-/Ka-Band, Dual-Polarized, ±60° 2-D-Scanning Patch Phased Array Antenna on a Triangular Lattice

This chapter focuses on a novel low-profile, dual-polarized SAPA antenna design operating over the SATCOM K-/Ka-bands with a ±60° scan range. Starting from a dual-band, dual-polarized patch antenna, WAIM is achieved with a dielectric sheet placed above the aperture. Afterwards, wideband interconnects are integrated in a way that does not perturb impedance matching. The triangular lattice is leveraged to alleviate routing and packaging constraints. Experimental validation of both AVSWR and radiation characteristics is demonstrated with measurements of 19-element and 127-element prototypes, respectively.

2.1 Wide-Angle Impedance Matching of a Dual-Band, Dual-Polarized Patch Phased Array

As a starting point for the design process, a cross-slot fed [40] patch array in a triangular lattice was designed to achieve good impedance matching (AVSWR < 2) at broadside in the infinite array environment. This initial unit cell (UC) is depicted in Fig. 2.1. As shown in Fig. 2.1(b) the UC includes five conductor layers in Astra MT77 laminates ($\varepsilon_r = 3$, $\tan\delta = 0.0017$). The exterior conductor layer has a different thickness to account for the electroless palladium immersion gold (EPIG) surface finish. The laminates are bounded by Astra MT77 1067-style prepregs ($\varepsilon_r = 2.98$, $\tan\delta = 0.0019$). Based on previous studies [41], the surface roughness of the conductor layers and vias is accounted for with the Huray model [42], assuming copper conductivity, a nodule radius of 0.7 μm and a surface ratio of 3.8. Two striplines in layers L4 and L5 [Fig. 2.1(c)] feed a cross-slot on layer L6. This cross-slot in turn excites a microstrip patch etched on layer L8. At this stage, the UC does not include interconnects to lower layers (and ultimately the BFIC). Instead, the striplines are directly excited by wave ports, as shown in Fig. 2.1(c). Furthermore, a perfect electric conductor (PEC) boundary condition is enforced in the stripline layers (L1-L6) to suppress parallel-plate waveguide (PPW) modes [43]. The PEC boundary condition can be replaced by closely-spaced vias in a later design stage.

The UC is simulated with the finite element method (FEM) in Ansys HFSS. Periodic boundary conditions (PBCs) are enforced on the UC sidewalls and a Floquet port is placed above the aperture to simulate a 2-D infinite array environment. Then, the reflection of the TE_{00} and TM_{00} Floquet modes from the UC is investigated. Examining the UC for excitation of the Floquet port, rather than the antenna port, provides additional insights for achieving impedance matching. As shown in Fig. 2.2(a), when the Floquet port reference plane is shifted to 1.5mm above the aperture, the Floquet aperture admittance $Y_{\mathrm{a}\,00}^{\mathrm{TE/TM}}$ exhibits a reactive offset towards the inductive (upper half) region. Nevertheless, $Y_{\mathrm{a}\,00}^{\mathrm{TE/TM}} \approx 1$. Therefore, impedance matching can be achieved by a capacitive shunt susceptance b_s placed at the reference plane to compensate $\mathrm{Im}\{Y_{\mathrm{a}\,00}^{\mathrm{TE/TM}}\}$ for all three scan angles. Here, the shunt susceptance is realized using a high-permittivity dielectric sheet made

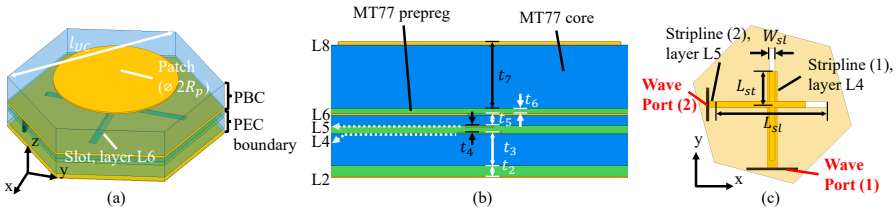


Figure 2.1: Geometry of the initial UC. (a) 3-D view with semi-transparent dielectric layers, (b) side view of PCB layers, and (c) L4-L6 layers with semi-transparent L6 layer. $R_p = 1.7$, $t_2 = 2t_4 = 2t_6 = 0.128$, $t_3 = 0.381$, $t_5 = 0.127$, $t_7 = 0.762$, $L_{\mathrm{st}} = 0.6$, $L_{\mathrm{sl}} = 4$, $W_{\mathrm{sl}} = 0.2$, and $l_{\mathrm{UC}} = 5.1$. Stripline conductor widths (not noted in Figs.): are $W^{(1)}_{\mathrm{STL}} = 0.37$, $W^{(2)}_{\mathrm{STL}} = 0.24$. L8 conductor thickness: 0.042. L2-L6 conductor thickness: 0.018. Units: millimeters.

of Rogers RO3010 substrate ($\varepsilon_r = 11.2$, $\tan\delta = 0.0022$) of standard thickness $t_9 = 0.13$ mm. The resulting modal reflection from the aperture, including the theoretically calculated b_s, is illustrated in Fig. 2.2(b). The wide-angle impedance matching (WAIM) sheet results in modal VSWR marginally above or below 2. The analytically computed b_s, which is shown in Fig. 2.2(c), is calculated according to [44]

$$\text{H-plane scan: } b_s(\theta_s) = (\varepsilon_r - 1)\frac{2\pi t_9}{\lambda_0}\frac{1}{\cos\theta_s}, \tag{2.1}$$

$$\text{E-plane scan: } b_s(\theta_s) = (\varepsilon_r - 1)\frac{2\pi t_9}{\lambda_0}(\cos\theta_s - \frac{\sin^2\theta_s}{\varepsilon_r\cos\theta_s}). \tag{2.2}$$

To validate the effectiveness of the WAIM sheet, the AVSWR of port 1 is compared for the UC with and without the WAIM sheet in Fig. 2.3. The WAIM sheet improves AVSWR for scanning in both principal planes, with AVSWR < 2 for $\theta_s \leq 60°$ up to 30.8 GHz.

2.2 PCB-Embedded Interconnect Integration

Since the UC without interconnects is well-matched, cascading interconnects with high return loss (RL) will preserve the AVSWR of the full-UC, provided the field distribution (and therefore the antenna port input impedances) is not strongly disturbed.

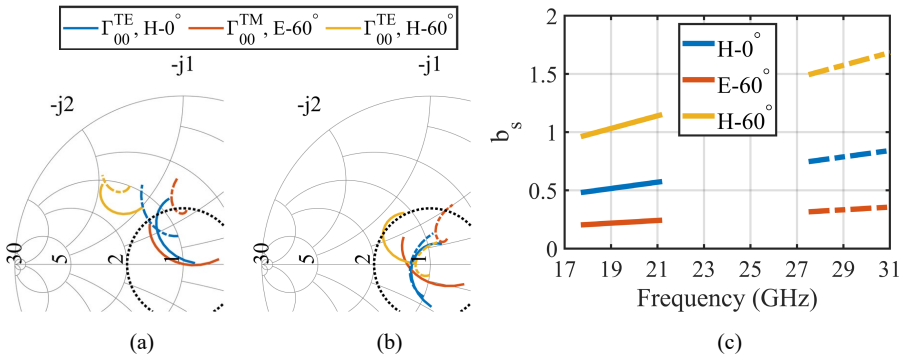


Figure 2.2: WAIM of UC without interconnects. Simulated co-polarized (port 1 polarization) Floquet mode reflection coefficient of the UC aperture for (a) the UC without b_s, and (b) the UC with b_s. (c) Analytically computed shunt susceptance b_s of the WAIM sheet normalized to free space impedance. For (a) and (b), the reference plane is 1.5 mm above the patch substrate. The solid lines and dash-dotted lines correspond to the K- and Ka-band, respectively.

The coaxial interconnect geometry is depicted in Fig. 2.4. The interconnects connect the striplines on L4 and L5, used in the UC feed of section 2.1, to microstrip lines in the external PCB layer L1. The interconnects use seven ground vias to minimize leakage (see Fig. 2.4(a)) [45]. The interconnect signal and ground vias are identical. Since the vias will be manufactured with sequential lamination, identical vias minimize the number of lamination cycles (for the prototypes presented later two lamination cycles were employed), simplifying the fabrication process. However, using identical vias necessitates the introduction of apertures on L6, as shown in Fig. 2.4(a), to avoid shorting the interconnect signal via. Furthermore, the signal vias feature L4-L6 and L5-L6 stubs, whose parasitic reactances might limit RL [46].

To ensure that the interconnects exhibit high RL, they are optimized separately from the antenna and with their microstrip and stripline conductors connected to 50 Ω ports. The resulting S-parameters for this configuration and for port reference planes located at the signal via are depicted in Fig. 2.5. As shown in Figs. 2.5(a) and (b), the interconnect input admittances on the stripline sides shift towards the capacitive region for increasing frequencies. The capacitive shift could be neutralized with decreased L6 pad diameters

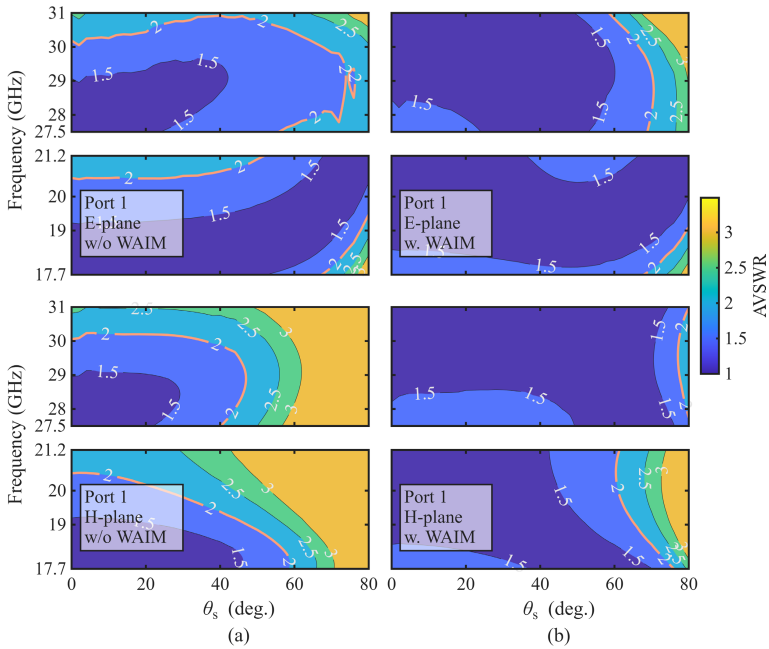


Figure 2.3: Simulated port 1 AVSWR of the UC without interconnects in a 2-D infinite array for E- and H-plane scanning. (a) without and (b) with the WAIM sheet.

(p_{L6}) or eliminating the via stub, at the cost of increased fabrication complexity. Despite the capacitive shift, the interconnect RL is marginally lower than 20 dB or better in the two bands [Figs. 2.5(c) and (d)]. Also, the interconnect insertion losses (ILs) remain below 0.2 dB, minimizing the reduction of UC realized gain.

Next, the interconnects are placed in the UC from section 2.1. To determine the positions of the interconnects in the UC, the E-field on L6 for port 1 excitation is examined (see Fig. Fig. 2.6(a)). The selected interconnect positions are away from strong E-field regions near the slot centers and in line with them, allowing stripline routing without bends. Additionally, the interconnect positions respect the spatial constraints of the equilateral triangular lattice, where each element has six equidistant neighbors. There is some leakage from the interconnect L6 apertures, as can be seen in Fig. 2.6(b), re-

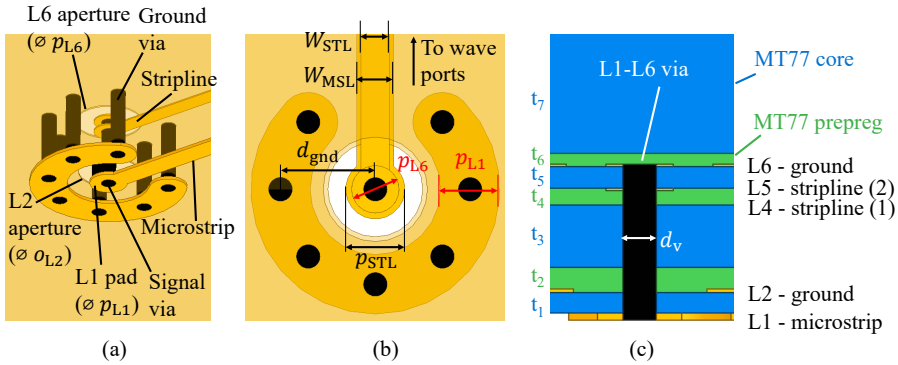


Figure 2.4: Interconnect geometry. (a) 3-D view without dielectric and with semi-transparent ground planes. (b) View from L6 ground plane side without dielectric and with semi-transparent ground planes. (c) Side view. For both interconnects: $t_1 = t_5 = 0.127$, $t_2 = 2t_4 = 2t_6 = 0.128$, $t_3 = 0.381$, $t_7 = 0.762$, $p_{L1} = 0.5$, $p_{L6} = 0.4$, $o_{L2} = 0.8$, $d_{gnd} = 0.8$, $W_{MSL} = 0.31$, and $d_v = 0.2$. For port (1) interconnect: $W_{STL}^{(1)} = 0.37$, $o_{L6}^{(1)} = 1.1$. For port (2) interconnect: $W_{STL}^{(2)} = 0.24$, $o_{L6}^{(2)} = 0.88$. Units: millimeters.

sulting in increased orthogonal port coupling. Specifically, peak port coupling to port 2 when port 1 is excited increases from −19.1 dB to −12.4 dB (for $\theta_s \leq 60°$ scanning in the E-/H-planes).

The significant number of vias (8 per interconnect) and the substantial interconnect footprint relative to UC size mostly compensate for the elimination of the PEC boundary condition used in Sec. 2.1. Nevertheless, to guarantee that the UC remains PPW mode-free, two more vias per UC are placed. The resulting UC geometry is illustrated in Fig. 2.7. Since ground plane apertures were introduced on L2 for the interconnect signal vias, an additional Floquet port is placed behind the aperture, as shown in Fig. 2.7(i).

Fig. 2.8 presents the AVSWR with interconnects for E- and H-plane scanning for both ports. A comparison of Figs. 2.8(a) and (b) establishes that the two UC ports exhibit similar behavior with scan, as a result of the minimal topological differences between the two ports. Also, comparing Fig. 2.3(b) with 2.8(a) confirms that port 1 AVSWR is similar before and after the interconnect integration.

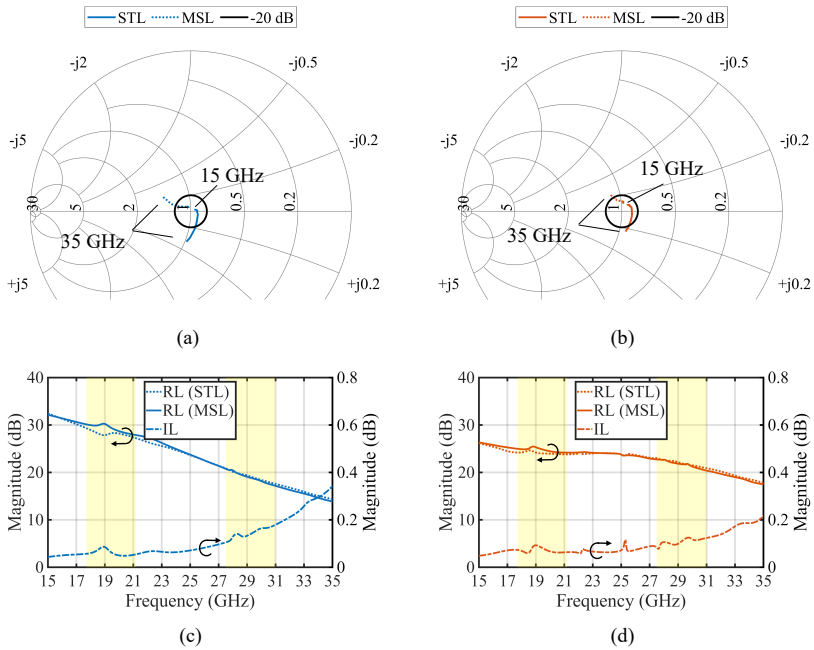


Figure 2.5: Simulated S-parameters of the interconnects outside the array. (a) Reflection S-parameters of the port 1 interconnect, (b) Reflection S-parameters of the port 2 interconnect, (c), RL and IL of the port 1 interconnect, and (d) RL and IL of the port 2 interconnect. STL - stripline port, MSL - microstrip port.

The port 1 realized gain in a 2-D infinite array environment is evaluated from the transmission coefficients between port 1 and the modes of the Floquet port situated above the aperture, following the approach in [47]. The results are depicted in Fig. 2.9. As observed, the co-polarized realized gain closely follows the theoretical limits for scanning angles up to at least $\theta_s \leq 60°$. A slightly increased degradation is noted at 31 GHz, which can be attributed to surface wave excitation in the patch substrate for wide-angle scanning. Nevertheless, for all frequencies, the realized gain for $\theta_s \leq 60°$ scanning in the principal planes remains within 4.9 dB of the theoretically attainable values at broadside.

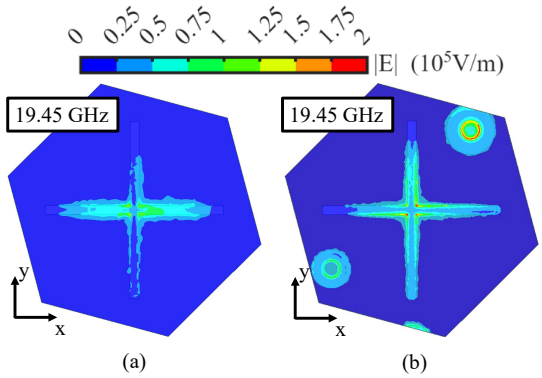


Figure 2.6: (a) E-field on layer L6 when port 1 is excited for the UC without interconnects, and (b) E-field on layer L6 when port 1 is excited for the UC with interconnects and two additional vias.

2.3 Experimental Validation

To experimentally validate simulations and robustness with respect to manufacturing tolerances of the UC described in Sec. 2.2, two connectorized phased array prototypes have been fabricated. For lower-frequency applications, experimental characterization of 2-D phased arrays is performed using a single fully connectorized prototype and low-cost connector hardware (such as SMA connectors) [49]. In this manner, both AVSWR and realized gain can be measured in one prototype of numerous elements. Unfortunately, full connectorization for both polarizations in the Ka-band requires expensive SMPS connectors and terminations [21], leading to a prohibitive prototyping cost for a large, fully-connectorized array. For example, consider a dual-polarized array prototype of the proposed UC and aperture size of $5\lambda_{high} \times 5\lambda_{high}$, which according to [3] is the minimum required for approximating the performance of an element embedded in a large, wide-scanning array at its highest operating frequency f_{high}. Using the SMPS termination with part number 8038-4007 by Amphenol SV Microwave, we estimated the termination cost to be approximately 30000 €.

As a compromise, we have adopted a two-prototype approach as follows:

1. Realized gain was measured for one port of an element embedded in a

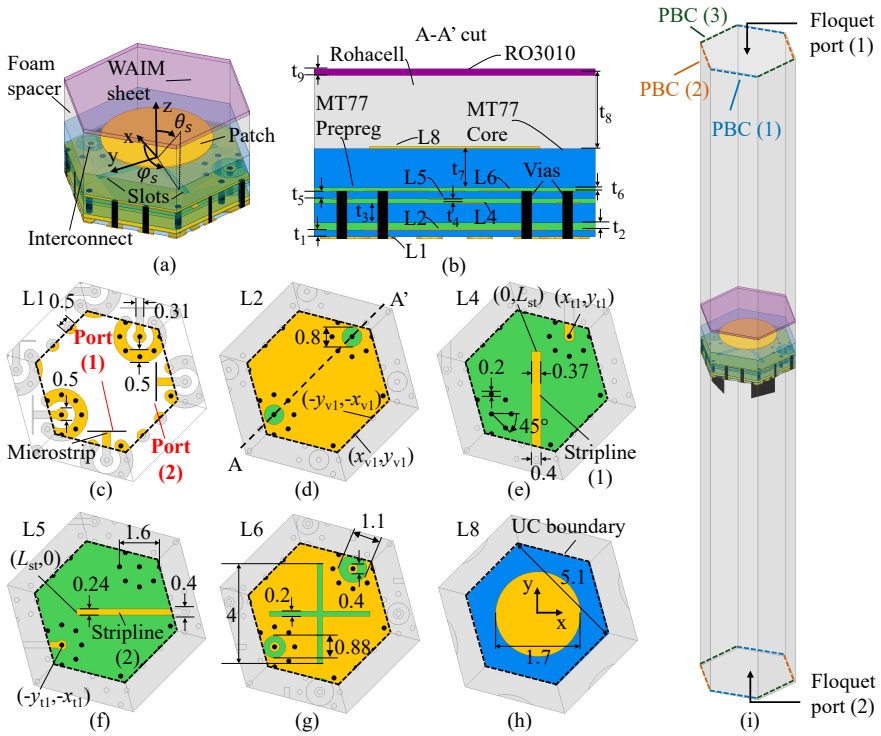


Figure 2.7: UC with interconnects and WAIM sheet. (a) 3-D view with semi-transparent dielectric layers, (b) side view, (c)-(h) PCB conductor layers, and (i) 3-D view with PBCs and Floquet port. $t_1 = t_5 = 0.127$, $t_2 = 2t_4 = 2t_6 = 0.128$, $t_3 = 0.381$, $t_7 = 0.762$, $t_8 = 1.5$, $t_9 = 0.13$, $x_{v1} = 1.456$, $y_{v1} = -2.15$, $x_{t1} = 1.32$, $y_{t1} = 1.8$, $L_{st} = 0.6$. The area outside the dashed lines corresponds to the adjacent UCs. Unless otherwise stated, units: millimeters.

127-element array prototype.

2. Active VSWR was computed from measurements of mutual coupling for one port of an element embedded in a 19-element array prototype.

The two prototypes, the measurement procedures, as well as the measurement results are described in the following subsections.

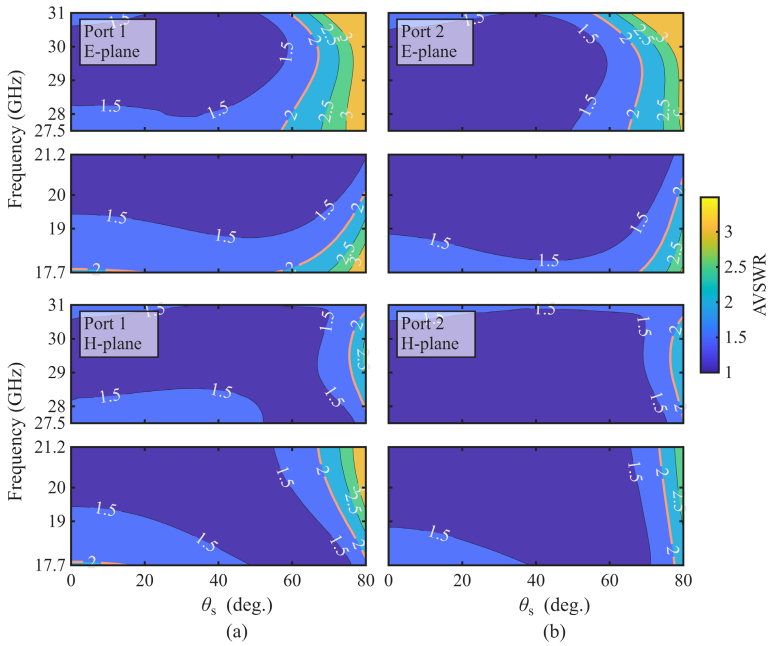


Figure 2.8: Simulated AVSWR in a 2-D infinite array of the UC with interconnects for E- and H-plane scanning. (a) port 1, (b) port 2.

127-Element Prototype for Realized Gain Measurement

The 127-element prototype PCB is presented in Fig. 2.10. The prototype features a single port connectorized with an SMPM SMD connector, while the other ports are terminated with SMD resistors [Fig. 2.10(a)]. Some of the prototype's edge elements utilize dummy interconnects (without signal vias) to form complete cavities on their feed layers and suppress the excitation of PPW modes. The prototype array has a hexagonal shape, which is formed by a series of concentric hexagonal rings of elements [50], as shown in Fig. 2.10(b). This arrangement enables a center element for triangular lattice arrays, with an equal number of elements on each side of the center element. The WAIM sheet and the foam spacer are attached to the prototype PCB with screws, as shown in Fig. 2.10(c).

The prototype's realized gain was measured using the compact antenna

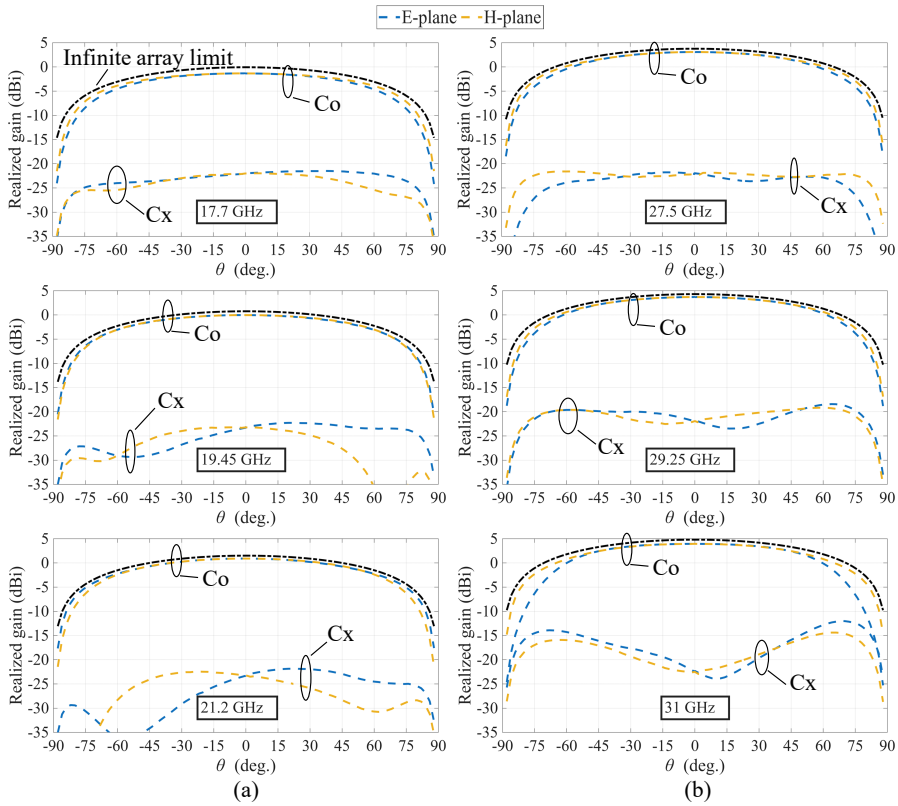


Figure 2.9: Simulated realized gain for port 1 in the 2-D infinite array environment, for E- and H-plane scanning. (a) K-band and (b) Ka-band. Also shown is the realized gain limit in a 2-D infinite array environment [48]. The port 1 reference plane is at the center of the signal via on layer L1.

test range (CATR) setup of the Chalmers anechoic chamber. As shown in Fig. 2.11(a), the 127-element prototype is mounted on a 3-D printed plastic holder, which in turn is mounted on the chamber's metal mast. The effect of this metal mast on measurements was minimized by attaching absorbers on it with dual lock fasteners. The prototype is connected to the Vector Network Analyzer (VNA) via a short (15 cm-long) 0.047-inch 2.4 mm-to-SMPM coaxial cable, which in turn is connected to the chamber's coaxial

Figure 2.10: 127-element prototype. (a) PCB backplane, (b) PCB antenna side, and (c) antenna side with foam spacer and WAIM sheet. The sixth hexagonal ring of elements is marked with dashed lines in Fig. (b).

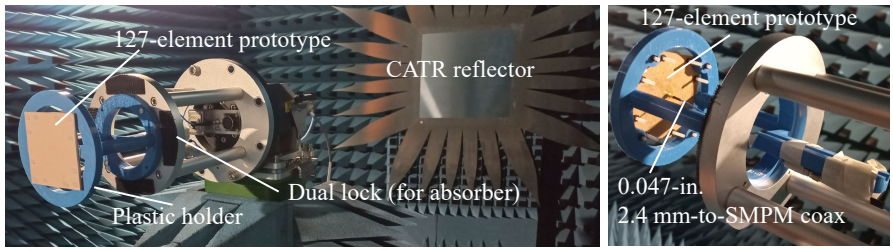


Figure 2.11: 127-element prototype measurement setup. (a) Antenna side and CATR reflector. (b) PCB backplane and cable connection. During measurements, the metal mast was covered with absorbers attached with dual lock fasteners.

cable, as shown in Fig. 2.11(b). The 0.047-inch coaxial cable is employed to avoid damage to the delicate SMD connector of the prototype. The loss of this cable (approximately 0.9 dB in the K-band and 1.1 dB in the Ka-band) has been extracted from the measured realized gain.

The measured and simulated realized gains are compared in Fig. 2.12 for the lowest, center and highest frequencies of the two bands. The results show very good agreement, particularly for the co-polarized components, where only minor differences are observed. Given the inherent challenges of mmWave fabrication and measurement accuracy, this agreement is excellent. The most notable deviations occur in the H-plane cross-polarized components in the Ka-band, as shown in Fig. 2.12(b). However, the cross-polarized components are at significantly lower levels than the co-polarized ones, and therefore, are more susceptible to the effects of fabrication inaccuracies.

19-Element Prototype for Active VSWR Evaluation

The 127-element prototype of the previous subsection only enables validation of metrics involving a single port. Therefore, to measure mutual coupling and compute Active VSWR [51], [52], a 19-element PCB was fabricated and is shown in Fig. 2.13. As can be seen in Fig. 2.13(a), the antenna elements are once more arranged in hexagonal rings around a center element. The 19-element prototype has ten connectorized ports of the same polarization (see 2.13(b)) to compute AVSWR of the center element “6”. The prototype’s

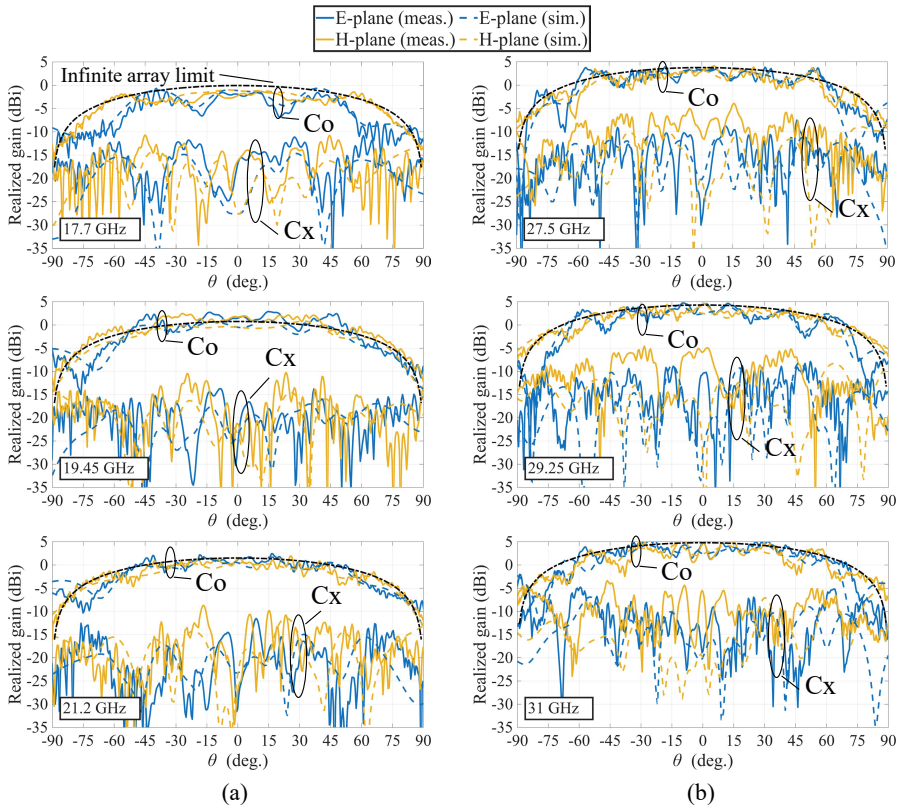
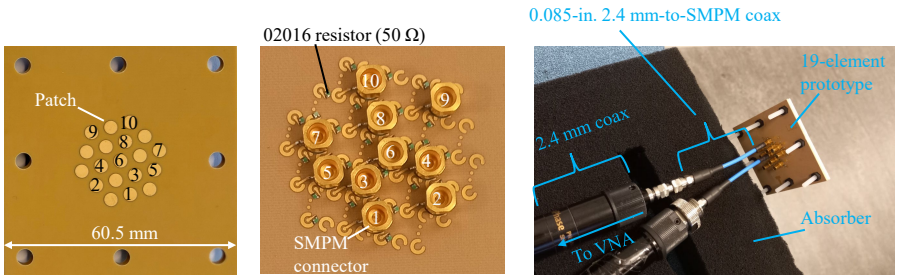


Figure 2.12: Simulated and measured realized gain for the center element of the 127-element array, in the E- and H-planes. (a) K-band and (b) Ka-band. The loss of 2.4 mm-to-SMPM cables has been excluded from the results (0.9 dB and 1.1 dB in the K- and Ka-band, respectively). Also shown is the realized gain limit in a 2-D infinite array environment [48].

S-parameters were found sufficiently symmetric in simulations to permit accurate AVSWR computation [51], [52] for element "6" via S-parameter symmetry. Therefore, only ten ports were connectorized. The non-connectorized ports were terminated with SMD resistors. A photograph of the measurement setup is shown in Fig. 2.13(c). To avoid damaging the SMD connectors with



(a) (b) (c)

Figure 2.13: 19-element prototype. (a) PCB antenna side, (b), PCB backplane and (c) Measurement setup. The non-measured connectors in (c) are terminated with 50 Ω coaxial terminations.

the heavy 2.4 mm cables connected to the VNA, thinner 0.085-inch 2.4 mm-to-SMPM cables were used. Calibration with the 18CK010-150 calibration kit from Rosenberger allows the reference plane to be shifted to the SMPM interface of the 0.085-inch cables. The non-measured coaxial connectors were terminated using 50 Ω coaxial terminations with part number 18K15R-0.5E3 from Rosenberger.

Unfortunately, the solder joints of two connectors, labeled as "6" and "3" in Fig. 2.13(b), were damaged during measurement. As a result, it became impossible to measure S_{63} and S_{65}. Instead, AVSWR was computed from the eight measured S-parameters using symmetry and assuming ports "3" and "5" (and their corresponding symmetric ports with respect to element "6") are not excited.

To simplify simulations, the prototype was simulated without connectors. The simulated S-parameters of the connector were then cascaded to the array's simulated S-matrix. The resulting AVSWR is compared with the measured one for the same elements excited in Fig. 2.14. Simulations and measurements generally agree, with the most notable differences observed for the E-plane scan in the K- band. The differences between the simulation and measurements can be attributed to manufacturing tolerances and higher than simulated connector impedance mismatch, which was confirmed from test board measurements that will be described in Chapter 3.

The proposed PA antenna is compared with the state-of-the-art dual-polarized

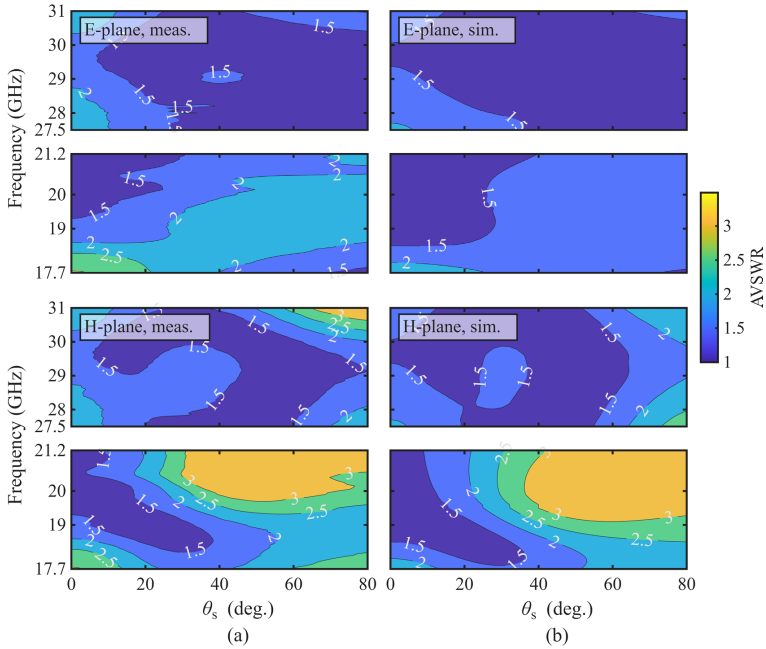


Figure 2.14: Simulated and measured AVSWR of the center element "6" of the 19-element prototype for E- and H-plane scanning. (a) measured and (b) simulated.

2-D scanning arrays in the K-/Ka-bands in Table 2.1. Compared to [22], the proposed SAPA has a larger frequency ratio that allows operating in both K- and Ka-bands. In addition, it offers grating-lobe-free ±60° 2-D scan throughout both bands, in contrast to the interleaved lattice SAPA in [18]. Compared to other PCB-fabricated PA antennas offering grating-lobe free scanning [22], [23], the PA antenna proposed here has a larger UC footprint thanks to the triangular lattice implementation.

2.4 Conclusion

In this chapter, a low-profile, dual-polarized SAPA antenna for K-/Ka-band SATCOM with a ±60° 2-D scan range was presented. Starting from a dual-

Table 2.1: Comparison of experimentally validated wide-angle scanning dual-band and wideband K-/Ka-band phased arrays with dual polarization. The highlighted columns correspond to PA antennas with both radiators and interconnects realized in PCB.

Ref.		[20]	[21]	[18]	[23]	[22]	This Work
Polarization		Dual linear	Dual linear	Dual linear	Dual circular	Dual linear	Dual linear
Lattice		Rectangular	Triangular	Interleaved	Rectangular	Rectangular	Triangular
UC footprint		$0.25\lambda^2_{\text{high}}$	$0.334\lambda^2_{\text{high}}$	$0.613\lambda^2_{\text{high}}$ (K) $0.307\lambda^2_{\text{high}}$ (Ka)	$0.226\lambda^2_{\text{high}}$	$0.176\lambda^2_{\text{high}}$	$0.241\lambda^2_{\text{high}}$
Element type		Vivaldi	E-dipole	Patch	E-dipole	M/E-dipole	Patch
Manu-facturing		PCB + 3-D printed	PCB + Al. plate	PCB	PCB	PCB	PCB
Feed		PCB + 3-D printed	Plate-mounted coax	PCB	PCB	PCB	PCB
Profile		$1.85\lambda_{\text{high}}$	$0.47\lambda_{\text{high}}$	$0.09\lambda_{\text{high}}$	$0.26\lambda_{\text{high}}$	$0.15\lambda_{\text{high}}$	$0.32\lambda_{\text{high}}$
$f_{\text{high}}/f_{\text{low}}$ (sim.)[2]		1.67:1	3.31:1	1.57:1	1.75:1	1.42:1	1.73:1
Scan B/W (sim.)[1]	Broad-side	18–30 (50%)	13–43 (107%)	19.2–19.8 (3.1%) 28.7–30.2 (5.1%)	17.7–21.2 (18%)* 27.5–31 (12%)*	26–37 (34.9%)	17.9–21.2 (16.9%) 27.5–31 (12%)
	E-60°	18–30 (50%)	7–38 (138%)	N/A[3]	N/A[4]	26–38 (37.5%)	17.9–21.2 (16.9%) 28.1–30.6 (8.5%)
	H-60°	18.5–29.5 (45.8%)	0%	N/A[3]	N/A[4]	26–27.2 (4.5%) 33–37 (11.4%)	17.7–21.2 (18%) 27.5–31 (12%)

[1]in GHz, AVSWR < 2. [2]Defined for AVSWR < 2 at broadside. [3]Not available - radiating grating lobes for 60° scanning beyond 29.2 GHz. [4]Not available - AVSWR versus scan not reported. *Return loss in 1×8 array configuration, for other works infinite array results are reported. E-60° - E-plane, $\theta_s = 60°$, H-60° - H-plane, $\theta_s = 60°$.

band, dual-polarized patch antenna triangular lattice UC, WAIM up to ±60° was achieved with a dielectric sheet above the aperture. Then, the broadband interconnects were integrated so as not to perturb the impedance matching. Measurements of 19-element and 127-element prototypes validated the simulated AVSWR and realized gain performance, respectively.

CHAPTER 3

Measurement setup for PCB-Based Ka-Band Phased Arrays

This chapter presents the design of the cost-effective measurement setup used for the Chapter 2 prototypes. Several array measurement approaches are reviewed, and their scalability and cost shortcomings are identified. Then, the footprint of the connector coaxial-to-microstrip transition is minimized by shaping the connector pad, reducing the number of pad-grounding vias needed and providing increased placement flexibility for connector placement. The resulting transition enables the identical connectorization of all ports of a prototype corresponding to one polarization.

Additionally, miniaturized terminations using SMD resistors are designed by co-simulating transmission lines, grounding vias and resistor parasitic reactances with commercially available resistor models. Several commercially available SMD resistors are evaluated. The evaluation results are exploited in the design of two compact termination solutions. The designed component performance is evaluated with S-parameter measurements of test boards which show repeatable performance.

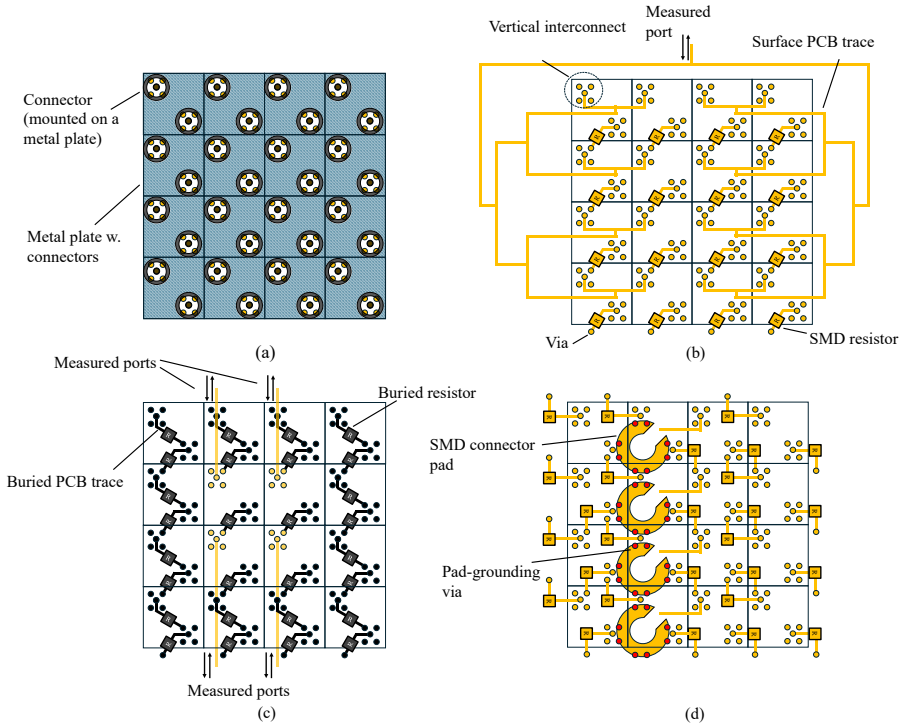


Figure 3.1: Measurement approaches for dual-polarized Ka-band arrays. (a) Full connectorization with a metal plate [21], (b) beamforming network [53], (c) routing to the edge of the board [22], and (d) SMD connectors [54].

3.1 Measurement Approaches

Several approaches have been proposed for connectorizing dual-polarized Ka-band phased arrays as illustrated in Fig. 3.1. One approach [21] uses SMPS connectors integrated in a metal plate (shown in Fig. 3.1(a)). The plate enables tight connector placement without requiring space for individual PCB-connector attachment. As a result, all antenna ports can be connectorized, and mutual coupling, as well as embedded element patterns, can be measured. Unfortunately, the metal plate impedes the characterization of antennas with planar transmission lines on the backplane, such as those used in the UC presented in Chapter 2. Additionally, as explained in Chapter 2, a substantial

number of costly coaxial terminations is required.

To minimize cost, several antenna elements can be measured with a single port, and/or lower-cost terminations can be employed. For example, ports can be excited with a beamforming network (BFN) [53], [Fig.3.1(b)]. However, this approach does not permit measurement of mutual coupling coefficients. Furthermore, the BFN introduces additional reflections that are absent in the active array. Alternatively, a few elements can be individually routed [22] to edge-mount connectors (see Fig. 3.1(c)). However, in this work, the resistively-terminated ports are terminated in an additional, internal layer. This introduces additional effects that are not present in the active array.

Routing to the board's edge is eliminated if SMD connectors are used. SMD connectors are used in [55] to measure an 8×8 single-polarized Ka-band wide-scanning array. However, accommodating the measurement and/or termination of a second polarization is not addressed. An array prototype with SMD connectors is illustrated in Fig. 3.1(d). Unfortunately, it is impossible to connectorize adjacent rows in the same fashion. This rules out recovering the AVSWR performance for the 2-D scanning array. The reason is the SMD connector pad position, which was chosen to enable good all-around grounding using vertical interconnect vias. This is precisely the limitation encountered in several works. In [40], every second element is connectorized. In [54], two prototypes are required to measure transmission with the elements directly adjacent to each other. This approach will become increasingly impractical if coupling to more distant elements is to be measured. In addition, non-identical pad positions can complicate prototype diagnostics and require increased design time. The common cause of the limitations observed in the works mentioned above and Fig. 3.1(d) is a non-scalable approach that does not respect the array's periodicity. The scalability challenges are also present in the measurement approaches shown in Figs. 3.1(b) and (c), where the routing complexity grows with increasing element count, due to the increase in routing junctions and individually routed elements, respectively.

This scalability problem is addressed here. First, the connector pad of a coaxial-to-microstrip transition is placed sufficiently close to the fed port to enable full connectorization of one polarization using SMPM connectors. The key enabler for this is the elimination of a connector pad resonance arising from limited grounding vias by adjusting its shape, thus enabling increased flexibility in connector pad placement. For non-excited ports, two compact termina-

tions are designed and optimized for 50 Ω impedance. The first termination, used in the 19-element prototype of Chapter 2, utilizes a high-performance 50 Ω resistor. In cases where there is more space, a more cost-effective termination using two low-cost 100 Ω resistors can be employed instead. This is the termination mostly employed in the 127-element prototype. The key design feature involves accounting for parasitic reactances by co-simulating the transmission lines, the ground vias, and the resistors using commercial simulation tools.

3.2 SMPM Coaxial-to-Microstrip Transition Design

A fraction of the backplane of the array from Chapter 2 is shown in Fig. 3.2. The PCB substrate between the microstrip layer and the microstrip ground plane, as already mentioned in Chapter 2, is Astra MT77 ($\varepsilon_r = 3$, $\tan\delta = 0.0017$) with a thickness of 0.127 mm. The rectangular UC boundaries are indicated with red dashed lines in Fig. 3.2. The rectangular UC is used instead of the hexagonal one, to accommodate the SMPM connector solely within one UC, as will be shown below. In Fig. 3.2(b), the proposed placement of the coaxial-to-microstrip transition is illustrated. The transition consists of a connector pad and a microstrip line segment, leading to a microstrip line bend. The connector pad shares vias with the vertical interconnects. The bend allows the microstrip line to be routed away from the adjacent vertical interconnect. The microstrip line segment between the connector pad and the bend has a characteristic impedance that differs from 50 Ω for impedance matching. In Fig. 3.2(c), the backplane with the transition and connectors placed is illustrated. The connector with part number $3287 - 6101$ by Amphenol SV Microwave is used. The connector choice was motivated by its tapered shape that minimizes the connector PCB footprint and the availability of vendor-supplied models to simulate the connector and compensate for potential mismatches. The proposed transition and connector placement respect the array periodicity, enabling all ports corresponding to a single polarization to be identically connectorized.

To ensure good impedance matching, the FEM in Ansys HFSS is employed to simulate the proposed transition. For simplicity, the simulations are performed for one connector with the microstrip terminated to a wave port with

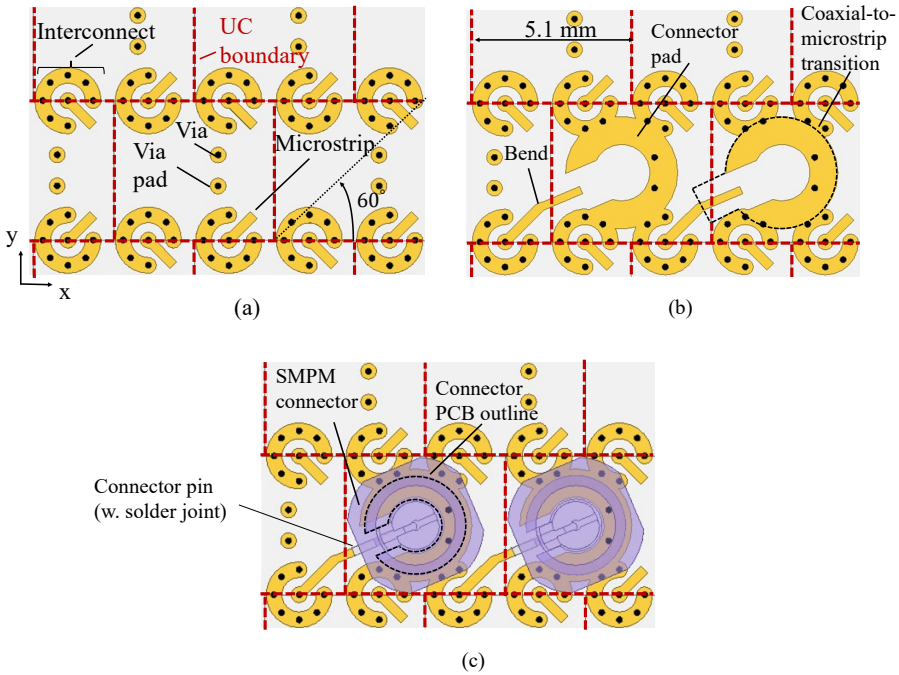


Figure 3.2: Array backplane (a) Without coaxial-to-microstrip transition, (b) with two coaxial-to-microstrip transitions, and (c) with two coaxial-to-microstrip transitions and two connectors.

50 Ω reference impedance. The simulated S-parameters are presented in Fig. 3.3(a). For the initial connector pad (shown in Fig. 3.3(b)), $|S_{11}| < -30$ dB for $f < 29$ GHz. However, an increase of $|S_{11}|$ follows, manifesting in an $|S_{21}|$ dip at 34 GHz. This dip is likely related to resonance in pad areas lacking ground vias. To shift this resonance to higher frequencies, the non-grounded area at the front of the pad is decreased (see Fig. 3.3(c)). The transition then remains resonance-free up to 35 GHz, validating the assumption. The non-grounded edge of this modified connector pad is then chamfered (illustrated in Fig. 3.3(d)), resulting in $|S_{11}| < -30$ dB for $f < 31$ GHz. Shaping the connector pad extends the usable frequency range of the connector without requiring additional vias or increasing the transition footprint. Additionally, the transition does not interfere with the non-connectorized port, which can

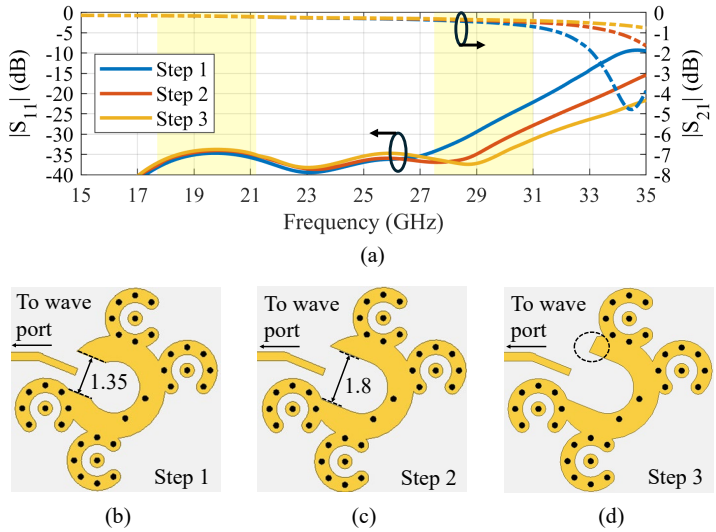


Figure 3.3: Coaxial-to-microstrip transition design. (a) Simulated S-parameters. The shaded regions correspond to the K-/Ka- SATCOM bands. (b) connector pad, step 1, (c) connector pad, step 2, and (d) connector pad, step 3. Unit for (b)-(d): mm.

be terminated with SMD terminations.

3.3 Resistive Termination Design

Several SMD resistors are evaluated for impedance matching to 50 Ω using their equivalent models. They are evaluated using equivalent models included in the Modelithics library [56], version 23.1, in Keysight ADS. These equivalent models are measurement-validated, apply to microstrip line connections and account for the parasitic reactances of the mounting pads. To simplify the resistor selection process, the parasitic reactances related to termination routing, namely, the transmission line discontinuities and via connections to ground are neglected for now. The evaluated resistors are presented in Table 3.1. They satisfy the following criteria i) off-the-shelf availability at Digikey, ii) equivalent models valid $\geq$ 30 GHz, and iii) component size equal to 0402 or smaller (approximately 1 mm $\times$ 0.5 mm).

Table 3.1: Evaluated SMD Resistors

Label	Model	Manufacturer	Size (in)	Type	Price (€)[1]
FC	FC	Vishay	0402	F	143
FCHP1	FCHP	Vishay	0402	W	111
FCHP2	FCHP	Vishay	0402	F	104
MCS	MCS 0402	Vishay	0402	W	2
UBR	UBR0402	KYOCERA AVX	0402	N/A	180
CH04	CH0402	Vishay	0402	F	265
CH02	CH02016	Vishay	02016	F	290
CRCW	CRCW01005 e3	Vishay	01005	W	4
RC	RC0100	YAGEO	01005	W	3

[1]Price per 100 resistors at Digikey (October 2025). W = Wraparound, F = Flip-chip, N/A = Not Available.

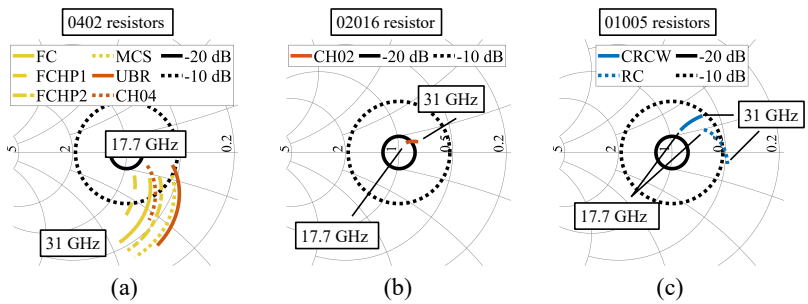


Figure 3.4: S_{11} of SMD resistors with equivalent circuits with 50 Ω nominal value for 50 Ω reference impedance. (a) 0402-size resistors, (b) 02016-size resistor, and (c) 01005-size resistors.

Fig. 3.4 presents the simulated results. All 0402-size SMD resistors exhibit a capacitive shift of the S_{11} loci with increasing frequency, with $|S_{11}| > -10$ dB at 31 GHz (see Fig. 3.4(a)). The 02016-size resistor $|S_{11}|$ remains well below -10 dB and is almost stable over frequency, as shown in Fig. 3.4(b). This can be attributed to device dimensions that are half that of the 0402-size resistors

combined with the flip-chip construction. This high-frequency resistor has been employed for terminations in the Ka- and V-bands [57], [58] without remarks on its performance. However, as presented in Table 3.1, this is the most expensive resistor evaluated. Finally, the simulated S_{11} of the 01005-size resistors is depicted in Fig. 3.5(c). For both 01005-size resistors $|S_{11}| \approx -10$ dB or less. This $|S_{11}|$ response indicates that the 01005-size resistor is a promising alternative for a small-footprint, low-reflection ($|S_{11}| < -10$ dB) termination that is substantially cheaper than a termination with the 02016-size resistor.

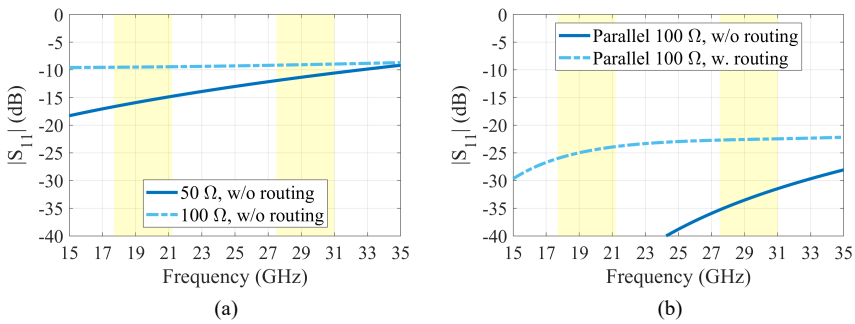


Figure 3.5: Simulated $|S_{11}|$ of terminations employing CRCW resistors. (a) 50 Ω and 100 Ω resistors without parasitic reactances due to routing. (b) Two 100 Ω resistors in parallel with and without parasitic reactances due to routing.

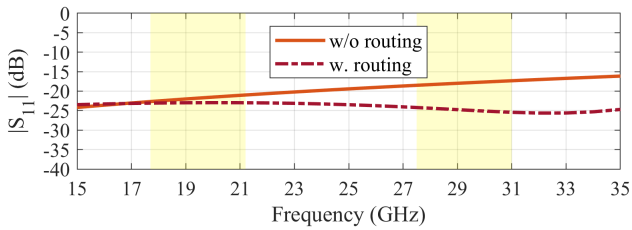


Figure 3.6: Simulated $|S_{11}|$ of terminations employing CH02016 resistor with and without parasitic reactances due to routing.

Since parasitic reactances depend on the nominal resistance value, we vary the nominal resistance value of the 01005-size CRCW resistor. The result is

illustrated in Fig. 3.5(a). The 100 Ω resistor $|S_{11}|$ is almost that of an ideal 100 Ω impedance. Therefore, two parallel 100 Ω resistors will result in a termination well-matched to 50 Ω, as shown in Fig. 3.5(b). At this point, the effect of parasitic reactances is introduced by simulating the transmission lines, the resistor junction, and the ground vias using the FEM in Keysight ADS. The parasitic reactances increase termination $|S_{11}|$, but it remains < -20 dB up to 31 GHz [Fig. 3.5(b)]. The termination compactness is maintained by grounding the resistors on the vias of the terminated interconnect. To facilitate impedance matching, the microstrip junction between the two resistors has a greater than 50 Ω characteristic impedance. Similarly, the CH02016 resistor is employed in a termination that occupies only one interconnect side, with the termination's $|S_{11}|$ illustrated in Fig. 3.6. This termination uses a single 50 Ω resistor due to the CH02016 resistor's cost.

3.4 Test Board Measurements

To experimentally validate the designed components, several test boards have been manufactured and measured using a VNA. The test boards are pictured in Fig. 3.7. To avoid damage to the test boards from the cables connected to the VNA, thinner, flexible cables are used. Rosenberger's 18CK010-150 calibration kit allows the reference plane to be shifted to the SMPM interface of the flexible cables. The measurement setup is shown in Fig. 3.8(a).

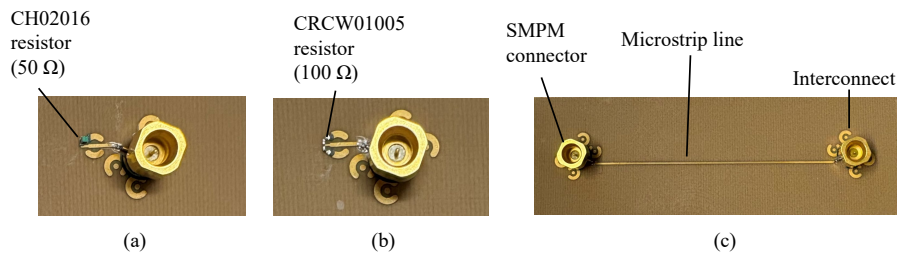


Figure 3.7: Termination and connector transition test boards. (a) SMPM connector-to-01005 resistor termination, (b) SMPM connector-to-02016 resistor termination, and (c) SMPM connectors in back-to-back configuration.

Fig. 3.8(b) presents measurement results of two test boards (labeled SMPM-

1 and SMPM-2) and Ansys HFSS simulations of the coaxial-to-microstrip transition in a back-to-back configuration [Fig. 3.7(c)]. Measured and simulated $|S_{21}|$ agree, validating the surface roughness modeling. There is $\approx$ 10 dB increase in measured reflections compared to simulation. Nevertheless, test board measurement results closely match one another, confirming the transition's repeatability. This repeatability indicates that the cause of the discrepancies is identical for the two boards. Potential causes include substrate thickness tolerances ($\pm 10\,\%$) and accuracy limitations of the connector model.

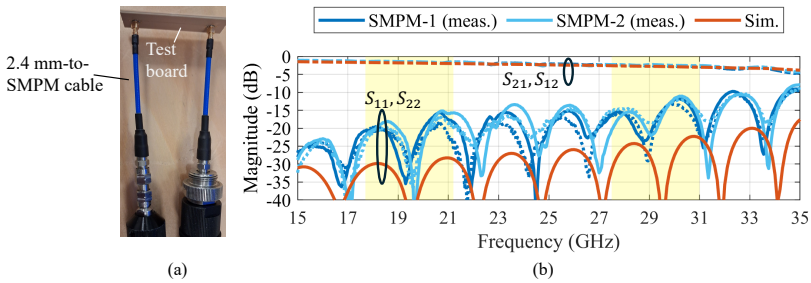


Figure 3.8: Measurement of the test boards with the coaxial-to-microstrip transition in a back-to-back configuration. (a) Photograph of the measurement setup and (b) comparison of simulated and measured S-parameters.

The measured and simulated S-parameters of the test boards depicted in Figs. 3.7(a) and (b) are shown in Fig. 3.9. Because the connector and terminations were designed in HFSS and ADS respectively, each termination is cascaded with the connector mounted at the transition using Ansys Circuit. Good agreement with the simulations is achieved $\leq$ 26 GHz when $|S_{11}| \geq -20$ dB. However, simulation and measurements diverge at higher frequencies, as expected from the back-to-back test board results.

3.5 Conclusion

In this chapter, we presented a scalable measurement setup with surface-mount connectors and resistors suitable for PCB-based, dual-polarized, wide-scanning phased arrays operating in the Ka-band. A resonance of the coaxial-

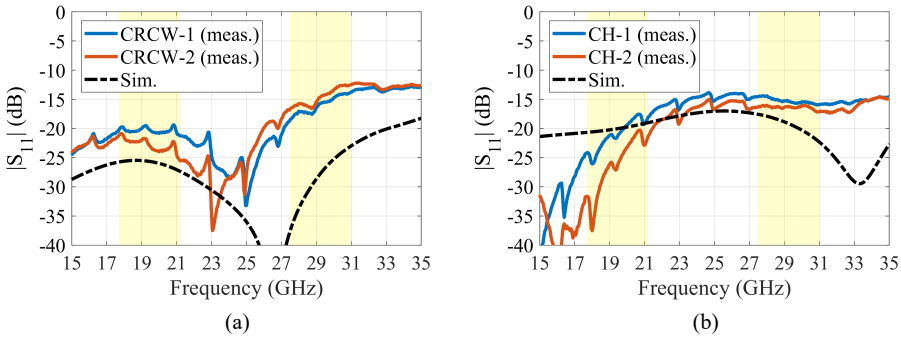


Figure 3.9: Comparison of measured and simulated $|S_{11}|$ of terminations employing (a) CRCW resistors and (b) CH02016 resistors.

to-microstrip transition was mitigated by shaping the connector pad. The resulting transition enables connectorization of all ports of PA prototypes corresponding to one polarization. SMD resistors were evaluated. Then, two terminations with SMD resistors were designed. Test boards employing the designed transition and terminations were fabricated, with their measurement results showing repeatable performance.

CHAPTER 4

Summary of included papers

This chapter provides a summary of the included papers.

4.1 Paper A

Theodoros Pavlidis, Thomas Schäfer, Artem R. Vilenskiy, Lukas Nyström, Ahmed A. Kishk, Marianna V. Ivashina
Low-Profile, K-/Ka-Band ±60° 2-D-Scanning Dual-Polarized Patch Antenna Array on a Triangular Lattice for SATCOM-on-the-Move Applications
Submitted to the IEEE Antennas and Wireless Propagation Letters .

In this paper [59], a low-profile, dual-polarized shared-aperture phased-array antenna operating over 17.9–21.2 GHz and 28.1–30.6 GHz with a 2-D ±60° scan range and Active VSWR < 2 is presented. It targets compact, low-cost, high-performance SOTM user terminals. Such terminals demand wide-scan, DP operation across widely separated K-/Ka-bands and PCB solutions that enable co-location of both the radiating elements and BFICs on a single low-cost board. The proposed design resolves these constraints by

co-integrating a broadband coaxial microstrip-to-stripline interconnect and a WAIM dielectric layer above the aperture, realized with an air gap. The triangular lattice is leveraged to alleviate routing and packaging constraints. Measurements of two prototypes validate the Active VSWR and radiation characteristics, demonstrating a competitive solution for next-generation K-/Ka-band SATCOM arrays.

4.2 Paper B

Theodoros Pavlidis, Thomas Schäfer, Ahmed A. Kishk, Marianna V. Ivashina
Design Challenges and Solutions for Characterizing Mutual Coupling Coefficients in PCB-based Ka-band Dual-polarized Wide-scan Phased Arrays
Accepted in 20th European Conference on Antennas and Propagation .

A scalable measurement setup for PCB-based, wide-scanning phased arrays operating in the SATCOM Ka-band is presented [60]. It addresses the challenges of dense element spacing in dual-polarization configurations as well as the non-ideal performance of commercial SMD resistors at mmWave frequencies. The measurement setup eliminates the need for additional fixtures and/or PCB conductor layers. Test boards for the transition and terminations are fabricated and their S-parameters measured. The measurement results validate the repeatable performance of the designed components. The designed terminations and transition are used in the fabricated phased array prototypes presented in Paper A.

CHAPTER 5

Concluding Remarks and Future Work

This thesis contributes to research on antennas for the next generation of mobile networks by investigating SAPA antennas, along with their prototyping challenges, for the SATCOM K-/Ka-bands. The introduced PA achieves a balanced combination of bandwidth-scan performance, low-profile, and manufacturability, making it well-suited for compact, low-cost, 6G SATCOM user terminals.

Chapter 2 presented a K-/Ka-band dual-polarized, 2-D wide-angle scanning PA with embedded interconnects in a triangular lattice. In Chapter 3, measurement setups for Ka-band PAs were reviewed. Then, a scalable measurement setup based on SMD connectors and resistors was introduced.

Beyond the presently considered K-/Ka-band SATCOM array, one relevant future direction is the extension toward multi-band PAs in FR3. The demonstrated combination of low-profile implementation, dual polarization, wide-angle scanning, and radiator–front-end co-location on a PCB platform is also of interest for compact array solutions operating over multiple bands in the upper microwave and lower mmWave range. In such cases, the triangular lattice remains attractive since it provides a larger unit cell footprint than a rectangular lattice for the same scan volume, which can alleviate routing and

packaging constraints when several bands and integrated functions must be accommodated within one aperture.

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