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PENGPENG SUN • Parameter Extraction and SPICE Modeling of Packaged GaN Power Transistors Using 2-port S-Parameter Characterization • 2026

Parameter Extraction and SPICE Modeling of Packaged GaN Power Transistors Using 2-port S-Parameter Characterization

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DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2026
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THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Parameter Extraction and SPICE Modeling of Packaged GaN Power Transistors Using 2-port S-Parameter Characterization

Pengpeng Sun

Department of Microtechnology and Nanoscience - MC2
Department of Electrical Engineering
Chalmers University of Technology
Gothenburg, Sweden, 2026

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Pengpeng Sun

Technical Report MC2-478
ISSN 1652-0769
This thesis has been prepared using LaTeX.

Chalmers University of Technology
Department of Microtechnology and Nanoscience
Microwave Electronics Laboratory – MEL
Department of Electrical Engineering
Electric Power Engineering
SE-412 96 Göteborg, Sweden
Phone: +46 (0)31 772 1000
www.chalmers.se

Printed by Chalmers Reproservice
Gothenburg, Sweden, April 2026

All models are wrong but some of them are useful. - George E. P. Box

Abstract

This thesis presents a standards-compatible characterization and modeling methodology for a commercial 650 V GaN transistor based on 2-port S-parameter measurements, targeting the accurate extraction of low-nanohenry inductances and picofarad-level capacitances. A systematic comparison with conventional one-port impedance techniques highlights 2-port S-parameters as a broadband and reliable approach for extracting small circuit elements in surface-mounted GaN devices. To ensure accuracy and reliability in the low-value range, a dedicated short–open–load–thru (SOLT) calibration kit has been developed. The design incorporates a short-compensation structure that accounts for via and ground-plane inductance, enabling more reliable de-embedding of fixture residuals. All measured impedance levels are constrained within the 10% accuracy range of the network analysis methods, ensuring traceable and reliable parameter extraction. The extracted parameters extend down to approximately 1 pF for capacitance, 157 pH for inductance, and 32 mΩ for resistance. The extracted inductances, resistances, and nonlinear capacitances are integrated into an industrially recognized physics-based SPICE compact model, establishing a practical workflow from device-level measurement to model implementation without requiring proprietary device information. Cross-domain validation in both frequency and time domains, including S-parameter verification up to 1 GHz and double-pulse test (DPT) up to 400 V, demonstrates close agreement between measurement and simulation in LTspice and Keysight ADS. At higher switching speeds, where parasitic effects dominate circuit behavior, the proposed model adequately predicts the measured ringing and switching waveform, whereas the supplier model exhibits noticeable deviations and excessive oscillations, highlighting the reliability and accuracy of the device parameter extraction. In addition, under identical simulation settings in LTspice and the same operation conditions, the proposed model demonstrates higher computational efficiency compared to the supplier's model, making it suitable for practical circuit-level analysis with reduced simulation cost and improved transparency.

Keywords: GaN, SPICE modeling, S parameters, nonlinear capacitance, parasitic elements, double-pulse test, half-bridge converter.

List of Publications

This thesis is based on the following publications:

[A] **P. Sun, T. Thiringer and C. Fager**, "Procedure for switching loss determination in an oscillatory environment of GaN FETs in a half-bridge connection". Published in 2024 Energy Conversion Congress and Expo Europe (ECCE Europe).

[B] **P. Sun, T. Thiringer, C. Fager, G. Lasser and J. Härsjö** , "Accurate SPICE Model Development for 650V GaN Transistor Using 2-Port S-Parameter Measurements". Published in 2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE US).

[C] **P. Sun, T. Thiringer and A. Logotheti**, "Modeling GaN HEMT Devices: Physical Insights into Intrinsic and Extrinsic Circuit Components of the SPICE model". Accepted in 2026 International Power Electronics Conference, IPEC-Nagasaki 2026 -ECCE Asia.

[D] **P. Sun, T. Thiringer, C. Fager, G. Lasser, J. Härsjö, R. Solano, and A. Logotheti**, "Accurate Extraction of Low-nanohenry and Picofarad Elements in Packaged GaN Power Transistors Using S-Parameter Characterization". Submitted.

Acknowledgments

First of all, I would like to express my sincere gratitude to my main supervisor, Prof. Torbjörn Thiringer and my examiner, Prof. Christian Fager, for their invaluable guidance, patience, and insightful supervision throughout this journey. Without their firm support and encouragement, I would not have come this far.

My deepest gratitude goes to Torbjörn for always believing in me and standing by my side during the most challenging moments. Thank you for fostering a warm and encouraging environment. Your wisdom, kindness, and guidance have profoundly influenced both my personal and professional growth.

Thank my industrial supervisor at Volvo Cars, Dr. Joachim Härsjö, and my co-supervisor, Assistant Prof. Gregor Lasser, for their continuous encouragement, valuable suggestions, and generous assistance throughout this work. I would also like to extend my sincere thanks to my manager, Riccardo Negri, for the feedback and support to help me grow.

Thank my colleagues at E2, MC2, and Volvo Cars for the engaging discussions, teamwork, and supportive atmosphere that made this experience both enjoyable and rewarding. Special thanks to my office mate, Sima Soltanipour, for the countless conversations, encouragement, and memorable moments we shared along the way. Your friendship, companionship, humor, and positive spirit created a welcoming atmosphere that made both work and daily life far more enjoyable. Also, thanks a lot for sharing your templates and codes, which significantly reduced both the time and effort required throughout this work. Many thanks to Adamantia Logotheti, and Ragnar Ferrand-Drake Del Castillo, for dedicating time to answering my questions on the physics of GaN HEMTs. To Stefan Lundberg, I am deeply grateful for your valuable and selfless support with the DPT test setup. To Babak Alikhanzadehalamdari, my sincere thanks for generously sharing your scripts and expertise regarding the test equipment. To Sindhu Kanya Nalini Ramakrishna and Sepideh Amirpour, thanks a lot for your support with writing and formatting, which greatly improved the clarity and presentation of this work. To Rikard Karlsson, thanks for fixing the lab access and training for me. To Rafael Bausone Solano, it is a great pleasure to work with you on the pulse measurements. To Vaishnavi Ravi, thanks for supporting me on the test components and lab equipment.

Also, I want to take this opportunity to thank my colleagues, Araavind,

David, Ruonan, Mebtu, Sankar, Wentao, Qixuan, Meryem, Linhua, Bowen, Luca, Maciej, Meng-Ju, Emma, Evelina, Vineetha, Ritambhara, Moon Moon, Douglas, Eva, Annie, and Elizabeth at E2, Zhiyi, Haojie, Kai-Hsin, Rob, Han, Patrick, Divya, Lucian, Hossein, Tobias, and Debora at MC2, Chi, Ali, Srikanth, Swetcha, Sirini, Dennis, Axel, Ahmed, Krishnan, Olcay, Mert, Cynthia, Fatemeh, and Rajat, at Volvo Cars, for all the friendly interactions, lovely talks, and after-works.

Last but not least, I am deeply and sincerely grateful to my wife, Yiru, whose unwavering love, belief, and encouragement have been my constant source of strength. I would not be where I am today without her. Her support has inspired me to persevere through all the challenges and to grow beyond what I ever thought possible.

Pengpeng Sun
Gotheburg
May 2026

Acronyms

2DEG:	2 Dimensional Electron Gas
AC:	Alternating current
DC:	Direct Current
ASM:	Advanced SPICE Mode
BW:	Bandwidth
CWG:	Coplanar-Waveguide
DC:	Direct Current
DPT:	Double Pulse Test
DUT:	Device Under Test
FET:	Field Effect Transistor
FEM:	Finite Element Analysis
GaN HEMT:	Gallium-Nitride High Electron Mobility Transistor
GCPW:	Grounded Coplanar Waveguide
HV:	High voltage
IF:	Intermediate frequency
LF:	Low Frequency
LV:	Low voltage
MOSFET:	Metal Oxide Semiconductor FET
MVSG-HV:	MIT Virtual Source GaN FET-High Voltage
PCB:	Printed Circuit Board
PDN:	Power Distribution Network

RF:	Radio Frequency
S parameter:	Scattering parameter
SDD2P:	Symbolically Defined 2-port Device
Si:	Silicon
SiC:	Silicon Carbide
SNR:	Signal to noise ratio
SOL:	Short-Open-Load
SOLT:	Short-Open-Load-Thru
SPICE:	Simulation Program With Integrated Circuit Emphasis
TDS:	Time-Domain Reflectometry
TRL:	Thru-Reflect-Line
VNA:	Vector Network Analyzer
WBG:	Wide Bandgap

Mathematical symbols

B_{X}:	Susceptance of object X
C:	Capacitance
C_1:	Parasitic Capacitance of the upper transistor
C_2:	Parasitic Capacitance of the lower transistor
C_{ds}:	Drain-source capacitance
C_{g}:	Gate capacitance
C_{gd}:	Gate-drain capacitance
C_{gs}:	Gate-source capacitance
$C_{\mathrm{g,total}}$:	Total gate capacitance
D:	Dissipation factor
D_{X}:	Current detector
E_{BD}:	Breakdown field
E_{g}:	Bandgap energy
E_{D}:	Forward error terms related to directivity
E'_{D}:	Reverse error terms related to directivity
E_{L}:	Forward error terms related to load match
E'_{L}:	Reverse error terms related to load match
E_{RT}:	Forward error terms related to reflection tracking
E'_{RT}:	Reverse error terms related to reflection tracking
E_{S}:	Forward error terms related to source match
E_{S}':	Reverse error terms related to source match

E_{TT}:	Forward error terms related to transmission tracking
E_{TT}':	Reverse error terms related to transmission tracking
E_{X}:	Forward error terms related to isolation
E'_{X}:	Reverse error terms related to isolation
f_{osc}:	Resonant frequency
G_{X}:	Conductance of object X
I:	Current
I_{ds}:	Voltage controlled drain-source current source
I_{DS}:	Drain-source current source
I_{load}:	Load current
I_{SD}:	Source-drain current source
L:	Inductance
L_{d}:	Parasitic drain inductance
L_{g}:	Parasitic gate inductance
L_{stray}:	Power loop inductance of the PCB
L_{total}:	Total measured inductance
L_{wire}:	Inductance of wire
Q_1:	Quality factor
Q_1:	Upper transistor
Q_2:	Lower transistor
Q_{g}:	Gate capacitance charge
Q_{ds}:	Drain-source Capacitance charge
Q_{gd}:	Gate-drain Capacitance charge

Q_{gs}:	Gate-source Capacitance charge
R_{d}:	Parasitic drain resistance
R_{g}:	Parasitic gate resistance
$R_{\mathrm{ds,on}}$:	On-state resistance
$R_{\mathrm{ds,on1}}$:	Drain-side on-state resistance
$R_{\mathrm{ds,on2}}$:	Source-side on-state resistance
$R_{\mathrm{d,total}}$:	Total drain resistance
R_{on}:	Gate resistance for turn-on
R_{off}:	Gate resistance for turn-off
R_{s}:	Parasitic source resistance
$R_{\mathrm{s,total}}$:	Total source resistance
R_{X}:	Resistance
S_{11}:	Reflection coefficient
S_{12}:	Forward transmission coefficient
S_{12}:	Reverse transmission coefficient
S_{22}:	Reflection coefficient
T_{j}:	Junction temperature
V:	Voltage
ΔV:	Induced voltage by the power loop inductance
V_{1+}:	Incident voltage of port 1
V_{1-}:	Reflected voltage of port 1
V_{2+}:	Incident voltage of port 2
V_{2-}:	Reflected voltage of port 2

v_{s}:	Saturation electron velocity
V_{DC}:	DC-link voltage
V_{DS}:	Drain-source voltage
V_{GS}:	Gate-source voltage
$V_{\mathrm{GS,th}}$:	Threshold gate-source voltage
Z_{X}:	Impedance
Z_{X}:	Impedance of object X
Z_{11}:	Input impedance at port 1 when port 2 is open-circuited
Z_{12}:	Reverse transfer impedance
Z_{12}:	Forward transfer impedance
Z_{11}:	Output impedance at port 2 when port 1 is open-circuited
X_{X}:	Reactance of object X
Y_{X}:	Admittance of object X
Y_{11}:	Input admittance at port 1 when port 2 is short-circuited
Y_{12}:	Reverse transfer admittance
Y_{21}:	Forward transfer admittance
Y_{22}:	Output admittance at port 2 when port 1 is short-circuited
λ:	Thermal conductivity
θ:	Angle of impedance
ω:	Angular frequency

Contents

Part I

Overview

CHAPTER 1

Introduction

1.1 Background

Power semiconductors are a key enabling technology for efficient energy conversion in power electronic systems, as their performance directly determines switching behavior and overall system efficiency. In recent years, wide bandgap (WBG) semiconductor devices, such as Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) FETs, have emerged as leading technologies due to their wide bandgap, high electron saturation velocity, and strong electric-field capability. These superior material properties, summarized in Table 1.1 [1], [2], enable higher efficie ncy, higher switching frequencies, and increased power density.

Compared to conventional silicon (Si) materials, both SiC and GaN exhibit a superior trade-off between on-resistance and breakdown voltage due to their higher breakdown electric field strength, as illustrated in Fig. 1.1. This allows for more compact device structures with reduced conduction losses within the same voltage class. Furthermore, GaN offers further advantages over SiC, including higher saturation velocity, bandgap energy, and critical electric field, making it particularly suitable for high-frequency and high-voltage applica-

Table 1.1: Material Properties

Parameter	Si	4H-SiC	GaN
Bandgap energy E_g (eV)	1.12	3.26	3.39
Electron mobility μ_g ($cm^2/(V{\cdot}s)$	1500	1000	1200
Breakdown field E_{BD} (MV/cm)	0.3	3.0	3.0
Thermal conductivity λ (W/cm·K)	1.5	4.9	2.1
Saturation electron velocity v_s ($\times 10^7$cm/s)	1.0	2	2.5

tions, despite its lower thermal conductivity. In addition, the use of GaN-on-Si technology enables reduced fabrication costs by leveraging standard silicon manufacturing processes, making GaN devices cost-effective for comparable performance [3], [4], [5], [6], [7], [8].

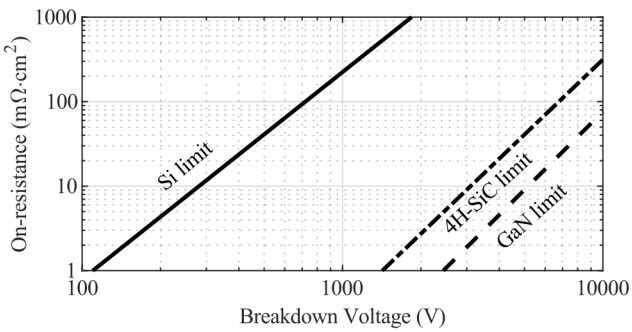

Figure 1.1: Theoretical on-resistance of different materials in relation to blocking capability [2], [6], [7], [8], [9].

Currently, GaN power devices are predominantly realized as lateral high electron mobility transistors (HEMTs) [2], [6], [10]. As shown in Fig. 3.1, a two-dimensional electron gas (2DEG) is formed at the AlGaN/GaN heterointerface, creating a high-mobility channel on the order 1800 $cm^2/(V{\cdot}s)$ [11]. Together with the large saturation velocity, this significantly reduces device resistivity and enhances switching performance [3]. In addition, the absence of a p-n body diode eliminates reverse recovery losses [3], [4]. Even though the lack of a p–n junction also implies limited avalanche capability, GaN devices exhibit superior transient overvoltage capability, enabling GaN FETs to with-

stand surge events without avalanche breakdown [12]. To summarize, GaN as a material provides a wide bandgap, a high breakdown electric field, and a high electron saturation velocity. Meanwhile, the 2DEG at the heterostructure interface enables a high sheet carrier density without doping through spontaneous and piezoelectric polarization, along with a relatively high-mobility channel. As a result, the combination of intrinsic material properties and heterostructure-induced channel characteristics makes GaN HEMTs highly promising for power applications.

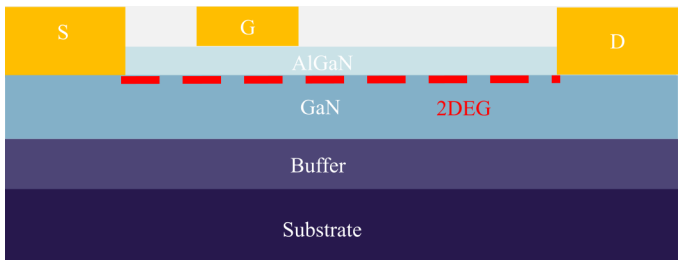

Figure 1.2: Cross-sectional view of a HEMT, illustrating the 2DEG channel formed at the hetero-junction interface.

However, the relatively low gate threshold voltage of enhancement-mode GaN HEMTs (1-2 V) [13], [14], [15], [16], [17] increases their susceptibility to false triggering, particularly under high-speed switching conditions. Furthermore, circuit parasitics can induce voltage ringing and fluctuations at the gate–source and drain–source terminals, potentially leading to unintended switching or device failure. Therefore, accurate GaN FET models are essential to predict device behavior and enable reliable design and optimization of high-voltage, high-speed power electronic systems.
Modeling GaN power transistors requires accurate extraction of capacitances, inductances, and resistances, which is particularly challenging due to their small device dimensions and high switching speeds. For the same voltage rating, GaN devices exhibit an on-state resistance more than five times lower than that of SiC devices [2], [18], [19]. Their compact packaging further results in parasitic inductances as low as 0.1 nH [20], [21], [22], making low-impedance characterization necessary. Industrial measurement approaches therefore extend the characterization bandwidth to several hundred megahertz to resolve such small parasitic elements [20]. In addition, GaN devices can operate at

switching frequencies exceeding 10 MHz, nearly an order of magnitude higher than those typically reported for SiC devices [23], [24], [25], [26]. The associated voltage and current rise and fall times can be shorter than 10 ns, generating harmonics that extend into the several-hundred-megahertz range [27], [28], [29]. Under these conditions, intrinsic capacitances reported in datasheets, which are conventionally measured at 100 kHz or 1 MHz, are insufficient to accurately represent the device behavior during fast switching. Furthermore, the Miller capacitance in GaN devices can fall within the sub-picofarad range, approaching the practical accuracy limits of measurement instruments and making reliable extraction challenging. Higher measurement frequencies help reduce capacitive impedance, increase the measurable current, and improve sensitivity. Measurement frequencies above a few hundred megahertz are also required to capture resonance phenomena and enable accurate separation of capacitive and inductive components. Moreover, the low-nanohenry inductances and picofarad-level capacitances of the device can be strongly influenced by residual parasitics introduced by the measurement setup [30]. Since GaN devices are predominantly surface-mounted and available in diverse package configurations across suppliers, accurate characterization further requires measurement techniques for low-value elements, customized test fixtures, and reliable de-embedding procedures.

1.2 Aim

With the background, this thesis aims to examine existing impedance determination approaches, evaluate their applicability to surface-mounted GaN devices, and propose a suitable method for GaN device parameterization. The key factors include frequency coverage, impedance range, accuracy, connection, and calibration. The reliability and accuracy of the extracted parameters should be validated against the supplier model and experimental results at various operating conditions.

1.3 Previous work

To achieve the above-mentioned goals, an overview of the relevant previous work in the literature is presented in this section.

Impedance parameterization

Electromagnetic and electrostatic simulations have been adopted to estimate the parasitic inductance of packaged cascode GaN transistors [31]. Accurate simulation requires detailed knowledge of internal layout, geometric dimensions, bonding-wire configuration, and material properties, which are typically unavailable for normal users. In addition, simulations are computationally intensive due to fine meshing and accuracy requirements, and convergence is not always guaranteed. Extraction techniques based on switching transients have also been reported, where parasitics are inferred from oscillatory behavior in the time or frequency domain. Time-domain approaches rely on the voltage induced across stray inductance during rapid current transitions (di/dt). To capture fast current transient measurement requires high-bandwidth current sensing and is sensitive to noise and probe limitations [32]. The frequency domain reflects the resonance of the inductance–capacitance network. The oscillation frequency is related to the resonance condition by

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

where L and C are the equivalent inductance and capacitance in the circuit. However, the effective capacitance includes both voltage-dependent intrinsic device capacitances and external parasitic capacitances, which may be of comparable magnitude. A similar ambiguity exists for inductance, where package parasitics and external loop inductances are coupled. Furthermore, when parasitic values fall in the low-nanohenry and picofarad range, bandwidth limitations for voltage probes can restrict the ability to resolve the corresponding high-frequency oscillations.

Conventional capacitance characterization is commonly performed using LCR meters, impedance analyzers, or equivalent functionality integrated in C–V analyzers or curve tracers. Different circuit configurations are typically required to access individual capacitance components when using LCR meters and impedance analyzers. Such reconfiguration increases experimental complexity and introduces additional uncertainty, which becomes significant when measuring capacitances in the picofarad range [30], [33], [34], [35], [36]. Furthermore, due to the dispersion and parasitic components of the selected capacitors for the circuit, the measurable frequency range is limited to a few megahertz [33]. Although the high accuracy and reliability of LCR meters

and impedance analyzers for one-port impedance determination are well documented in [37], [38], [39], [40], one-port measurements can become sensitive to error for semiconductor devices with picofarad capacitances even when the floating terminal is terminated with the guard connection [34], [41], [42]. For C–V analyzers or curve tracers, dedicated test fixtures are generally required for surface-mounted GaN devices [35], [42], [43], [44], and open/short compensation is needed to de-embed fixture residuals. Accurate compensation requires the parasitic impedance of the correction structure to be much smaller than that of the device under test, which becomes increasingly difficult when the target parasitics fall in the low-nanohenry and picofarad range [30], [45]. It is recommended that the residual short impedance remain below 1/100 of the impedance of the target parasitics [30]. Although load and phase compensation can further improve measurement accuracy, implementing such standards in PCB fixtures for surface-mounted GaN devices is practically challenging. In addition, the measurement frequency is typically limited to 1 MHz, as preparing a well-defined reference standard within the actual device characterization environment is difficult [36]. In practice, measurement uncertainty is also influenced by the relative magnitude and ratio among C_{gd}, C_{ds}, and C_{gs}, as noted in the instrument datasheet [46]. When one capacitance is significantly smaller than the others, sensitivity increases and repeatability degrades, which has been observed in picofarad-level measurements.

Time-domain reflectometry (TDR) has also been applied to parasitic extraction using transmission-line theory [47], [48]. This one-port reflection technique does not require prior knowledge of internal geometry or material properties, but commercial TDR systems are typically optimized for a nominal impedance of 50 Ω. Deviations from this reference impedance can introduce mismatch and reduce extraction accuracy.

More recently, S-parameter based techniques have been applied to extract parasitic inductances and capacitances of discrete GaN devices [20], [21], [49], [50], [51], [52], [53], demonstrating the suitability of broadband network measurements for packaged GaN device characterization. In [21], the test fixture is represented using a simplified circuit model, which may not fully capture the complexity of customized measurement setups [30]. As a result, the extracted impedance values can exceed the 10% accuracy limit of the VNA. Other reported approaches [49], [50] do not include explicit fixture calibration, introducing additional uncertainties and systematic errors in the de-embedding

process. In [51], [52], dedicated probe stations are required, which limits applicability to practical device-level measurements. Furthermore, although S-parameter measurements are employed for parameter extraction, the measurement accuracy, necessity, and applicability range are not discussed. Their advantages over conventional impedance measurement techniques, particularly for low-value circuit parameter characterization, are also not explicitly addressed, which weakens the justification of the approach. Consequently, accurate de-embedding and traceable measurement procedures remain critical challenges in GaN power transistor characterization. This gap highlights the need for a repeatable and reliable device-level characterization methodology with a verified accuracy range for low-nanohenry and picofarad-level measurements.

Parameter validation

To verify the accuracy and reliability of the extracted components, they are commonly incorporated into transistor models for circuit-level simulations. Several modeling approaches for GaN devices have been reported in the literature, each offering advantages and limitations as summarized in Table 1.2. The Compact Modeling Council (CMC) has recognized two physics-based compact models for GaN devices: the Advanced SPICE Model for GaN (ASM-GaN) and the MIT Virtual Source GaN HEMT–High Voltage (MVSG-HV) model. The physics-based models provide a physics-based framework and are well-suited for devices where detailed fabrication parameters such as channel dimensions, access region lengths, barrier thickness, and field-plate geometry are available. Although the MVSG-HV compact model has been validated using the EPC2010 GaN transistor in a buck converter configuration [54], its accuracy in reproducing switching transient waveforms has not been validated. The ASM-GaN model [55], [56] is designed to capture both small- and large-signal behavior in RF and power devices. It demonstrates good agreement with measured capacitance–voltage (C–V) and current–voltage (I–V) characteristics for a 650 V cascode GaN FET. Without process and fabrication information, the model's practical applicability for general device modeling and circuit design is limited.
To avoid reliance on detailed device geometry parameters, behavioral models and analytical switching models are developed. Analytical switching models are often developed based on waveforms acquired from specific converter

topologies, such as buck, boost or half-bridge circuits, to describe switching transitions and predict transient waveforms [27], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68]. These approaches partition the switching process into multiple equivalent circuit stages, with state variables obtained by solving stage-dependent differential equations derived from Kirchhoff's laws. The number and structure of stages vary across methods and depend strongly on topology, operating conditions, and parasitic elements. Under high dv/dt and di/dt of GaN devices, oscillatory interactions increase modeling uncertainty and complicate stage partitioning. Moreover, analytic formulations are difficult to integrate directly into circuit simulators [65]. As a result, these models are typically topology-specific and require detailed information of parasitic elements, limiting their general applicability.

Behavioral models are commonly implemented in SPICE simulators using analytical equations or lookup tables to represent nonlinear device characteristics, including I–V and C–V behaviors. Equivalent subcircuits are constructed using controlled sources governed by empirical or physics-based expressions [69], [70], [71], [72], [73], [74], [75]. Empirical models offer implementation simplicity and low computational cost but generally provide lower predictive accuracy than physics-based formulations [76]. Lookup-table approaches require dense measurement data. Insufficient sampling necessitates interpolation or extrapolation, which can degrade accuracy [73]. Prior studies[75] and supplier report [74] document noticeable discrepancies between simulation and experiment. Although improved agreement can be achieved with physical parameters and complex empirical formulations [69], [71], [72], [73], this often increases model complexity and reduces general applicability.

Several behavioral models for GaN devices based on S-parameter extraction and small-signal modeling have been reported in [28], [29], [49], [51], [77], [78]. The Chalmers (Angelov) model introduced in [77] was later adapted in [29], [51] to reduce the number of fitting coefficients, simplify the hyperbolic equations, and describe the third-quadrant characteristic. In [49], parasitic elements are extracted using a small-signal equivalent circuit model and incorporated into supplier models. Another empirical modeling approach based on S-parameter measurements is presented in [28], [78]. This method requires fitting 30 capacitance coefficients and 16 current coefficients, making the modeling process time-consuming and increasing the risk of fitting errors. In addition, capacitance-based formulations of nonlinear capacitances

may introduce convergence issues during circuit simulations. The experimental validation is limited to a 200 V DC-link voltage, while the target device is rated at 650 V, which restricts the model's validity under higher-voltage operating conditions. Furthermore, small-signal modeling is typically implemented in Keysight ADS rather than in a widely compatible SPICE format, limiting their broader applicability for circuit simulation and design.

Table 1.2: Comparison of GaN Power Transistor Modeling Approaches

Model	**Type**	**Accuracy**	**Contributions**	**Limitations**	**Validation**	**Circuit Simulation**
Compact physical model [54], [55], [56]	Device model	Very high	Physics-based and structurally accurate representation; deep insight into device-level physics; high predictive accuracy with complete parameter sets; captures trapping effects	requires proprietary physical parameters (geometry, doping, mobility); high mathematical complexity; heavy computational burden; possible convergence issues in large circuit simulations	Buck converter, fly-back converter	TCAD, Cadence Spectre, Keysight ADS
Behavioral model (lookup table, empirical or semiphysical) [69], [70], [71], [72], [73], [74], [75]	Device model	High	Implementation in SPICE simulators; low computational cost to approximate nonlinear device behavior; compatible with empirical or physics-based formulations	Requires dense datasets for lookup tables; extrapolation can degrade accuracy for lookup tables; a large number of fitting coefficients increases model complexity and reduces efficiency; relies on datasheet information	DPT	LTspice, Pspice
Analytical switching model [27], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67]	Circuit model	modest and acceptable	Provides detailed insight into switching transitions; Useful for loss estimation and transient analysis; captures stage-by-stage switching dynamics	Must have simulated or experimental waveforms before modeling work; requires manual partitioning of the switching process into stages; topology-specific and not easily transferable; requires accurate parasitic parameter estimation; relies on solving differential equations; sensitive to high dv/dt and di/dt oscillations; difficult to implement directly in circuit simulators; not suitable for device-level modeling	Buck converter, DPT	Cadence Spectre, Matlab

To summarize, accurate extraction of GaN FET circuit elements remains challenging due to the extremely small parasitic inductances and intrinsic capacitances involved, as well as the strong influence of test fixture and measurement setup parasitics. Existing approaches often rely on simplified fixture models, incomplete de-embedding procedures, or proprietary device geometry information, which limits their accuracy, reproducibility, and applicability to commercial devices. In addition, the integration of extracted parasitic parameters into industrially recognized physics-based compact models suitable for SPICE simulation remains limited. As a result, a consistent and industrially recognized workflow linking GaN device parameter extraction to model construction is missing.

1.4 Identified research gaps

The following gaps are identified for accurately characterizing and extracting the parameters of surface-mounted GaN power devices based on the review of previous work in Section:

(I) A comprehensive and systematic review of existing impedance determination techniques is lacking. In particular, the selection of S-parameter measurements using a VNA is often not sufficiently justified or critically evaluated for GaN power devices.

(II) The extraction of low-nanohenry inductances, milliohm-level resistances, and pico- to sub-picofarad capacitances remains a significant challenge. Measurement results are highly sensitive to parasitics introduced by test fixtures and setups, which can significantly compromise accuracy and reliability. Existing approaches often rely on simplified fixture models or incomplete de-embedding procedures, leading to extraction errors. Furthermore, some simulation-based methods depend on proprietary device geometry, limiting their applicability to commercially available devices.

(III) The absence of standardized measurement and extraction procedures makes it difficult to reproduce results across different experimental setups and laboratories. Discrepancies observed between literature and datasheet values highlight the need of transparent and reliable GaN power device parameterizations for benchmarking and validation purposes.

(IV) Extracted parasitic parameters are not consistently incorporated into industrially recognized SPICE compact models. Consequently, a unified and industrially compatible workflow linking parameter extraction to validated circuit-level modeling is still missing.

1.5 Contributions

To address these knowledge gaps, this work presents an accurate and standard-compatible approach to extract GaN circuit elements, emphasizing the characterization of small parasitics based on S parameters.The following main contributions are identified:

- A systematic justification of the benefits of using 2-port S-parameter measurements over conventional one-port impedance methods for low-impedance and broadband characterization of surface-mounted GaN devices, which has not been explicitly clarified in prior studies;
- The development of a standards-compatible SOLT calibration kit tailored for surface-mounted GaN transistors, ensuring measurements remain within the 10% accuracy range. A dedicated short-compensation structure is incorporated to improve de-embedding accuracy for very intrinsic and small parasitic elements;
- Integration of the extracted circuit parameters into an industrially recognized physics-based compact model suitable for SPICE simulation, forming an industrially compatible workflow from GaN parameter extraction to model construction;
- Cross-domain experimental validation of the extracted parameters in both time and frequency domains, including double-pulse testing up to 400 V and S-parameter validation up to 1 GHz, demonstrating consistent agreement between measurement and simulation and confirming the reliability of the proposed extraction methodology for small intrinsic and parasitic components in low-nanohenry and picofarad range.

Moreover, this study offers several additional contributions that enhance its practical value and applicability. The nonlinear capacitance, resistance, and inductance are extracted without the need for specialized equipment like curve

tracers, C–V analyzers, or probe stations. The modeling approach is fully independent of proprietary device geometry or process data, making it widely applicable to a broad range of commercial GaN devices. Moreover, a charge-based model is employed to accurately represent nonlinear, voltage-dependent capacitances, thereby ensuring both simulation convergence and physical accuracy. Power loop inductance and parasitic capacitance are characterized with a VNA to make the simulation results reliable.

CHAPTER 2

Impedance Measurement Methodology

This chapter is based on the following article:

- **P. Sun**, T. Thiringer, C. Fager, G. Lasser, J. Härsjö, R. Solano, and A. Logotheti, "Accurate Extraction of Low-nanohenry and Picofarad Elements in Packaged GaN Power Transistors Using S-Parameter Characterization," submitted.

2.1 Overview

This chapter presents an overview of different measurement methods and instruments outlined in Chapter 1.3, aiming to justify the motivation of S-parameter characterization on surface-mounted GaN transistors.

2.2 S parameters

Scattering (S) parameters in the frequency domain describe the relation between the incident and reflected waveforms in networks as presented in Fig. 2.1. The Smith chart is a commonly used tool to visualize S parameters as

demonstrated in Fig. 2.2. S-parameters are often displayed in logarithmic form as $20log_{10}|S|$ in decibels (dB) on VNAs. For passive networks, the absolute values of S parameters are no greater than 1, and thus the corresponding values are negative in dB.

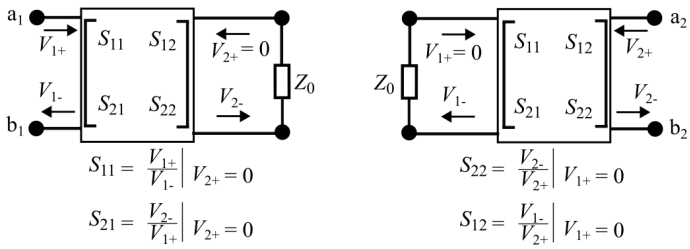

Figure 2.1: S parameters of a 2-port network. S_{11} and S_{22} denote reflections at ports 1 and 2, respectively, while S_{12} and S_{21} represent the reverse transmission and forward transmission, respectively. A more negative S_{11} in dB means less signal is reflected. An S_{21} in dB closer to 0 means more signal passes through.

2.3 Impedance

Impedance is defined in ohms (Ω) as the opposition to the flow of alternating current (AC) presented by the joint effect of resistance and reactance [79] in a circuit. Its complex quantity can be represented in a vector plane as shown in Fig. 2.3. Its inversion is defined as admittance in siemens (S).

2.4 Impedance measurement methods

Precise impedance measurement plays a fundamental role in the development and analysis of passive devices, semiconductors, and power electronic circuits. Accurate characterization of impedance enables reliable evaluation of device behavior, supports high-fidelity circuit simulation, and guides the selection of appropriate components for high-performance designs. Furthermore, accurate impedance characterization requires rigorous fixture compensation and calibration. At high frequencies or low impedance measurement occasions, residual resistance, inductance and capacitance associated with test fixtures

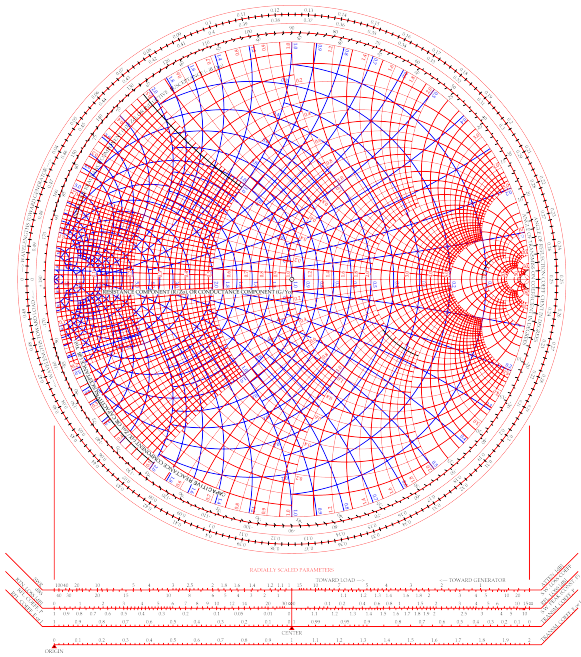

Figure 2.2: Smith chart to visualize S parameters (Color by J. Colvin, University of Florida, 1997).

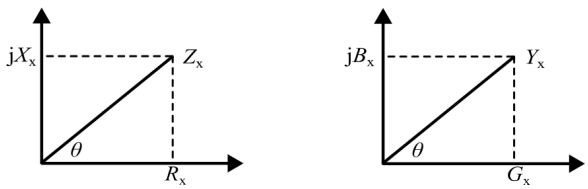

Figure 2.3: Complex quantity of impedance Z_x and admittance Y_x, showing its real and imaginary parts. R_x is resistance, X_x is reactance, G_x is conductance and B_x is susceptance.

or probes can dominate the measured response [30], [80], [81]. Consequently, proper compensation and calibration techniques to de-embed these parasitic effects are as critical as selecting an appropriate measurement instrument. By combining suitable measurement techniques with proper compensation and

calibration, accurate device models can be extracted for simulation, ensuring that power electronic designs are robust and optimized for their actual operating conditions.
Several impedance measurement techniques have been established, each with inherent advantages and limitations in terms of frequency coverage, impedance range, accuracy, test condition, and physical properties of the device under test (DUT).

Bridge method

The bridge method is shown in Fig. 2.4. When no current flows through the detector by adjusting the resistance R_s, the unknown resistance R_x is obtained through the balance equation

$$R_\mathrm{x} = R_\mathrm{s}\frac{R_2}{R_1} \tag{2.1}$$

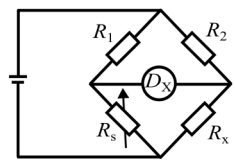

Figure 2.4: Circuit of the resistance bridge or Wheatstone bridge method [82]. D_X is the current detector.

I-V method

A basic circuit for the *I-V* method is shown in Fig. 2.5. The unknown impedance Z_x is calculated from the ratio of measured voltage and current under certain excitations. The voltage across the DUT is measured directly, while the current is obtained indirectly through a precisely known low-value shunt resistor R. The unknown impedance is obtained with the following expression

$$\begin{cases} \bar{I} = \dfrac{\bar{V}_2}{R} \\ \bar{Z}_{\mathrm{x}} = \dfrac{\bar{V}_1}{\bar{I}} \end{cases} \tag{2.2}$$

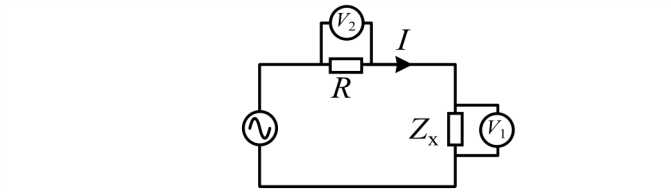

Figure 2.5: Circuit of the I-V impedance method [30].

RF I–V method

The RF *I-V* measurement method follows the same principle as the conventional I–V approach but uses a 50 Ω impedance-matched circuit with a coaxial test port to enable high-frequency operation. Separate measurement configurations are employed for low- and high-impedance DUTs. The impedance is determined from measured voltage and current, where the current is derived from the voltage across a known resistance or, more commonly, a low-loss transformer, which limits the lower frequency range [30], [83].

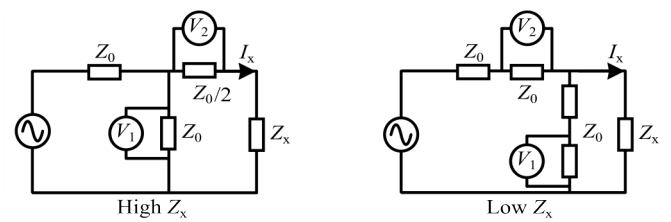

Figure 2.6: Circuit of the RF I-V impedance method with high impedance type on the left and the low impedance type on the right [30], [84]. Z_0 is the 50 Ω characteristic impedance.

Accordingly, the unknown impedance is obtained with the following expression

[30]

$$\begin{cases} \bar{Z}_{\mathrm{x}} = \dfrac{\bar{V}_{\mathrm{x}}}{\bar{I}_{\mathrm{x}}} = \dfrac{Z_0}{2}\left(\dfrac{\bar{V}_1}{\bar{V}_2} - 1\right) \text{ (High } Z_{\mathrm{x}}\text{)} \\ \bar{Z}_{\mathrm{x}} = \dfrac{\bar{V}_{\mathrm{x}}}{\bar{I}_{\mathrm{x}}} = \dfrac{2Z_0}{\dfrac{\bar{V}_2}{\bar{V}_1} - 1} \text{ (Low } Z_{\mathrm{x}}\text{)} \end{cases} \tag{2.3}$$

Auto-balancing bridge method

The auto-balancing bridge method is shown in Fig. 2.7. The current I_{x} and I_{r} are balanced through adjusting the range resistor R_{r}, forming a virtual ground before the amplifier. The unknown impedance is calculated with the following expression[30]

$$\bar{Z}_{\mathrm{x}} = \frac{\bar{V}_{\mathrm{x}}}{\bar{I}_{\mathrm{x}}} = R_{\mathrm{r}}\frac{\bar{V}_{\mathrm{x}}}{\bar{V}_1} \tag{2.4}$$

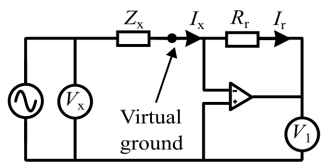

Figure 2.7: Circuit of the auto-balancing bridge method with a simple operational amplifier [30], [83].

Network Analysis Method

The S-parameter measurement methods for impedance analysis are conducted with vector network analyzers (VNAs) in the kilohertz to gigahertz region. It consists of 1-port reflection, 2-port series-thru, and 2-port shunt-thru methods, each of which has a suitable measurement impedance range. The reflection method illustrated in Fig. 2.8 is commonly used to measure impedance from 1 Ω to 2 kΩ with approximately 10% accuracy. The unknown impedance is obtained using the following expression

$$\begin{cases} S_{11} = \dfrac{V_2}{V_1} = \dfrac{Z_\mathrm{x} - 50}{Z_\mathrm{x} - 50} \\ \\ Z_\mathrm{x} = 50\dfrac{1 + S_{11}}{1 - S_{11}} \end{cases} \tag{2.5}$$

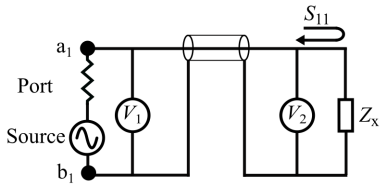

Figure 2.8: Equivalent circuit of 1-port reflection method [83], [84]. The current is limited by the 50 Ω input impedance. V_2 and V_1 are the reflected voltage and incident voltage, respectively. The coaxial connection is shown with a cylindrical symbol.

The 2-port methods are the RF equivalent of the Kelvin technique [80]. The series-through method determines the impedance by connecting the DUT in a transmission–series configuration, as illustrated in Fig. 2.9. Both S_{11} and S_{21} parameters can be utilized to evaluate the impedance using the following expressions.

$$\begin{cases} Z_\mathrm{x} = 100\dfrac{S_{11}}{1 - S_{11}} \\ \\ Z_\mathrm{x} = 100\dfrac{1 - S_{21}}{S_{21}} \end{cases} \tag{2.6}$$

The 10% impedance accuracy range for the S_{21} method is around 5 kΩ to 20 kΩ [83], which makes it suitable for high impedance characterization.
The shunt-through method determines the impedance by placing the DUT in a transmission–shunt configuration, as illustrated in Fig. 2.10. The impedance is subsequently evaluated using the following expression

$$\begin{cases} Z_\mathrm{x} = -25\dfrac{1 + S_{11}}{S_{11}} \\ \\ Z_\mathrm{x} = 25\dfrac{S_{21}}{1 - S_{21}} \end{cases} \tag{2.7}$$

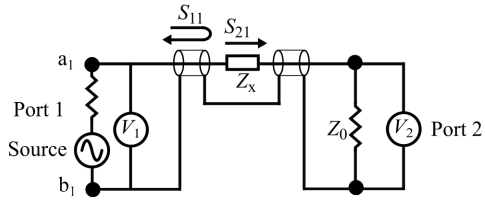

Figure 2.9: Equivalent circuit of 2-port series-thru method [83], [84].

Its 10% impedance accuracy range is around 1 mΩ to 100 Ω, which makes it suitable for low-impedance characterization.

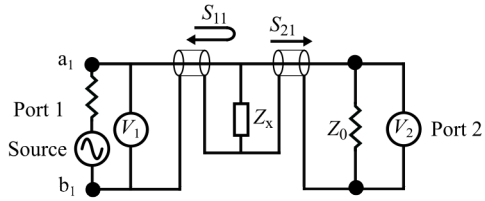

Figure 2.10: Equivalent circuit of 2-port series-thru method [83], [84].

2.5 Calibration

Direct measurement at the instrument terminals is not feasible due to the physical mismatch between the terminals and the device under test (DUT). Therefore, test fixtures and leads are used, introducing parasitic effects such as residual impedance, admittance, and electrical length between the calibration plane and the DUT. These parasitics degrade measurement accuracy and must be compensated.
Common compensation techniques for impedance analyzers and LCR meters include [30]

- **Offset compensation:** corrects measurements by subtracting a known residual component.
- **Open/short compensation:** models fixture residuals using a simple L/R/C/G equivalent circuit illustrated in Fig. 2.11.

- **Open/short/load compensation:** extends the method to complex residual networks, treating the test fixture residuals as a linear four-terminal network represented by ABCD parameters shown in Fig. 2.12.

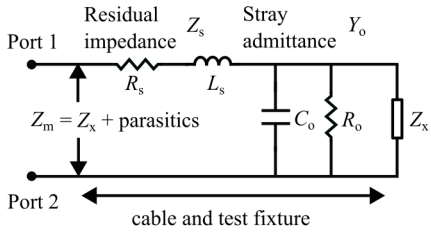

Figure 2.11: Equivalent circuit of open/short compensation method [30]. H_p and L_p denote the high- and low-side potential terminals, respectively. while H_c and L_c represent the high- and low-side current terminals respectively.

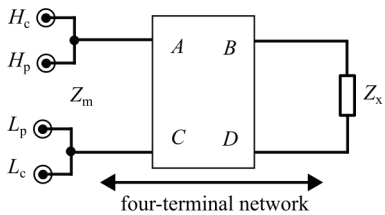

Figure 2.12: Equivalent circuit of Open/short/load compensation compensation method [30].

For VNA calibration, short-open-load-thru (SOLT) is the commonly used method as presented in 2.13.

- **Short (S):** represents a short circuit for reflection measurements
- **Open (O):** represents an open circuit at the reference plane
- **Load (L):** provides a termination equal to the characteristic impedance 50 Ω, minimizing reflections at the reference plane
- **Thru (T):** establishes a direct connection between two ports, serving as a reference for transmission measurements

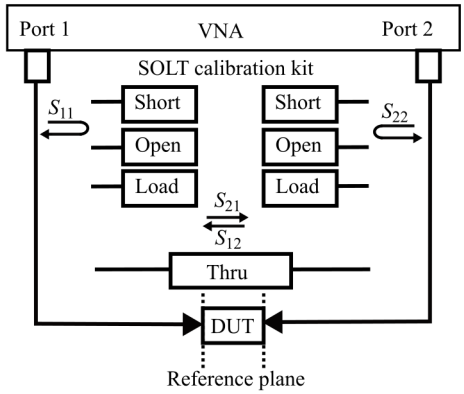

Figure 2.13: Schematic diagram of a 2-port VNA measurement setup, incorporating SOLT calibration standards as described in [83], [85]. This configuration yields the highest accuracy by removing major systematic errors [86].

2.6 Method selection

The impedance measurement techniques are tabulated in Table 2.1. For two-terminal or one-port devices, auto-balancing bridge methods offer the highest accuracy, typically about 0.05%, up to approximately 120 MHz [30]. Radio-frequency (RF) I–V techniques extend the usable frequency range into the gigahertz region with typical accuracy around 1% [30]. For higher frequencies, network analysis is generally preferred, providing broadband characterization comparable to RF I–V techniques when a suitable configuration is selected for the specific measurement range [40]. For three-terminal or 2-port devices such as packaged GaN power transistors, network analysis uniquely enables simultaneous extraction of intrinsic and extrinsic parameters without reconfiguring the measurement setup. In contrast, impedance analyzers require separate connections to measure different parameters, which increases uncertainties and reduces measurement consistency due to the parasitic components and dispersion and of the selected capacitors [36]. From a connectivity perspective, a four-wire configuration provides the highest measurement accuracy. However, since the DUT typically has only one pad per terminal, implementing a true four-wire connection for auto-balancing or I–V measurement methods is generally impractical. An extended shielded two-terminal configuration is

more feasible in practice, but its usable frequency range is typically limited to about a megahertz range due to additional errors introduced by cable extensions. A detailed comparison of commonly used equipment for impedance measurements is summarized in Table 2.2. As can be seen, no single equipment simultaneously incorporates all measurement capabilities and satisfies all requirements. Tradeoffs are needed to select the most appropriate technique for specific applications.

Table 2.1: Comparison of common impedance measurement methods [30]

	Frequency Range	**Advantages**	**Disadvantages**	**Measurement Instrument**	**Common applications**
Bridge method	DC to 300 MHz	High accuracy, Wide frequency coverage by using different types of bridges, Low cost	Needs to be manually balanced, Narrow frequency coverage with a single instrument	LF LCR meter	Generic component measurement
Resonant method	10 kHz to 70 MHz	Good Q accuracy up to high Q	Needs to be tuned to the resonance point, Low impedance measurement accuracy	Q-adapter/Q-Meter	High Q device measurement
Auto-balancing bridge method	20 Hz to 120 MHz	High accuracy and wide impedance measurement range	Limited operating frequency range	LF LCR meter/Impedance analyzer	Grounded device measurement, Generic component measurement
I-V method	10 kHz to 100 MHz	High accuracy, wide impedance range	Limited operating frequency range	LF LCR meter/Impedance analyzer/Frequency response analyzer (FRA)	Floating device measurement, Suitable for probe-type and in-circuit tests
RF I-V method	1 MHz to 3 GHz	High accuracy for RF components	Recalibration required for each modification, Not suitable for LF measurements	RF LCR meter/Impedance analyzer	Grounded RF device measurement, Suitable for probe-type tests
Network analysis method	5 Hz and above	Wide frequency coverage from LF to RF, Different connections to achieve a wide impedance range	Recalibration required for each modification	VNA, Time Domain Reflectometry Analyzer (TDRA)	Generic component measurement, Network analysis for 2-port devices

Based on these considerations, 2-port S-parameter characterization using a VNA is well-suited for broadband GaN device characterization. In this context, S-parameter characterization offers several critical advantages over conventional 1-port impedance measurements. First, unlike terminal voltages and currents, traveling waves remain invariant along low-loss transmission lines, enabling accurate measurements even when fixtures and interconnects separate the device under test from the calibration plane [87]. This is particularly important for packaged low-impedance GaN devices with diverse package styles and unavoidable test fixtures. Accurate de-embedding of fixture and interconnect parasitics is essential and inherently supported by S-parameter measurements. Second, VNAs provide a wide dynamic range, low noise, and wide frequency measurements that allow simultaneous extraction of intrinsic and extrinsic elements from 2-port measurements from the same configuration. This ensures measurement consistency and reduces uncertainty associated with circuit reconfiguration during the whole measurement period. In contrast, this is not achievable with conventional 1-port impedance analyzers, which need different wiring and external circuits to measure different elements. This leads to increased measurement variability and reduced repeatability. Third, GaN transistors exhibit intrinsic capacitances in the picofarad range, parasitic resistance in the milliohm range, and parasitic inductance in the low-nanohenry range. Accurate separation of capacitive and inductive components often requires measurement frequencies exceeding 500 MHz to capture the resonance phenomena [29]. Conventional low-frequency auto-balancing impedance analyzers are typically limited to below 120 MHz, while RF impedance analyzers operate from several megahertz to a few gigahertz [30]. As a result, the characterization of GaN devices requires two impedance analyzers to cover the necessary frequency range as shown in Fig. 2.14. In contrast, a single low-frequency (LF) VNA provides continuous coverage from a few hertz to several gigahertz, enabling unified broadband characterization of GaN devices.

For surface-mounted devices, the measurement accuracy strongly depends on calibration quality, which determines how effectively systematic errors from the instrument, cables, connectors, and test fixtures are removed [89]. Conventional impedance analyzers typically rely on short–open–load (SOL) compensation, which can be augmented with a low-loss capacitor to improve phase accuracy at high frequencies [30]. In contrast, VNAs support a wider range of

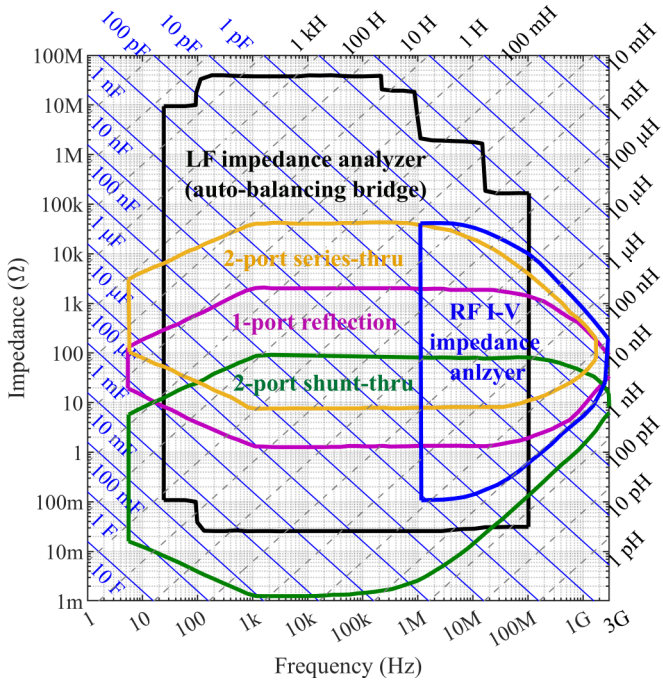

Figure 2.14: Reactance chart for reliable 10% impedance measurement accuracy range of impedance analyzer and VNA methods [37], [39], [40], [88]. It should be noted that the *I-V* method is not discussed since its 10% measurement range is narrower than the auto-balancing bridge method. The 4-wire connection is utilized for impedance analyzer measurements to ensure high accuracy. It is worth noting that the lower-left region is influenced by the use of magnetic cores employed to measure very low impedances at low frequencies, while the lower-right region is affected by approximately 20 pH of residual inductance [83]. The lower-left region can be flattened by adopting proper common mode suppression [81], [88].

vector calibration techniques, including SOL, SOLT, TRL (thru-reflect-line), and related variants [90]. Among these, SOLT calibration is one of the most widely adopted and accurate methods. It compensates dominant systematic error sources through a 12-term error model and enables direct correction of measured S-parameters while preserving consistency between measurement

and modeling domains [30], [86], [91], [92]. After full 2-port calibration, measurement uncertainties below 0.5% have been reported in [91], [92]. Furthermore, prior studies conclude that the impedance uncertainty measured using a SOLT-calibrated VNA is not higher than that obtained with dedicated impedance analyzers [93], further supporting the accuracy of the proposed measurement methodology.
Overall, although 2-port S-parameter measurements with VNAs do not achieve the same absolute accuracy and long-term stability as dedicated impedance analyzers, their superior frequency coverage, calibration flexibility, and measurement consistency allow them to achieve comparable accuracy while providing substantially broader characterization capability for high-voltage power GaN transistors with various packages.

Table 2.2: Comparison between LCR Meter, Impedance Analyzer and VNA

	LF LCR Meter	**Impedance Analyzer**	**LF Vector Network Analyzer**
Main application	LCR component	LCR component, semiconductor, dielectric/magnetic material measurement, power distribution network (PDN)	LCR component, semiconductor, dielectric/magnetic material measurement, power distribution network (PDN)
Measurement Method	I-V/bridge/auto-balancing bridge	I-V/bridge/auto-balancing bridge/RF I-V	Network analysis
Measurement type	1-port	1-port	1-port, 2-port, multi-port
Frequency Sweep	Spot/List/Continuous	Continuous	Continuous
Time Domain Analysis	No	No	Yes (TDR)
Parameters	Z, Y, L, C, R, X, G, B, Q, D, θ	Z, Y, L, C, R, X, G, B, Q, D, θ	S11, S22, S12, S21, Z, Y, θ
Frequency Range	DC to a few tens of MHz	a few Hz to more than 100 MHz (LF), a few MHz to a few GHz (RF)	a few Hz to hundreds of MHz or a few GHz
Display	Numerical/Graphical	Graphical	Graphical
Function	two-element model for LCR component analysis	three- or four-element model for LCR component analysis, possible in-circuit measurements with special adapters	Equivalent circuit analysis, in-circuit measurement
Compensation or Calibration	Short-open	SOL, Low-loss capacitor (LLC)	SOL, SOLT, TRL and more
Test fixture	Not necessary, available if required	Usually required for accurate analysis	Coaxial fixtures required
Connection	4-wire (Kelvin) with one guarding connection	4-wire (Kelvin) with one guarding connection, shielded two-terminal	coaxial 2-wire (1-port measurement), RF equivalent of the Kelvin technique (2-port measurement)
Advantage	Affordable solution, ease of use, high speed	High accuracy over a wide measurement range, resonant analysis, circuit modeling	High-speed measurement over a wide frequency range, resonant analysis, circuit modeling, gain measurements for active devices

CHAPTER 3

Case Study

This chapter is based on the following articles:

- **P. Sun**, T. Thiringer, C. Fager, G. Lasser, J. Härsjö, R. Solano, and A. Logotheti, "Accurate Extraction of Low-nanohenry and Picofarad Elements in Packaged GaN Power Transistors Using S-Parameter Characterization," submitted.
- **P. Sun**, C. Fager, G. Lasser, J. Härsjö, "Accurate SPICE Model Development for 650V GaN Transistor Using 2-Port S-Parameter Measurements". Published in 2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE).

3.1 Overview

The main objective of this thesis is to develop a suitable methodology for extracting low-value circuit parameters in GaN power transistors. An equivalent circuit model of the GaN device is formulated based on its cross-sectional structure. To enable accurate parameter extraction, the design and optimization of appropriate test fixtures are systematically addressed. Furthermore, a

dedicated measurement setup is developed to obtain the S-parameters of the device for subsequent extraction and analysis.

3.2 Equivalent Circuit Model of GaN HEMT

The modeling object in this work is GS66502B (650 V, 7.5 A), which is an enhancement-mode (E-mode) GaN-on-silicon high-electron-mobility transistor (HEMT). A typical cross-sectional view of an E-mode GaN HEMT is shown in Fig. 3.1. The high-mobility two-dimensional electron gas (2DEG) forms at the AlGaN/GaN heterojunction, providing a conductive channel between the source and drain. A p-GaN layer beneath the gate metal creates a Schottky-barrier contact, which, together with the GaN diode between the p-GaN and AlGaN layers, forms a back-to-back diode configuration. This configuration electrically isolates the gate from the channel and enables normally-off operation of the device [94].
To ensure a physically consistent interpretation, the equivalent circuit model in Fig. 3.2 is derived with each element mapped to its physical origin, as illustrated in Fig. 3.1. The equivalent circuit is divided into two parts [95]:

1. The intrinsic device elements, $I_{\mathrm{d}s}$ (voltage-controlled current source), $C_{\mathrm{g}s}$, $C_{\mathrm{g}d}$, $C_{\mathrm{d}s}$ (non-linear capacitance), and $R_{\mathrm{d}s,on}$ (on-state channel resistance), which are functions of the applied bias voltages;

2. The extrinsic parasitic elements, R_{s}, R_{d}, R_{g}, L_{s}, L_{d}, and L_{g}, which are extrinsic parasitic elements due to metal contacts and packaging, and are independent of the bias voltages. It is worth noting that the contact resistance $R_{\mathrm{c},x}$, where $x = s, g, d$, is incorporated into the corresponding parasitic resistances at each terminal.

In this study, trapping effects and dynamic $R_{\mathrm{d}s,on}$ variations are not explicitly modeled. Recent advances in GaN device technology have significantly mitigated trapping-related degradation, with commercial devices typically exhibiting limited dynamic on-resistance variation under practical operating conditions [96], [97], [98], [99]. Reported measurements indicate that dynamic $R_{\mathrm{d}s,on}$ variation in modern devices is generally within 5–9% [97], [98], [99]. In addition, system-level analyses show that even 60% assumed variation has 0.15% impact on the efficiency of an LLC converter [97], indicating

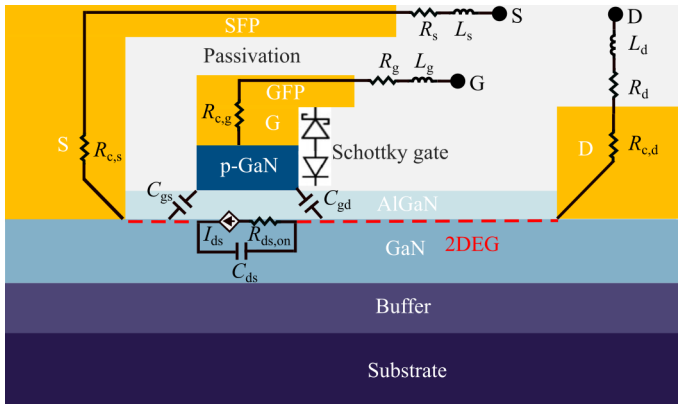

Figure 3.1: Cross-sectional view of a Schottky-gate transistor (SGT) with one gate field plate and one source field plate [54], [94]. Field plates spread the electric field over the channel and increase the breakdown voltage.

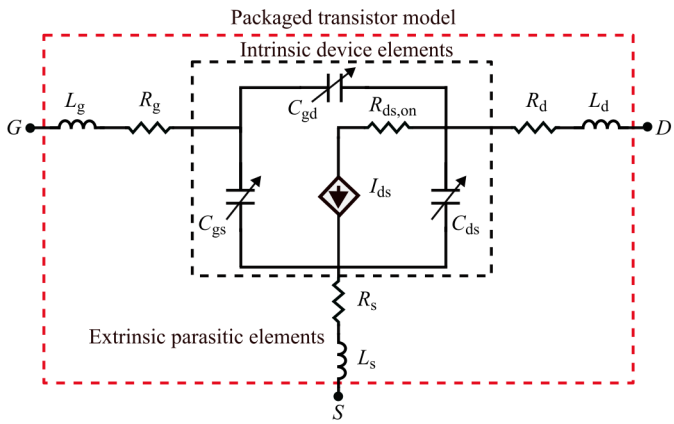

Figure 3.2: Equivalent large-signal circuit model of the selected 650 V GaN HEMT, illustrating the intrinsic device and associated extrinsic parasitic elements.

limited circuit-level impact. Experimental studies further report that the on-resistance of recent GaN devices primarily increases with load current due to self-heating, while trapping-related effects are largely suppressed and only weakly influenced by switching speed or gate resistance [98].

Gate-threshold voltage instability caused by bias stress and trapping typically requires relatively long stress durations to become observable. For example, a stress time of approximately 10 minutes is reported in [100] to produce a measurable threshold-voltage shift, which is significantly longer than the small-signal measurement duration used in this work. In addition, the same tests are repeated with both increasing gate and drain voltage from the lowest voltage to the highest voltage and decreasing the voltage from the highest voltage to the lowest voltage. Identical results are obtained. Therefore, bias-history effects on threshold voltage during the characterization process are expected to be negligible. Furthermore, the influence of threshold-voltage shift on dynamic $R_{\mathrm{D}S(on)}$ can be mitigated by applying sufficiently high gate-drive voltage. For p-GaN devices, this effect becomes negligible when the gate-source voltage exceeds +5 V [100], [101]. In this work, the on-state resistance is evaluated over a gate-source voltage range of +5 V to +7 V, where only minor variation is observed. For validation in the double-pulse test (DPT), a +6 V gate-source voltage is used, further minimizing the influence of trapping-induced dynamic $R_{\mathrm{D}S(on)}$ variation and threshold-voltage shift on the measured switching waveforms [101].
Therefore, under the operating conditions considered in this work, the influence of bias history, measurement sequence, and stabilization time on the extracted small-signal parameters is expected to be limited. Nevertheless, dynamic effects may require dedicated investigation for earlier-generation devices or under extreme stress conditions, such as beyond 100% of the rated voltage.

3.3 Test Fixture Design

In this work, S-parameter measurements are employed to determine the resistance, capacitance, and inductance of packaged GaN transistors. By modeling the device as a 2-port network, these quantities are obtained through the transformation of measured S-parameters into impedance (Z) and admittance (Y) representations. The accuracy of this procedure is fundamentally limited by fixture parasitics and calibration uncertainty, which become increasingly critical as device parasitics approach the low-nanohenry and picofarad range. The achievable accuracy therefore depends on the fidelity of the error model, the quality of calibration standards, and the repeatability of the measurement fix-

tures. For high-frequency GaN characterization, calibration uncertainty can easily dominate the intrinsic device parasitics if the fixture residuals are not effectively removed.

Prior work in [21], [29], [78] introduced a fixture-level equivalent circuit modeling approach for coplanar-waveguide (CWG) measurement fixtures. This method has demonstrated effectiveness at moderate frequencies up to 200 MHz [30]. However, it relies on lumped representations of distributed fixtures and on calibration standards whose impedance may approach the 10% accuracy limits of one-port reflection and 2-port series measurements [80], [83]. The 2-port series–thru technique is generally more suitable for higher-impedance measurements and may be less sensitive when resolving very small parasitic inductances [30], [81], [93]. These factors are particularly relevant for modern surface-mount GaN devices, where parasitic inductances and capacitances are extremely small. In addition, the calibration approach does not explicitly include a thru or load standard. The thru standard establishes the reference connection between ports and improves the determination of insertion loss and phase response, while a load standard with a known impedance (typically 50 Ω) helps reduce instrument- and fixture-related variations, especially at higher frequencies (above approximately 5 MHz) [45]. As a result, the extracted parameters can become influenced by fabrication tolerances, substrate variations, reference-plane uncertainty, and measurement setup effects.

To address these limitations, this work introduces a microstrip-line–based full 2-port SOLT calibration kit shown in Fig. 3.4b that rigorously accounts for fixture parasitic elements and eliminates the need for equivalent fixture circuit modeling [89]. Microstrip-line design has higher stability and less sensitivity to PCB fabrication tolerances, material properties, and mechanical variations, including copper plating thickness, conductor thickness non-uniformity, and dielectric constant (Dk) fluctuations[102], [103]. Compared with the fixture-dependent strategy, the proposed method directly links measurements to standards-based VNA error correction as shown in Fig. 3.3. Each actual S parameter of the intrinsic DUT is a function of all four measured S parameters and twelve error terms, thereby enabling precise de-embedding of test fixture parasitics and reliable extraction of intrinsic device parameters. In addition, the 2-port 12-error correction is performed entirely in the S-parameter domain inside the VNA, preserving numerical stability and ensuring consistent treatment across the full frequency range. By avoiding intermediate S–Z or S–Y

transformations, the method maintains consistency between measurement and modeling domains and reduces numerical sensitivity during parameter extraction.

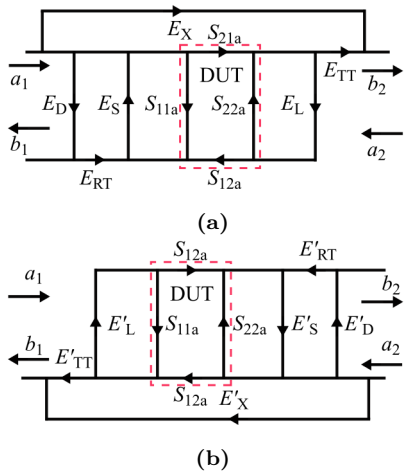

Figure 3.3: Full 2-port 12-term error correction (a) forward-error model; (b) reverse-error model [86], [92]. E_D, E_S, E_{RT}, E_L, E_{TT}, and E_X denote the forward error terms corresponding to directivity, source match, reflection tracking, load match, transmission tracking, and isolation, respectively. The primed quantities E'_D, E'_S, E'_{RT}, E'_L, E'_{TT}, and E'_X represent the corresponding reverse-direction error terms. It should be noted that our kit provides 10 error terms since isolation is neglected for better accuracy [104], [105].

After 2-port calibration, measurement uncertainties below 0.5% are reported in the suppliers' application notes [86], [91]. Measurement uncertainty of inductive impedance using a VNA with SOLT calibration is not higher than that of a dedicated impedance analyzer, which further supports the accuracy of the proposed approach [93].
Moreover, calibration alone is not sufficient to guarantee accurate DUT characterization because the device is measured with the test fixture. Residual impedance associated with vias and ground planes therefore introduces additional measurement error. To mitigate this effect, short compensation is applied as illustrated in Fig. 3.4a. Unlike conventional open/short compensation methods that introduce an external shorting bar [30], the source pad is

directly connected to the transmission line, as shown in Fig. 3.4a. Matching the via and ground-plane geometry to those of the test board ensures consistent de-embedding of parasitic inductance and preserves calibration fidelity.
Regarding the hardware realization, microstrip lines offer a planar structure with simpler fabrication and more predictable dimensional control compared to grounded coplanar waveguide (GCPW) implementations in [106]. Although GCPW can offer lower radiation loss and improved isolation, its implementation on FR4 often requires via-connected ground planes between the top and bottom layers, which increases layout complexity and fabrication sensitivity. To ensure accurate definition of the electrical reference planes, the transmission lines are implemented with sharp-corner geometries rather than curved transitions. In the present work, the drain-side transmission line is connected from the top of the drain pad using a square-ended geometry. This configuration allows the effective transmission-line length to be clearly defined and accurately removed during calibration. In contrast, curved transmission-line implementations may require additional extensions for mechanical routing, making their effective electrical length more difficult to quantify and compensate. The transmission-line dimensions used in the calibration kit and in the device test board are kept identical to ensure consistent and accurate de-embedding. The relative angle between transmission lines does not affect the measurements, since potential crosstalk or signal leakage remains close to the VNA noise floor and is therefore negligible [86], [104]. As a result, the calibration kit is less sensitive to PCB fabrication tolerances and supports stable broadband operation with accurate de-embedding up to 1 GHz. This bandwidth is important for separating low-nanohenry inductive effects from picofarad-level capacitances, which cannot be reliably distinguished at lower frequencies. Consequently, the proposed setup enables broadband, repeatable, and traceable characterization of packaged GaN transistors, providing a reliable foundation for accurate parameter extraction.
A two-layer test board and its corresponding circuit schematic are shown in Fig. 3.5, where the GaN device is positioned to establish a well-defined electrical reference plane. The PCB specifications are summarized in Table 3.1. It is generally recommended that the fixture length does not exceed approximately one-twentieth of the wavelength at the highest measurement frequency when measuring impedances below 0.1 Ω with VNAs [80]. In this work, a transmission-line length of 19 mm is selected, which is slightly above

that guideline because the target impedance range is higher. This choice ensures operation in the gigahertz frequency range, providing adequate measurement margin while reducing the risk of out-of-range impedance conditions that may arise in fixture-dependent approaches, thereby improving measurement robustness and repeatability.

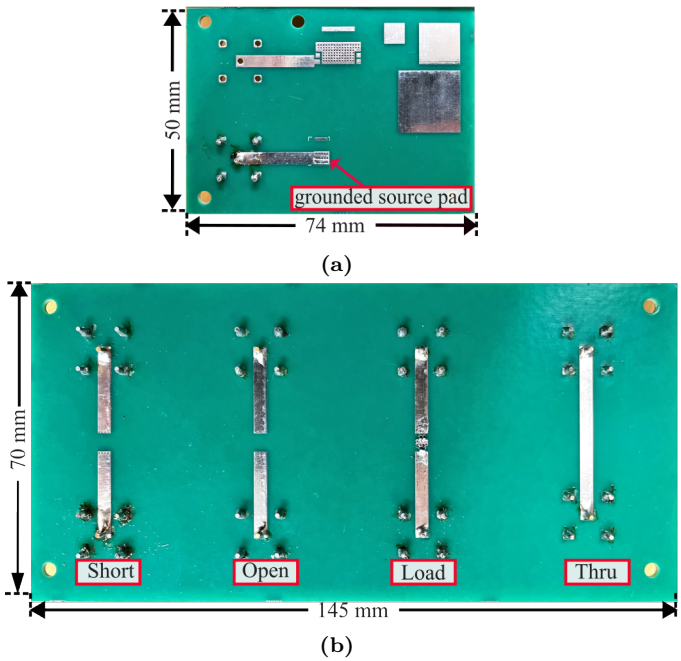

Figure 3.4: (a) Short-circuit compensation with the source pad grounded to the bottom plane; (b) SOLT calibration kit. The 50 Ω load is achieved by paralleling two 100 Ω resistors (package 0402, tolerance 0.1 %).

3.4 Measurement Methodology

An S-parameter measurement setup is constructed as shown in Fig. 3.6, with specifications summarized in Table 3.2. The measurement settings are selected to balance frequency resolution, linearity, and noise performance, ensuring that the extracted parameters are not sensitive to the chosen con-

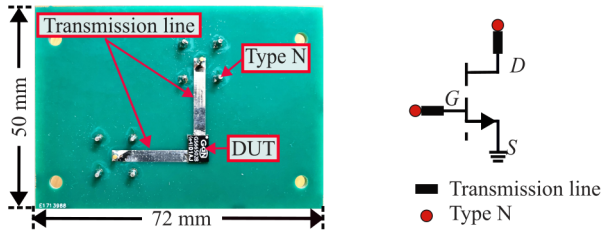

Figure 3.5: Test board with DUT mounted on the top and type N connectors on the bottom. The transmission line is on the top layer, and the ground plane is placed on the bottom.

Table 3.1: Specifications for the PCB

Parameter	Value
Layer	2
Core material	FR4
Dielectric constant Dk	4.5 (assumed)
Thickness	1.6 mm
Transmission line	19 mm × 2.92 mm

ditions. A total of 5001 points provides fine frequency resolution across the sweep range, enabling accurate capture of resonant features while maintaining stability [30]. A 1 kHz intermediate frequency (IF) bandwidth is adopted to reduce trace noise [84]. The source power level is set to −10 dBm, representing a compromise between maintaining receiver linearity and achieving sufficient signal-to-noise ratio (SNR). This level remains below 0 dBm to prevent error amplification of S-parameter errors during conversion to the impedance domain and is consistent with typical low-level semiconductor characterization practice with curve tracers [46]. The frequency range of 100 kHz to 1 GHz provides broadband coverage for low-impedance characterization within the 10% accuracy impedance range of the VNA illustrated in Fig. 2.14.

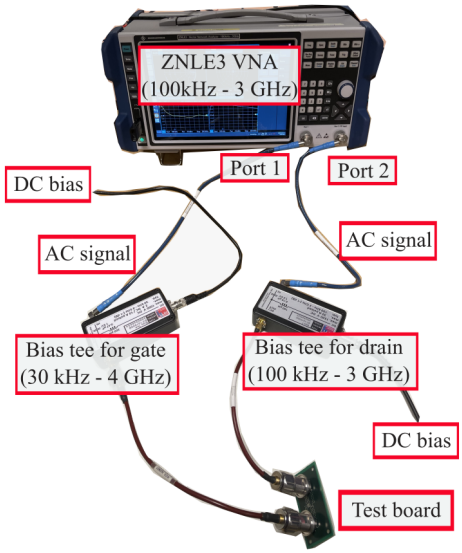

Figure 3.6: Configuration of the experimental setup for 2-port S-parameter measurements, illustrating the VNA, bias tees, coaxial connections, and test board used for device characterization.

Table 3.2: Specifications for S-Parameter Measurements

Parameter	Value
Vector Network Analyzer	2-port R&S ZNLE3
f	100 kHz to 1 GHz
Bias tee	HPPI BT-101000B
Bandwidth	1 kHz
Power level	-10 dBm
Gate voltage	-8 V - 8 V
Drain voltage	0 V - 650 V
Measurement points	5001
Characteristic impedance	50 Ω
Calkit standard	Ideal

CHAPTER 4

Circuit Parameter Extraction

This chapter is based on the following articles:

- **P. Sun**, T. Thiringer, C. Fager, G. Lasser, J. Härsjö, R. Solano, and A. Logotheti, "Accurate Extraction of Low-nanohenry and Picofarad Elements in Packaged GaN Power Transistors Using S-Parameter Characterization," submitted.

- **P. Sun**, C. Fager, G. Lasser, J. Härsjö, "Accurate SPICE Model Development for 650V GaN Transistor Using 2-Port S-Parameter Measurements". Published in 2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE).

4.1 Overview

This chapter demonstrates the detailed extraction process of the key circuit parameters from measured 2-port S parameters and pulse measurements.

4.2 Determination of Nonlinear Capacitance as a Function of Drain-Source Voltage

The nonlinear capacitances, namely C_{gs}, $C_{\mathrm{d}g}$, and C_{ds}, play an important role in switching behaviors and switching losses. Accurate capacitance extraction is crucial for predictive and reliable transistor behavior in modeling. Under off conditions, the equivalent circuit of the transistor can be simplified as shown in Fig. 4.1. For frequencies up to a few tens of megahertz, the impedance of the intrinsic capacitance is expected to be much larger than the impedance of extrinsic resistance and inductance. Therefore, the capacitance can be extracted from the imaginary part of the Y parameters, neglecting resistive and inductive effects. Note that off conditions refer to the condition where the gate-source voltage is lower than the threshold voltage, indicating that the transistor is reverse-biased.

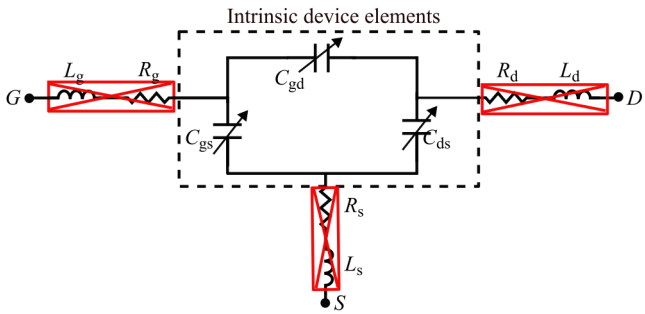

Figure 4.1: Equivalent low-frequency circuit of the transistor in the off state, with extrinsic elements neglected due to their negligible impedance. [107].

Correspondingly, the capacitances can be determined by transforming the measured S parameters into Y parameters, which are related through the

following expressions:

$$\begin{cases} C_{\mathrm{gs}} = \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega} \\ C_{\mathrm{ds}} = \frac{\mathrm{Im}(Y_{22}+Y_{12})}{\omega} \\ C_{\mathrm{gd}} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \\ C_{\mathrm{dg}} = -\frac{\mathrm{Im}(Y_{21})}{\omega} \end{cases} \tag{4.1}$$

where $Y_{12} = Y_{21}$ since the assumed circuit is a passive network. As illustrated in Fig. 4.2, the imaginary components of the Y parameters exhibit a linear dependence on frequency, demonstrating strong agreement with (4.1). The extracted capacitances show a distinct dependence on the drain–source voltage, as presented in Fig. 4.3. As anticipated, both C_{gd} and C_{ds} decrease with increasing $V_{\mathrm{D}S}$, whereas C_{gs} remains relatively constant. Furthermore, the close correspondence between C_{gd} and $C_{\mathrm{d}g}$ validates the accuracy and consistency of the proposed extraction methodology. The extracted capacitances remain stable up to 60 MHz, extending the valid frequency range for accurate parameter determination beyond the 35 MHz limit reported in [106].
Minor fluctuations are observed below 5 MHz, indicating that data from this frequency region can be sensitive to noise because of measurement limitations. As shown in Fig. 4.4, for capacitance around 100 pF measured by 1-port reflection (S_{11}) and 1 pF by 2-port series thru (S_{12}), 5–60 MHz makes sure that the measurements fall into the 10% accuracy range. Correspondingly, the nonlinear capacitance values are determined by averaging the measurement results within the 20–40 MHz frequency range, where the results remain stable and minimally influenced by measurement noise. As shown in Fig. 4.5, the extracted results exhibit strong agreement with the datasheet values, thereby confirming the accuracy and robustness of the proposed extraction methodology. To the best of the authors' knowledge, the observed mismatch of C_{gd} mainly originates from test fixture and connection residuals. When measuring picofarad and sub-picofarad capacitances, fixture and connection parasitics become comparable to the device under test, and conventional open/short compensation is no longer sufficient. Although the measurement instrument specifies high nominal accuracy [46], prior research in [43], [44] shows noticeable discrepancies of measured C_{gd} relative to datasheet values for 650 V GaN devices, indicating practical uncertainties dominated by

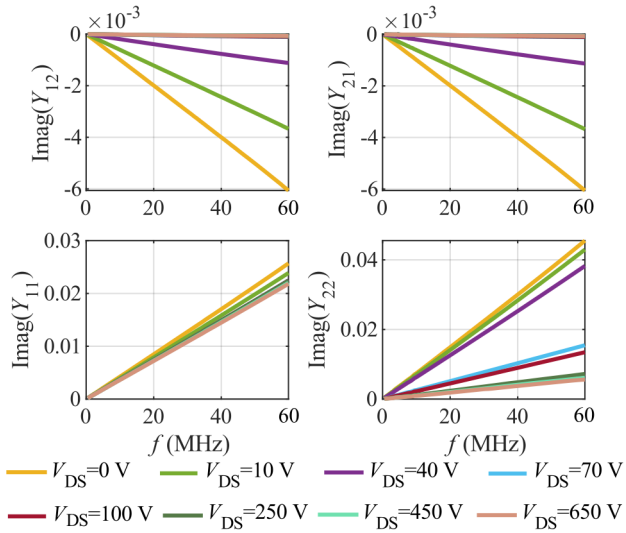

Figure 4.2: Imaginary parts of the measured Y parameters as functions of frequency under $V_{\mathrm{GS}} = 0$ V, with V_{DS} ranging from 0 V to 650 V to analyze the drain-source voltage dependent capacitance behavior.

fixture-dependent residuals. In addition, a capacitance of 0.2 pF lies outside the reliable 10% accuracy range of typical VNAs and impedance analyzers, which inherently introduces measurement uncertainty. This limitation highlights the importance of a repeatable and traceable device-level characterization framework. Since the test methods and conditions used in datasheets are often not fully disclosed, reproducing the same measurement results can be difficult, which may lead to discrepancies between reported values and independently measured results. Without clearly defined reference conditions, the same device may yield slightly different capacitance values when measured using different instruments or fixtures. To reduce such variations and improve measurement consistency, it is beneficial to establish a reference based on precisely known test methodology and setup. In this work, the tailored SOLT calibration kit enables capacitance extraction within a known accuracy range, providing a more reliable foundation for GaN device characterization.
To investigate the capacitance dependency on gate-source voltage at off conditions, the same extraction procedure is performed for $V_{\mathrm{GS}} = -2\ V$ and

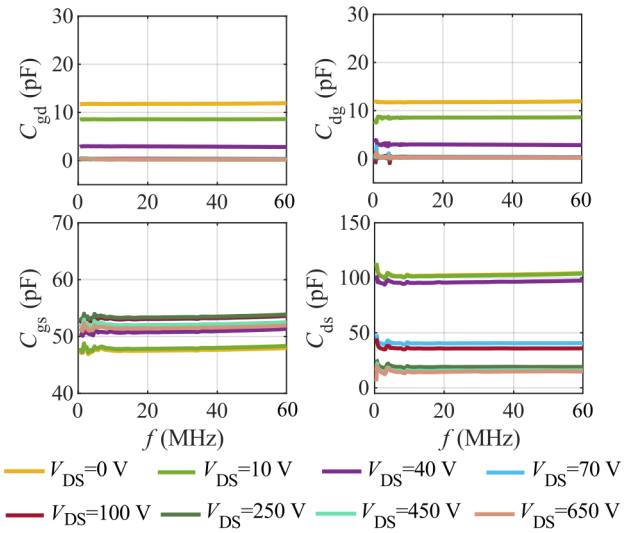

Figure 4.3: Extracted nonlinear capacitances as functions of frequency at V_{GS} = 0 V, with V_{DS} varied from 0 V to 650 V.

$V_{GS} = -4\ V$. The results of this analysis are demonstrated in Fig. 4.6. The capacitance C_{gs} and C_{gd} are observed to slightly vary with V_{GS}, while C_{ds} remains largely unaffected. To gain deeper insight into the dependence, further experiments are conducted and discussed in Section 4.4.

4.3 Determination of Inductance and Resistance

The resistive and inductive elements of the model shown in Fig. 3.2 are extracted using the simplified equivalent circuit detailed in Fig. 4.7. This extraction procedure occurs under on conditions. These conditions are established by applying a gate-source voltage above the threshold voltage to forward-bias the device, while simultaneously maintaining the drain-source voltage at 0 V. This ensures that the transistor operates in its on-state mode, but crucially, without any current conduction. The resulting circuit parameters are subsequently defined using the expressions presented below

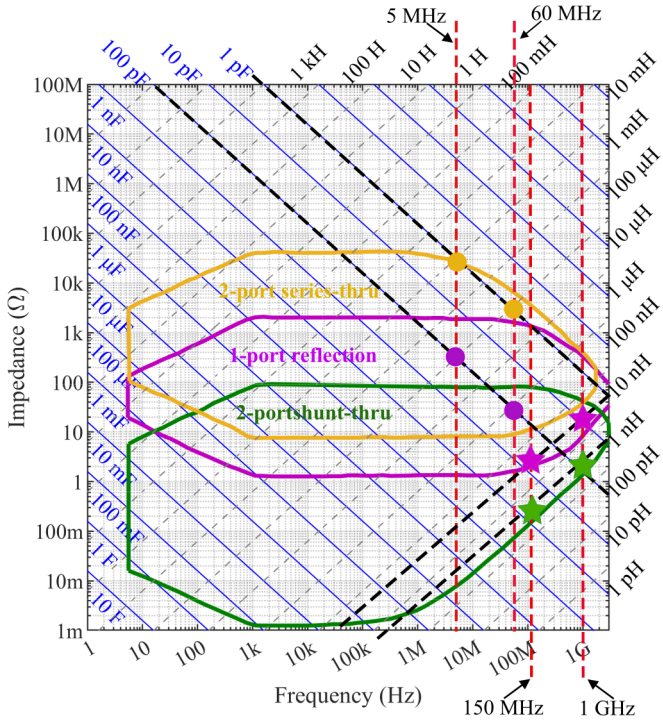

Figure 4.4: Frequency ranges for capacitance (dots) and inductance (stars) measurements within 10% accuracy range, showing the use of two-port series-thru and one-port reflection methods for capacitance extraction, and two-port shunt-thru and one-port reflection methods for inductance extraction.

$$\begin{cases} C_{\mathrm{g}} = C_{\mathrm{gs}} + C_{\mathrm{gd}} \\ R_{\mathrm{ds,on1}} = \frac{C_{\mathrm{gs}}}{C_{\mathrm{gs}}+C_{\mathrm{gd}}} R_{\mathrm{ds,on}} \\ R_{\mathrm{ds,on2}} = \frac{C_{\mathrm{gd}}}{C_{\mathrm{gs}}+C_{\mathrm{gd}}} R_{\mathrm{ds,on}} \end{cases} \tag{4.2}$$

where $R_{\mathrm{ds,on}}$ represents the on-state channel resistance of the device, which is a function of the applied gate-source voltage. It should be mentioned that $R_{\mathrm{ds,on}}$ is considerably smaller than the impedance contributed by the capaci-

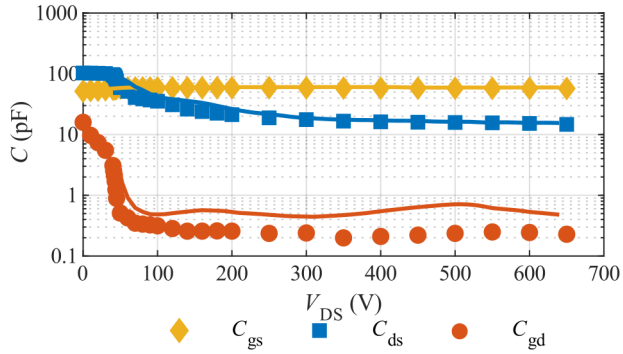

Figure 4.5: Nonlinear capacitances plotted as a function of V_{DS} (shown using dots), exhibiting close agreement with datasheet values (indicated using solid lines).

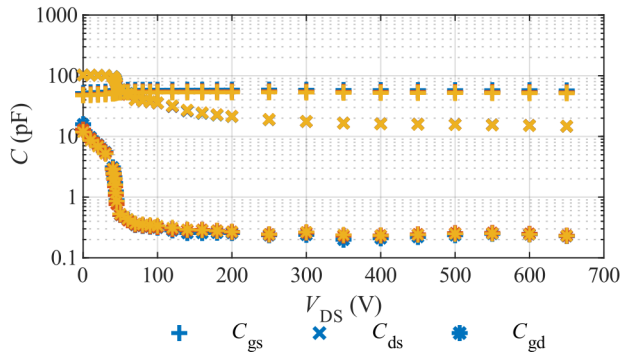

Figure 4.6: Extracted nonlinear capacitance for different gate–source voltages: $V_{\mathrm{GS}} = 0$ V (blue), $V_{\mathrm{GS}} = -2$ V (red), and $V_{\mathrm{GS}} = -4$ V (yellow).

tive elements in low-frequency ranges.
The resistive values are found by examining the real parts of the Z parameters, as shown in the subsequent expressions

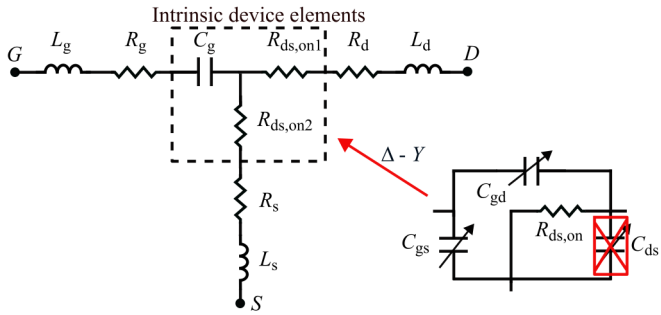

Figure 4.7: An equivalent circuit for on conditions [53]. C_{ds} is negligible since the channel resistance $R_{ds,on1}$ and $R_{ds,on2}$ are much smaller.

$$\begin{cases} R_{s,total} = R_s + R_{ds,on2} = \text{real}\,(Z_{12}) \\ R_g = \text{real}\,(Z_{11} - Z_{12}) \\ R_{d,total} = R_d + R_{ds,on1} = \text{real}\,(Z_{22} - Z_{12}) \end{cases} \tag{4.3}$$

where $Z_{12} = Z_{21}$ since the assumed circuit is a passive network. Consequently, $R_{s,total}$ and $R_{d,total}$ are expected to vary with the gate–source voltage, while R_g remains independent of it. The expected behavior is clearly evident in Fig. 4.8, and the strong agreement obtained enhances confidence in the validity of both the extraction methodology and the measurement results. The observed increase in the resistance can be attributed to two main factors. First, the skin effect becomes prominent at higher frequencies, reducing the effective conduction area of the pads and thereby increasing resistance. Second, the presence of capacitances compromises the validity of the $\Delta - Y$ transformation, which also contributes to the measured frequency-dependent resistance.
For simplicity in the extraction and modeling process, $R_{ds,on}$ is not extracted individually. Alternatively, R_d and R_s are employed to represent the combined resistance at the drain and source terminals, separately. The resistance values shown in Fig. 4.9 are obtained by averaging measurements over the 30 MHz - 40 MHz range for R_d and R_s and over the 60 MHz - 70 MHz range for R_g, to ensure stability and reduce measurement noise. The resistance values extracted from Z_{12} and Z_{21} closely overlap and exhibit nearly identical

magnitudes, confirming the validity of the reciprocal network assumption for the tested GaN device. As the resistance remains essentially constant from $V_{GS} = 5$ V to $V_{GS} = 7$ V, the average of this range is used to determine the final values listed in Table 4.1.

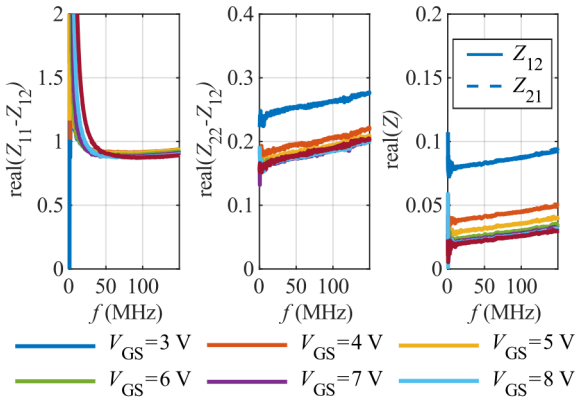

Figure 4.8: Real parts of impedance components versus frequency for different gate-source voltages $V_{GS} \in [3\text{ V}, 8\text{ V}]$. The left and middle plots show $\mathrm{Re}(Z_{11} - Z_{12})$ and $\mathrm{Re}(Z_{22} - Z_{12})$ respectively, highlighting the gate and drain resistance variations across frequency. The right plot compares $\mathrm{real}(Z_{12})$ and $\mathrm{real}(Z_{21})$, confirming the reciprocal nature of the device ($Z_{12} = Z_{21}$).

The inductance values are extracted from the imaginary components of the Z parameters, as expressed in the following equations

$$\begin{cases} L_s = \frac{\mathrm{Im}(Z_{12})}{\omega} \\ L_g = \frac{\mathrm{Im}(Z_{11}-Z_{12})}{\omega} - \frac{1}{\omega C_g} \\ L_d = \frac{\mathrm{Im}(Z_{22}-Z_{12})}{\omega} \end{cases} \tag{4.4}$$

To reduce the effects of the gate capacitance and enhance the accuracy of extraction of L_d and L_g, a scaling factor ω is adopted [78]. Subsequently, the inductance values are determined from the slope coefficients as defined below

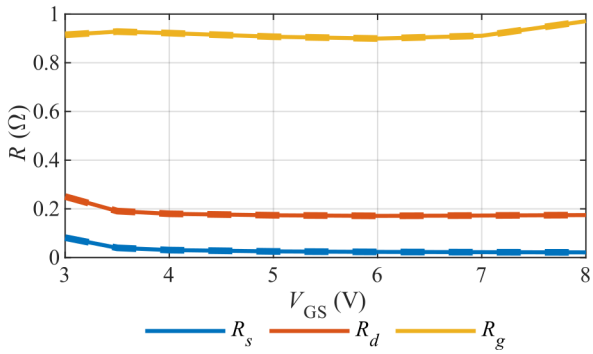

Figure 4.9: Extracted extrinsic resistances as functions of V_{GS}. The values are obtained from measurements under on conditions, showing weak dependence with $V_{\mathrm{GS}} \in [5\ \mathrm{V}, 7\ \mathrm{V}]$. Solid lines are obtained from Z_{12}, and dashed lines are obtained from Z_{21}.

$$\begin{cases} \mathrm{Im}\,(Z_{22} - Z_{12})\,\omega = \omega^2 L_{\mathrm{d}} \\ \mathrm{Im}\,(Z_{11} - Z_{12})\,\omega = \omega^2 L_{\mathrm{g}} - \frac{1}{C_{\mathrm{g}}} \end{cases} \tag{4.5}$$

The experimental results are shown in Fig. 4.10, showing consistent slope coefficients across all Z parameters at various gate-source voltages. This consistency indicates that the inductance is independent of the bias conditions, thereby further supporting the soundness of the proposed extraction methodology. The parasitic inductance associated with the vias and ground plane in Fig. 4.11 shows larger fluctuation at low frequency and increased stability at higher frequency, consistent with theoretical expectations. At frequencies below 500 MHz, the corresponding impedance is less than 1 Ω and therefore lies outside the 10% accuracy region of the one-port reflection method. At higher frequencies, the impedance falls within the valid measurement range and remains stable. Comparable results obtained from both VNA ports confirm consistent calibration and identical measurement conditions. The final inductance value is obtained by averaging the data from 800 MHz to 1 GHz and is subtracted from (4.4) and (4.5) to determine the corrected inductance values.

To obtain the final inductance values, two data points at 150 MHz and 800

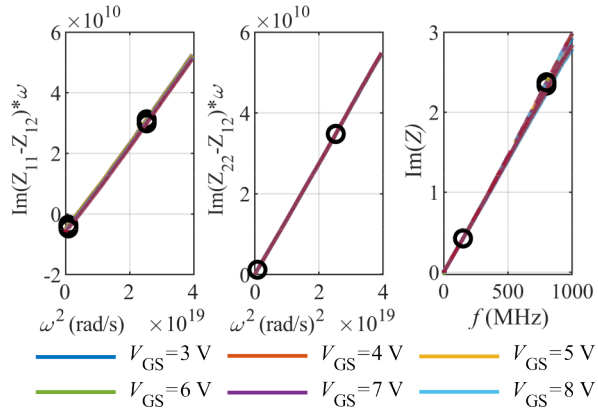

Figure 4.10: Scaled imaginary parts of impedance components versus frequency for $V_{GS} \in [3\text{ V}, 8\text{ V}]$. Measurements span the 100 kHz – 1 GHz range. The selected data points for inductance computation are indicated by black circles, specifically at 150 MHz and 800 MHz.

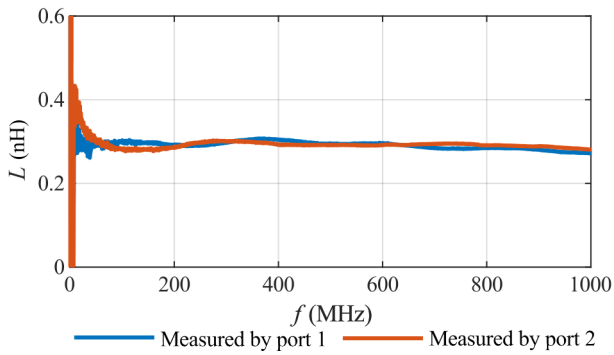

Figure 4.11: Parasitic inductance generated from the source pad vias and the ground plane obtained from the short-circuit compensation measurement. The two ports of the VNA measure the short-circuit compensation board individually.

MHz are selected for the slope calculation because this range ensures measurements within the 10% range as illustrated in Fig. 4.4. The measurement results are shown in Fig. 4.12 and tabulated in Table 4.1. For comparison purposes, the parameter values provided by the supplier's model (a Level 3 model

that includes the package stray inductance) [108] and the reported extraction results from [78] are also listed in the table. Considerable discrepancies are observed from these three sources, indicating that the parameter values can vary considerably across different production batches. Additionally, the supplier's model is designed to represent typical device behavior and may not accurately capture the specific performance of an individual device under all operating conditions. The findings highlight the necessity of obtaining direct measurements on the DUT in order to guarantee accurate modeling and reliable performance assessment.

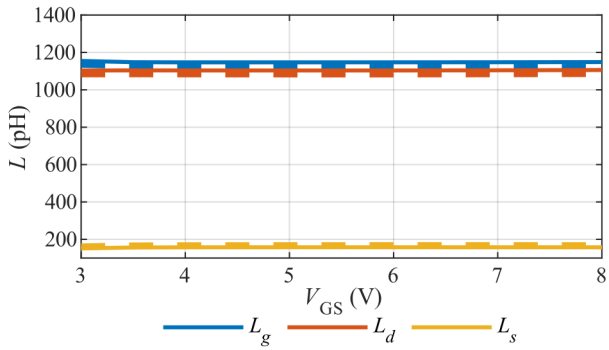

Figure 4.12: Extracted extrinsic inductances plotted as functions of V_{GS}, demonstrating their independence from the bias conditions. Solid lines are obtained from Z_{12}, and dashed lines are obtained from Z_{21}.

Table 4.1: Extracted Inductance And Resistance (25 °C)

Parameter	Extraction	Supplier model	Reference [78]
L_s	157 pH	150 pH	940 pH
L_g	1.147 nH	697.5 pH	560 pH
L_d	1.104 nH	170 pH	1.88 nH
R_s	32 mΩ	10.5 mΩ	14 mΩ
R_g	907 mΩ	225 mΩ	716 mΩ
R_d	181 mΩ	187.5 mΩ	158 mΩ

4.4 Determination of Nonlinear Gate Capacitance as a Function of Gate-source Voltage

When V_{GS} varies, electron accumulation or depletion occurs beneath the gate plates. The associated charge must be supplied during the turn-on process and removed during the turn-off process. This dynamic behavior is governed by the intrinsic gate-related capacitances. Although nonlinear gate capacitances are incorporated in supplier SPICE models [74], [108], their explicit voltage-dependent characteristics with respect to gate–source voltage are not reported in datasheets. In addition, several prior modeling approaches [49], [69], [70], [72], [73], [75] do not explicitly document or extract this voltage dependence, while the work in [57] requires information of the device physical properties, which limits transparency and reproducibility. To ensure accurate modeling of device behavior and reliable prediction of circuit-level performance, the gate-to-channel charge effects must be characterized across the full gate bias range. Due to the symmetric nature of two- dimensional electron gas (2DEG) channel, the channel charge can distribute between drain and source, making it difficult to distinguish and separately extract C_{gs} and C_{gd}. Consequently, C_{g} is used to represent the overall channel charge effects.

At the on state, the gate capacitance can be found by evaluating its value at 0 Hz, as described by (4.5). However, direct capacitance extraction at 0 Hz is impractical, as measurements start at 100 kHz and are susceptible to noise at low frequencies. Therefore, a linear extrapolation technique is employed on the measured data to estimate the capacitance value at 0 Hz. As illustrated in Fig. 4.13, this approach closely aligns with the measurements and provides an accurate estimation of the gate capacitance.

At the off state, gate capacitances are extracted using the methodology described in Section 4.2 and the resulting capacitances in relation to V_{GS} are shown in Fig. 4.14. The measured capacitance includes the fringing capacitance, the overlap capacitance between two metals, which are independent of the gate-source voltage [109]. The extracted gate capacitance exhibits negligible variation when $V_{\mathrm{GS}} < -6$ V, suggesting that the capacitance in this region represents the fringing capacitance and overlap capacitance. Consequently, the final gate capacitance representing the gate-to-channel charge in the channel is obtained by subtracting these parasitic contributions

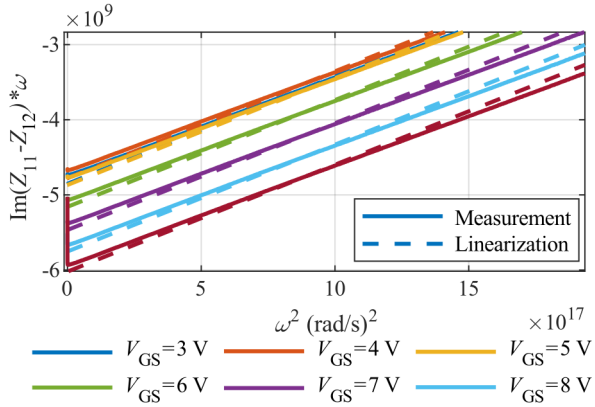

Figure 4.13: Gate capacitance obtained through linear extrapolation as functions of V_{GS}.

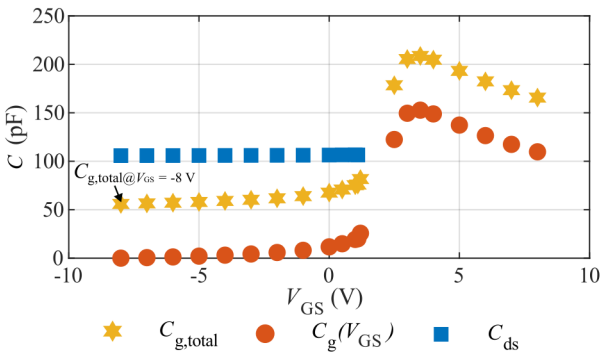

Figure 4.14: Nonlinear capacitances as a function of V_{GS}. The gate capacitance is observed to show strong dependencies on V_{GS} when $V_{\mathrm{GS}} > 0$ V. C_{ds} remains largely unaffected when $V_{\mathrm{GS}} < 0$ V and is not measurable when $V_{\mathrm{GS}} > 0$ V because it is assumed to be negligible compared to $R_{\mathrm{ds,on}}$.

$$C_{\mathrm{g}}(V_{\mathrm{GS}}) = C_{\mathrm{g,total}} - C_{\mathrm{g,total@}\,V_{\mathrm{GS}}=-8\ V} \tag{4.6}$$

The final capacitance values are shown in Fig. 4.14. The capacitance remains negligible under off conditions, increases with channel formation when $V_{\mathrm{GS}} > 0$

V, and decreases gradually at higher gate voltages as a result of gate leakage [110]. The results confirm the gate-voltage dependence and highlight the necessity of incorporating an additional capacitive element in the device model to accurately capture channel charge behavior.

4.5 Gate-to-Source Threshold Voltage Determination

The threshold voltage $V_{GS,th}$ is a key parameter influencing both the static and dynamic behavior of E-mode GaN devices. In this work, the transfer characteristics are characterized using the test setup illustrated in Fig. 4.15. Pulsed I–V measurements are employed to minimize self-heating effects and thermal drift. A sufficiently high V_{DS} is applied to ensure operation in the saturation region. Threshold-voltage instability associated with long-term electrical stress is not considered [100], [111].

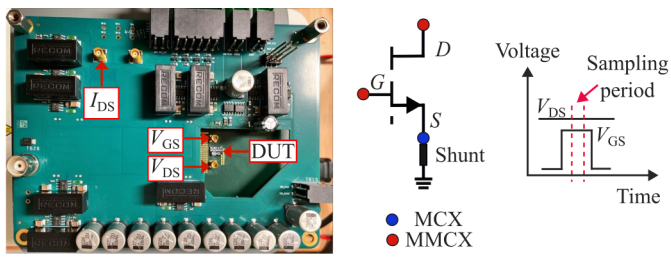

Figure 4.15: Test setup with the schematic for the pulsed I-V measurements. The pulse length is 400 μs with a repetition period of 500 ms.

The measured transfer characteristics are compared with the datasheet in Fig. 4.16. The extracted threshold voltage is approximately 1.6 V, defined at the conduction point of the measurable drain current. This value is supported by the gate-capacitance measurement, which exhibits an abrupt transition at approximately 1.6 V, corresponding to the change from the off state to the on state. Differences between the measured curve and the datasheet plot are observed. This deviation is consistent with device-to-device variation, as the datasheet specifies a $V_{GS,th}$ range of 1.1–2.6 V across production batches.

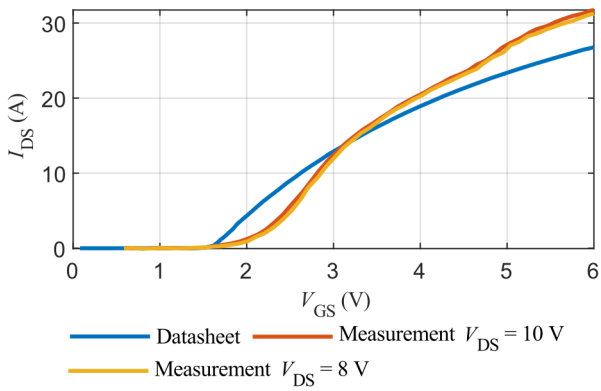

Figure 4.16: Transfer characteristics of the device measured at the saturation condition $V_{DS} > V_{GS}$ - $V_{GS,th}$.

CHAPTER 5

Modeling and Validation

This chapter is based on the following article:

- **P. Sun**, T. Thiringer, C. Fager, G. Lasser, J. Härsjö, R. Solano, and A. Logotheti, "Accurate Extraction of Low-nanohenry and Picofarad Elements in Packaged GaN Power Transistors Using S-Parameter Characterization," submitted.

5.1 Overview

This chapter focuses on modeling of the GaN device using the extracted circuit parameters in Chapter 4 and the verification against S parameters and switching waveforms in the double pulse test (DPT).

5.2 Parameter Fitting and Transistor Modeling

To facilitate continuous and accurate transistor simulations, parameters extracted at discrete measurement points are fitted to smooth analytical expressions. This approach guarantees model accuracy across the full operating

range and allows seamless implementation in circuit simulators like Keysight ADS and LTspice. In this work, analytical equations derived from physics-based models are employed to improve accuracy by imposing physical constraints on the extracted parameters, accounting for both static and dynamic characteristics.
The static characteristics can be described by the following analytical expressions

$$\begin{cases} I_{\mathrm{DS}} = x_2 \ln\left(1 + e^{x_3(V_{\mathrm{GS}} - V_{\mathrm{GS,th}})}\right) \dfrac{V_{\mathrm{DS}}}{1 + max\left(x_0 + x_1 V_{\mathrm{GS}}, 0\right) V_{\mathrm{DS}}}, \\ V_{\mathrm{DS}} > 0 \\ \\ I_{\mathrm{SD}} = y_2 \ln\left(1 + e^{y_3(V_{\mathrm{GD}} - V_{\mathrm{GD,th}})}\right) \dfrac{V_{\mathrm{SD}}}{1 + max\left(y_0 + y_1 V_{\mathrm{GD}}, 0\right) V_{\mathrm{SD}}}, \\ V_{\mathrm{DS}} < 0 \end{cases} \tag{5.1}$$

where x_0, y_0, x_1, y_1, x_2, and y_2 are fitting coefficients. The fundamental form of the expression was initially proposed for E-mode MOSFETs [112] and was subsequently developed further for GaN FETs by the MVSG-HV model [54]. This model exhibits high accuracy in compact device modeling, making it practically useful for both device- and circuit-level simulations. The *max* function guarantees correct operation in both forward conduction mode ($V_{\mathrm{DS}} > 0$) and reverse conduction mode ($V_{\mathrm{DS}} < 0$). The device's static characteristics are obtained from the datasheet and modeled in Keysight ADS with a symbolically defined 2-port device (SDD2P), as illustrated in Fig. 5.1. The fitting results are presented in Fig. 5.2, with the extracted model coefficients listed in Table 5.1. The fitted curves demonstrate excellent agreement with the datasheet, with no noticeable discrepancies observed.
To complement the static characteristic modeling and accurately represent the device's transient behavior, it is also essential to characterize its dynamic characteristics, represented by the nonlinear capacitances. Accordingly, the nonlinear capacitances as a function of the drain-source voltage are described using the charge-based models developed in [54], ensuring consistency with physical behavior and improved convergence in circuit simulations. The expressions are given as follows

$$\begin{cases} Q_{\mathrm{x}}(V_{\mathrm{DS}}) = \int C_{\mathrm{x}}(V_{\mathrm{DS}})dV_{\mathrm{DS}} + r_1 V_{\mathrm{DS}} \\ C_{\mathrm{x}}(V_{\mathrm{DS}}) = \dfrac{s_1 q_1}{1 + e^{q_1(-V_{\mathrm{DS}}+p_1)}} + \dfrac{s_2 q_2}{1 + e^{q_2(-V_{\mathrm{DS}}+p_2)}} \end{cases} \tag{5.2}$$

where x = ds, gs, gd, and s_1, s_2, p_1, p_2, q_1 and q_2 are fitting coefficients. A constant parameter r_1 is introduced to describe a constant capacitance component independent of the drain-source voltage. For the capacitance to gate–source voltage, an empirical expression with a gate-voltage constraint is proposed as follows

$$\begin{cases} Q_{\mathrm{g}}(V_{\mathrm{GS}}) = \int C_{\mathrm{g}}(V_{\mathrm{GS}})dV_{\mathrm{GS}} \\ C_{\mathrm{g}}(V_{\mathrm{GS}}) = s_1 \left(1 - q_1 V_{\mathrm{GS}}\right) \left(\frac{\pi}{2} + \arctan\left(p_1 \left(V_{\mathrm{GS}} - V_{\mathrm{GS,th}}\right)\right)\right) \end{cases} \tag{5.3}$$

It is worth noting that $V_{\mathrm{GS,th}}$ corresponds to the threshold voltage in Table 5.1, ensuring consistency and validity for static and dynamic characteristic modeling. The fitted results are exhibited in Fig. 5.3 - 5.4 and the fitting coefficients are summarized in Table 5.2.

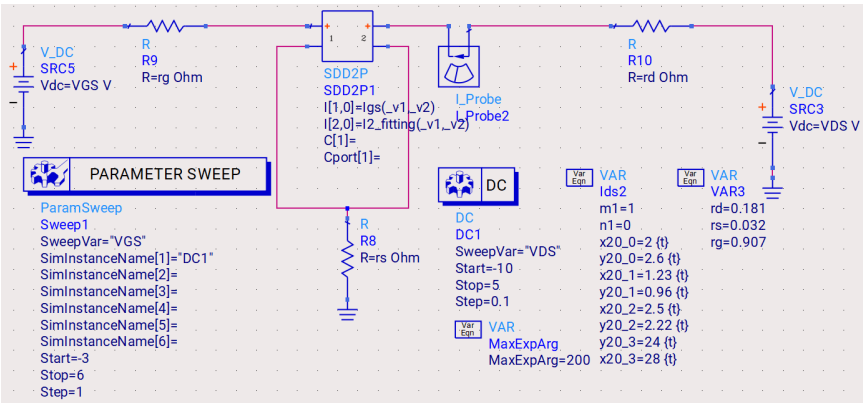

Figure 5.1: Simulation circuit for the static *I-V* curve fitting in ADS. The GaN transistor is represented by an SDD2P.

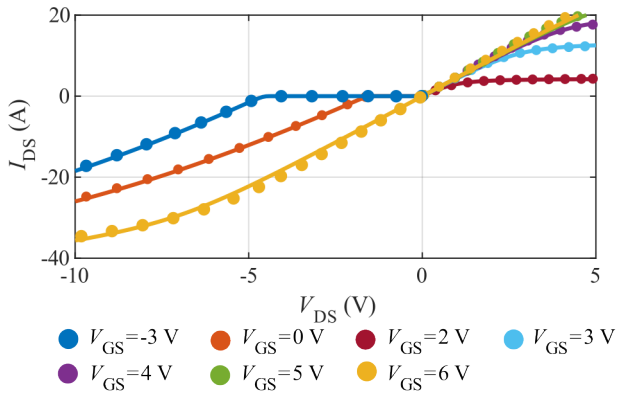

Figure 5.2: Fitted and datasheet-based static characteristics, where solid lines represent the fitted curves and dots denote the datasheet values.

Table 5.1: Model Coefficients for Static Characteristics

x_0	x_1	x_2	x_3	$V_{\mathrm{GS,th}}$
0.45	1.21	10.4	28	1.6
y_0	y_1	y_2	y_3	$V_{\mathrm{GD,th}}$
0.585	0.96	9.9	24	1.6

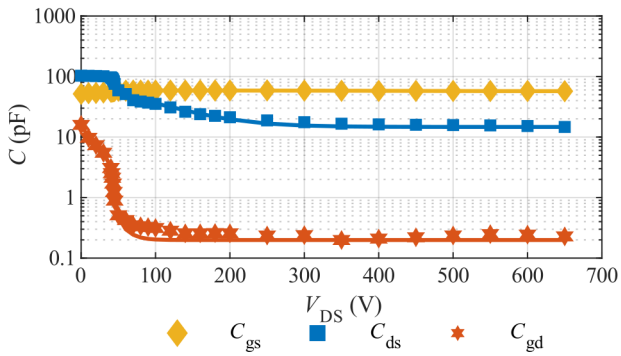

Figure 5.3: Fitted and measured nonlinear capacitances as functions of V_{DS}, where solid lines represent the fitted curves and dots denote the measured data.

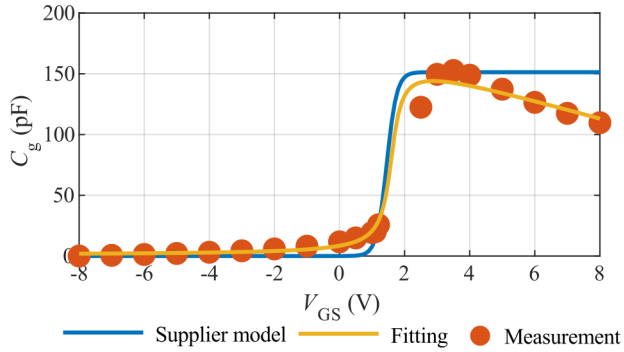

Figure 5.4: Comparison between the fitted curve, measured data, and the supplier's model showing the variation of the nonlinear gate capacitance as functions of V_{GS}.

Table 5.2: Model Coefficients for Dynamic Characteristics

	C_{gs}	C_{gd}	C_{ds}	C_g
s_1	$453.40e^{-12}$	$-12.38e^{-12}$	$-2.77e^{-9}$	$55.74e^{-12}$
p_1	$-1.30e^{4}$	39.38	67.27	4.09
q_1	0.0020	-0.40	-0.022	0.043
s_2	$36.78e^{-12}$	$-733.23e^{-12}$	$-53.42e^{-12}$	
p_2	34.18	-16.68	44.13	
q_2	-0.16	-0.10	-0.78	
r	$57.56e^{-12}$	$0.22e^{-12}$	$15.62e^{-12}$	

5.3 Validation and Performance Evaluation

An LTspice model is built using the parameters extracted from the proposed methodology. Its RF performance is validated through S-parameter comparisons with both experimental measurements and simulation results from the supplier's model. To assess its applicability in power converter applications, the model is further evaluated using DPT simulation and measurement results in a half-bridge configuration.

S Parameters Results

To evaluate the RF performance of the proposed model, two operating points, $V_{GS} = 0$ V, $V_{DS} = 550$ V in the off region and $V_{GS} = +6$ V, $V_{DS} = 0$ V in on region, are selected to match the experimental conditions. The measured S-parameters, along with those from the supplier's model and the proposed model, are compared in Fig. 5.5 - 5.6. For both operating points, the proposed model is closely aligned with the measured data and demonstrates improved agreement compared to the supplier's model. The observed symmetry ($S_{12} = S_{21}$) confirms the device's reciprocal and passive nature with no gain under the experimental conditions, highlighting its operation as a switch in power converter applications rather than as an amplifier in RF applications. It should be noted that the discrepancies between the simulated and measured S_{12} and S_{21} between simulation and measurement results at high frequency are mainly attributed to differences between the actual and extracted values of R_S and L_S. Since these parameters are very small, their accurate determination is inherently challenging.

Double Pulse Test Results

To evaluate the transistor's performance in power converter applications, DPT is commonly employed to analyze switching behaviors and loss characteristics. In this study, a half-bridge converter consisting of a power board and one gate driver board is designed as shown in Figs. 5.7 - 5.9. The power board is designed based on the fluxing canceling configuration to reduce the power loop inductance and optimize the switching performance of the GaN devices [113]. The corresponding DPT setup, as shown in Fig. 5.10, facilitates characterization of the switching performance of the GaN transistor under realistic operating conditions. Accordingly, the performance of the proposed model is validated by comparing its simulation results with the circuit illustrated in Fig. 5.11 and specifications summarized in Table 5.3, against both the measured data from the DPT setup and simulations obtained using the supplier's model. Critical comparison metrics include the gate-source voltage V_{GS}, drain-source voltage V_{DS}, and drain current I_{DS}. Particular attention must be paid to the gate–source voltage of the upper device, since the fast switching speed of WBG transistors can introduce cross-talk between phase-leg devices. This coupling may induce unintended turn-on of the upper device

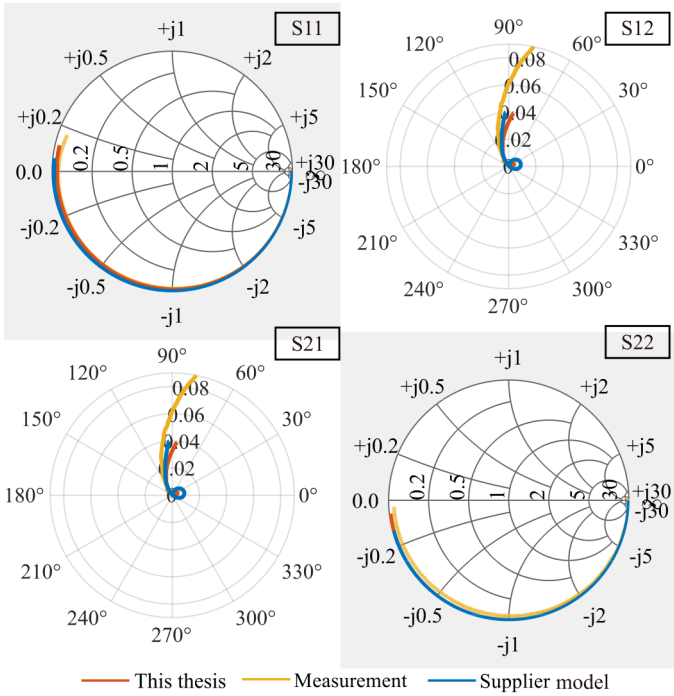

Figure 5.5: Comparison of S parameters from measurement, the supplier's model, and the proposed model in the off region under the bias condition $V_{GS} = 0$ V, $V_{DS} = 550$ V. The frequency range spans from 200 kHz to 1 GHz to mitigate low-frequency noise.

during lower-device turn-on, potentially resulting in shoot-through and device overstress [27], [114].

For meaningful simulation correlation to measurements, key parasitic elements, including gate resistance, gate loop inductance, power loop inductance, and parasitic capacitance, should be incorporated into the simulation to closely reflect the actual circuit behavior. FEM analysis is usually adopted to simulate the PCB and compute the parasitic values. In this study, a surface-mounted test board as shown in Fig. 5.12 is designed to experimentally determine the parasitic inductance and capacitance. Parasitic capacitances are measured using an empty PCB with connection points indicated in Fig. 5.13. For parasitic inductance extraction, the configuration shown in Fig. 5.14 is

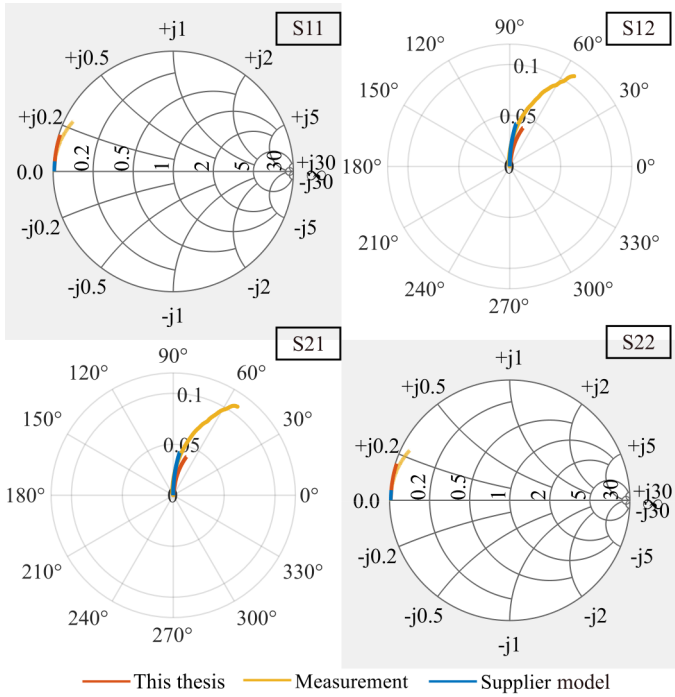

Figure 5.6: Comparison of S-parameters from measurement, the supplier's model, and the proposed model in the off region under the bias condition $V_{GS} = +6$ V, $V_{DS} = 0$ V. The frequency range spans from 200 kHz to 1 GHz to mitigate low-frequency noise.

Table 5.3: Specifications and Operation Conditions

Parameter	Description	Value
V_{DC}	DC-link voltage	[100, 200, 300, 400] V
I_{load}	Desired load current	[1.32, 2.66, 4.00, 5.33] A
L	Load inductance	0.15 mH
V_{GS}	Gate voltage	[-3, +6] V
R_{on}	Gate resistance	[5, 10, 15] Ω
R_{off}	Gate resistance	[5, 10, 15] Ω
T_a	Ambient temperature	25 °C

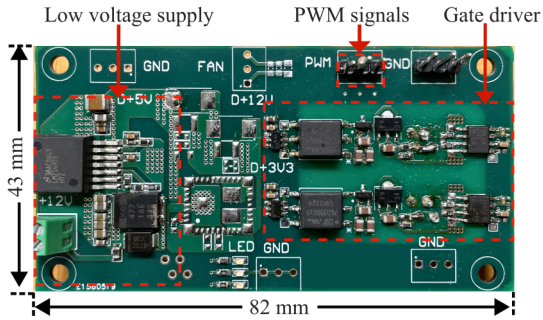

Figure 5.7: Six-layer gate driver board fabricated on FR4 substrate with 1.6 mm thickness.

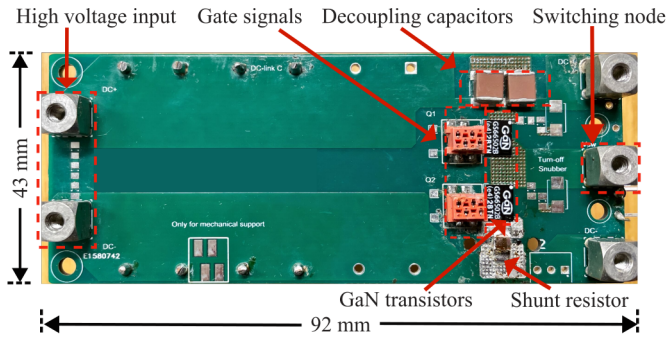

Figure 5.8: Four-layer power board fabricated on FR4 substrate with 1.6 mm thickness.

employed, where additional wires are used to short the pads and close the circuit loop. These wires serve two purposes: increasing the total impedance to ensure it falls within the valid measurement range of the one-port reflection method (Fig. 4.4) and enabling a practical connection between the PCB and the test board. To eliminate the influence of the added wires, a 40 mm reference wire is separately characterized (Fig. 5.15). Assuming that the inductance of the wire is proportional to its length, the power loop inductance is determined by subtracting the calibrated wire contribution from the total measured inductance, as expressed in the following equation

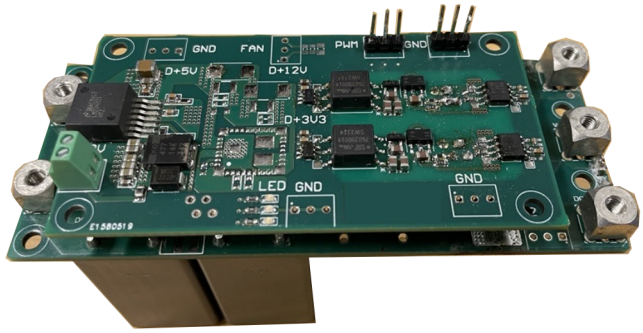

Figure 5.9: Assembled half-bridge converter showing vertical integration of the gate driver on top of the power board, resulting in a total height of 57 mm including the DC-link capacitors.

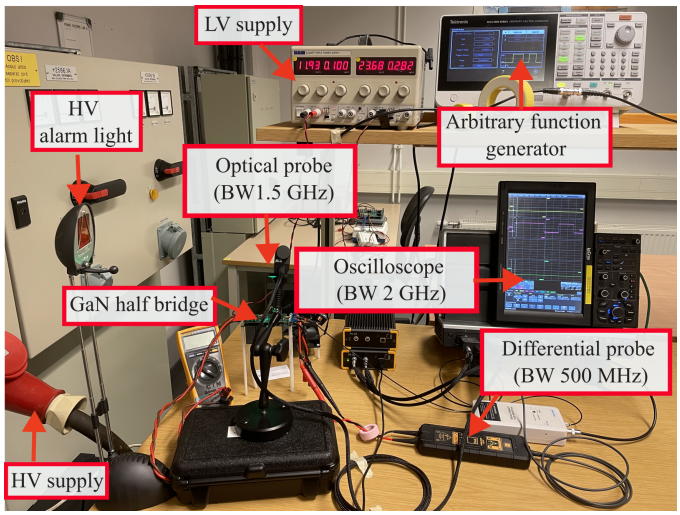

Figure 5.10: Experimental DPT setup built for a GaN-based half-bridge configuration. To capture the rapid switching transients, the FireFly optical probes with 1.5 GHz bandwidth are used to capture gate voltages, and the Bumblebee high-voltage differential probe with 500 MHz bandwidth is used to measure the drain voltage.

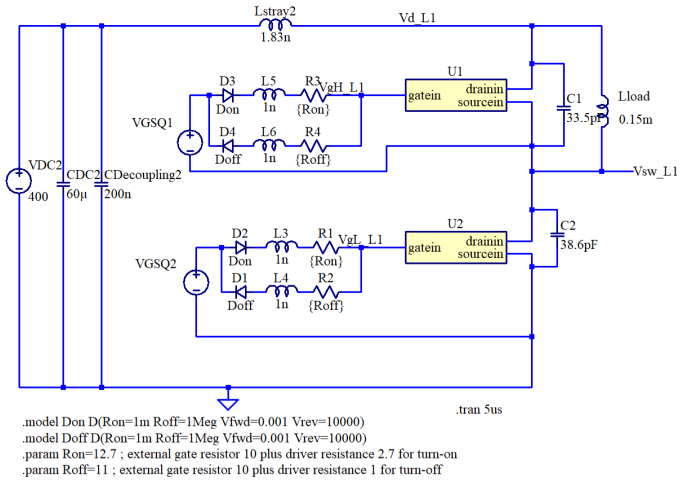

Figure 5.11: Simulation circuit with the proposed model in LTspice. The parasitic inductance and capacitance from the PCB for both the power loop and gate driver loop are considered to represent a realistic situation. The external gate resistance is 10 Ω, while the gate driver contributes an additional 2.7 Ω and 1 Ω to the total gate resistance for turn-on and turn-off circuits, respectively.

$$\begin{aligned} L_{\text{stray}} &= L_{\text{total}} - L_{\text{wire}} \frac{20 + 20 + 2.45 + 2.45 + 0.86}{40} \\ &= L_{\text{total}} - 1.144 L_{\text{wire}} \end{aligned} \tag{5.4}$$

where the length of each part is given in Fig. 5.14.
The measurement results are presented in Fig. 5.16 – Fig. 5.17. The parasitic capacitances are extracted by averaging the measured values over the 20 – 40 MHz frequency range, consistent with the procedure used for intrinsic capacitance determination. The parasitic inductances are obtained by averaging over the 10 – 20 MHz range, where the influence of resonance between parasitic inductance and capacitance is minimized. The extracted values are summarized in Table X. The measured inductance value is consistent with the simulated optimal power loop inductance [113], [115], which confirms the accuracy and reliability of the measurement. It should be noted that the gate

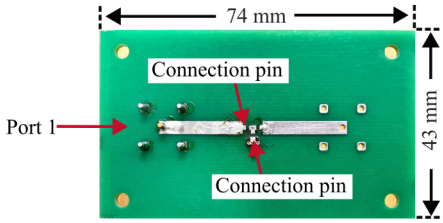

Figure 5.12: Test board for parasitic element characterization fabricated on FR4 substrate with 1.6 mm thickness.

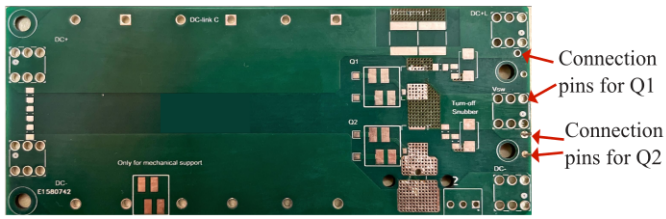

Figure 5.13: Illustration of connection pins for parasitic capacitance (C_1 and C_2) measurements of both GaN devices.

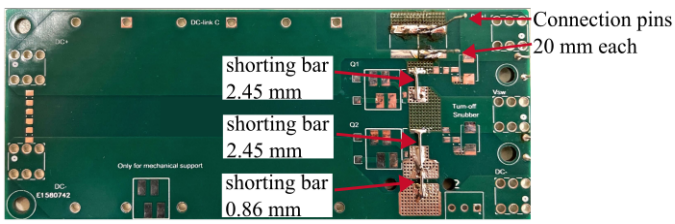

Figure 5.14: Illustration of connection pins for parasitic inductance (L_{total}) measurement of the half bridge.

loop inductance is estimated using a rule-of-thumb approximation to represent the inductive contribution of the gate loop.
Various operating conditions are measured to verify the performance and robustness of the proposed model. Validating the model across multiple operating points is important because GaN switching behavior is nonlinear and depends on voltage, current, and switching speed. A model that matches measurements at a single condition may not remain accurate when operating

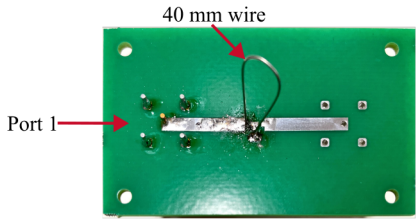

Figure 5.15: Illustration of 40 mm wire inductance (L_{wire}) measurement to compensate for additional wires introduced in inductance measurement.

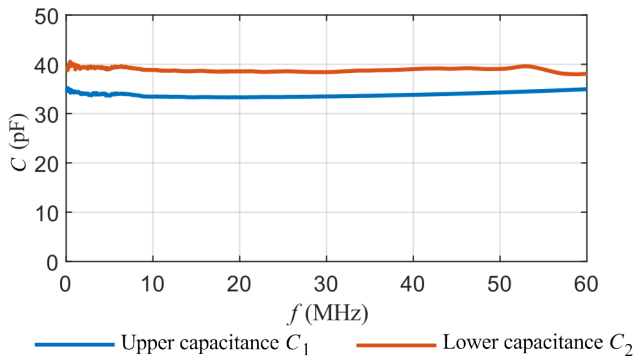

Figure 5.16: Parasitic capacitance measurements for both upper and lower GaN devices.

Table 5.4: Measured Results for Parasitic Elements

Parameter	Description	Value
C_1	Parasitic capacitance of Q_1	33.5 pF
C_2	Parasitic capacitance of Q_2	38.6 pF
L_{stray}	Power loop inductance	1.83 nH

points change. Therefore, tests under different conditions ensure the validity of the extracted parameters and the predictive capability of the model over a wide practical range.

As shown in Fig. 5.18, the proposed model demonstrates strong agreement with the measured waveforms in both timing and shape of the gate–source voltage V_{GS}, drain–source voltage V_{DS}, and drain current I_{DS} under differ-

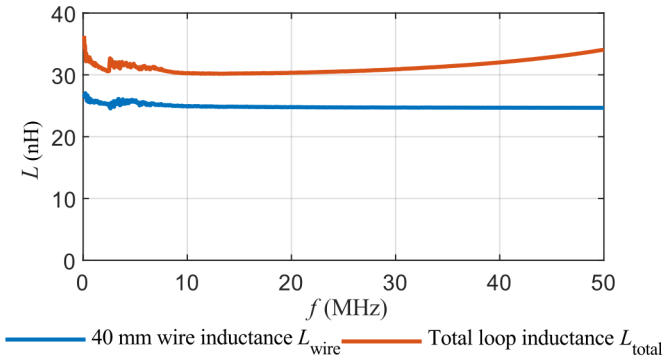

Figure 5.17: Parasitic inductance measurements for total loop inductance and wire inductance.

ent operating conditions. In particular, the model accurately reproduces the high-frequency ringing observed in the experimental voltage waveforms, which originates from the interaction between parasitic inductances and capacitances in the circuit. This agreement highlights the fidelity and predictive capability of the proposed modeling approach. In contrast, the supplier's model produces more damped responses, underestimating the oscillatory behavior observed in the measurements.

Some discrepancies are observed, which may be attributed to differences in parasitic elements and measurement setup. Specifically, because of the higher measured parasitic inductance in the proposed model, the ringing peaks in the gate-source voltage at the turn-on moment are higher, and the ringing frequency is lower than that predicted by the supplier's model. The measured data exhibit the lowest ringing frequency in the gate-source voltage, likely due to additional parasitic inductance and capacitance of the measurement equipment and peripheral circuitry. A higher overshoot voltage is observed in the measured drain–source waveform during turn-off [29], [70], [73], and its origin cannot be fully explained by the conventional estimation

$$\Delta V = L_{\text{stray}} \frac{di}{dt} \tag{5.5}$$

which assumes low-speed switching behavior. As discussed in [116], this expression is not directly applicable to GaN devices operating at very high

switching speeds. For certain operating conditions, the parasitic inductance and capacitance form a resonant loop in which appropriately distributed inductance can reduce, rather than simply increase, the overshoot voltage. In addition, measurement artifacts may contribute to the observed discrepancy. The differential probe has long leads when connecting to the test point on the PCB, indicating that extra parasitics can be introduced when capturing fast transient signals, which may influence the measured waveform.
For further validation, switching waveforms obtained with different gate resistances are presented in Fig. 5.19. Reducing the gate resistance increases the switching speed and makes the circuit more sensitive to parasitic elements, which provides a useful stress case for evaluating model behavior. Under these conditions, the supplier model predicts oscillatory behavior and instability trends that deviate from the measurements, whereas the proposed model continues to track the measured evolution of ringing and overall waveform shape as the gate resistance varies. Although minor discrepancies remain, the qualitative consistency across operating conditions indicates that the extracted parasitic parameters and modeling framework capture the dominant switching dynamics with reasonable accuracy.
Together, these results support the improved predictive capability of the proposed model for realistic switching behavior relevant to power converter applications. In addition, under identical simulation settings in LTspice and same operation conditions ($V_{\mathrm{DC}} = 400$ V, $I_{\mathrm{load}} = 5.33$ A), the proposed model demonstrates higher computational efficiency compared to the supplier's model as tabulaetd in Table 5.5, making it suitable for practical circuit-level analysis without increased simulation cost and with improved transparency.

Table 5.5: Comparison of Simulation Time at Different Gate Resistances.

	$R = 5\ \Omega$	$R = 10\ \Omega$	$R = 15\ \Omega$
Supplier model	4.79 s	1.47 s	1.22 s
This thesis	2.19 s	1.07 s	1.10 s

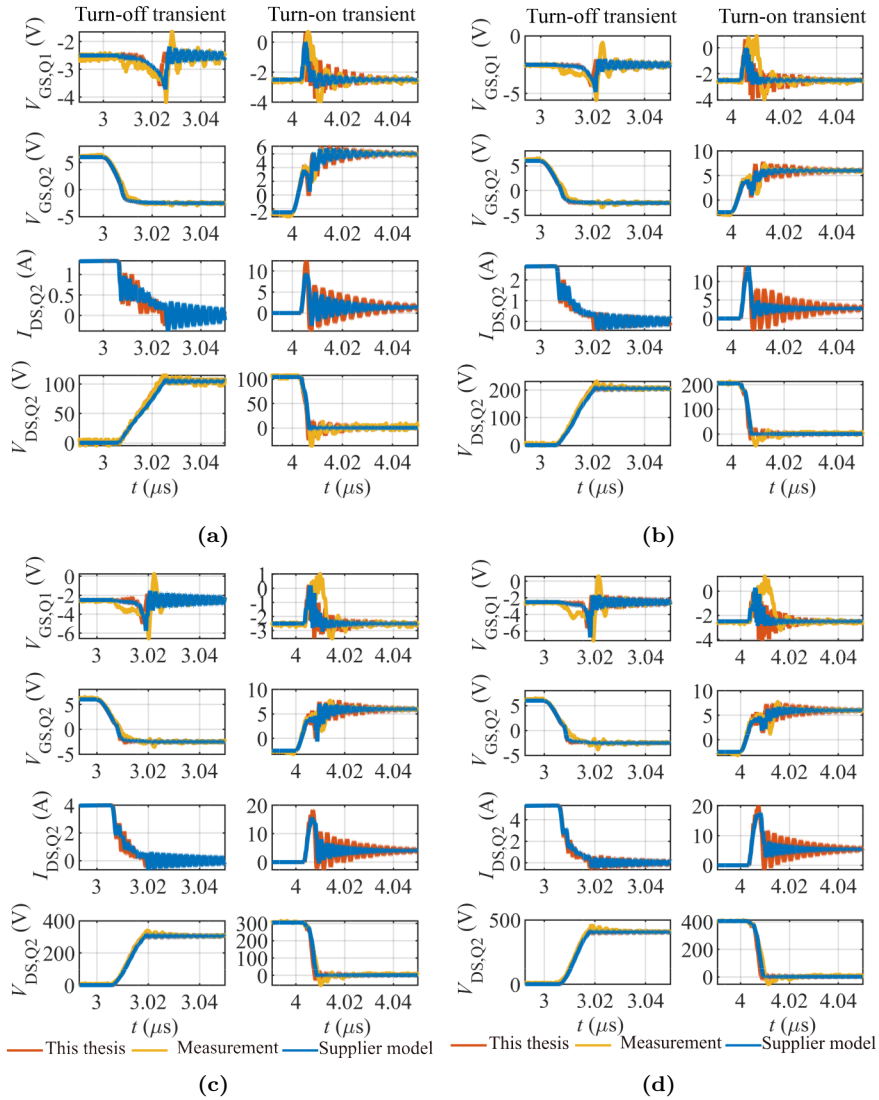

Figure 5.18: Comparison of DPT waveforms obtained from measurement, the supplier's Level 3 model, and the proposed model with $R_{on} = R_{off} = 10$ Ω (a) $V_{DC} = 100$ V, $I_{load} = 1.32$ A; (b)$V_{DC} = 200$ V, $I_{load} = 2.66$ A; (c) $V_{DC} = 300$ V, $I_{load} = 4.00$ A; (d) $V_{DC} = 400$ V, $I_{load} = 5.33$ A.

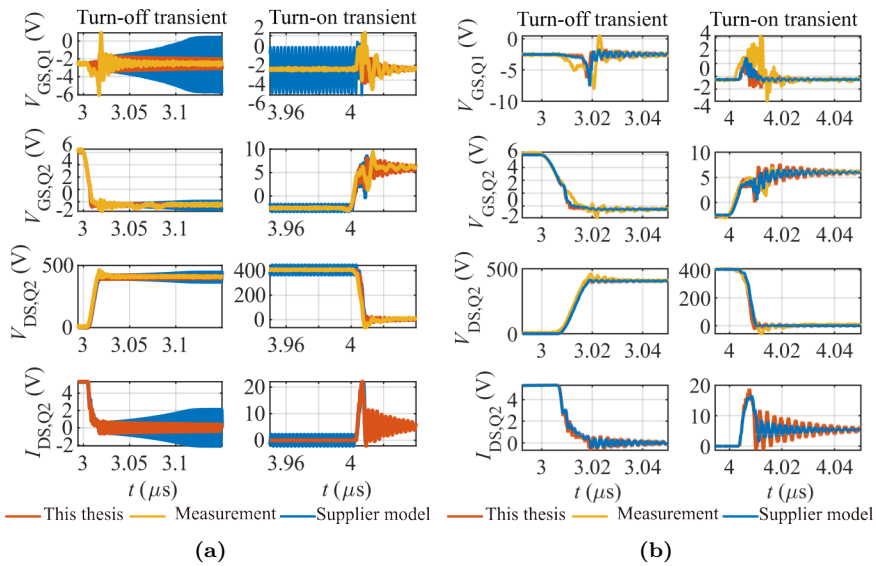

Figure 5.19: Comparison of DPT waveforms obtained from measurement, the supplier's Level 3 model, and the proposed model with $V_{\mathrm{DC}} = 400$ V, $I_{\mathrm{load}} = 5.33$ A (a) $R_{\mathrm{on}} = R_{\mathrm{off}} = 5\ \Omega$; (b) $R_{\mathrm{on}} = R_{\mathrm{off}} = 15\ \Omega$.

CHAPTER 6

Concluding Remarks and Future Work

This thesis presents a practical and accurate methodology for characterizing surface-mounted packaged GaN power transistors using S-parameter characterization, enabling reliable extraction of low-nanohenry and picofarad circuit elements and the direct implementation in SPICE-compatible device models. The work demonstrates that broadband S-parameter measurements can be effectively applied to characterize GaN power transistors, providing a consistent framework that links microwave measurement techniques with power electronics device modeling. A dedicated measurement and calibration approach is developed to enable reliable extraction of the very low parasitic impedances typically present in packaged GaN devices. Using broadband measurements up to 1 GHz, the intrinsic and extrinsic capacitances, resistances, and inductances are directly extracted from the measured S-parameters. The extracted parameters are then fitted using physics-based analytical expressions and incorporated into a Spice-compatible compact model, ensuring computational efficiency while avoiding the need for proprietary device geometry or process information. The validity of the proposed extraction methodology is demonstrated through both frequency and time domain validations. In the frequency domain, the simulated S parameters show strong agreement with measure-

ments across the measured frequency range. In the time domain, DPT results confirm that the developed model accurately reproduces the measured switching behavior of the device better than the supplier model, demonstrating its suitability for power converter simulations.
Overall, the proposed methodology provides a practical and accurate framework for translating broadband S-parameter measurements of GaN transistors into SPICE-compatible models, enabling accurate extraction of low-impedance parasitic elements and improving the predictive capability of circuit-level simulations for high-speed GaN power converters.
For future work, the proposed framework can be extended to incorporate a detailed thermal analysis to investigate the temperature dependence of the circuit parameters. This would involve repeating the characterization and extraction procedures under various temperature conditions, thereby enabling the development of a comprehensive thermal behavioral model. In addition, the observed discrepancies between simulation and measurement results highlight that device parameters are comparable to PCB parasitics, making accurate modeling difficult and potentially impacting overall system performance. High-fidelity measurement of fast transient voltage and current waveforms in GaN switching circuits would further enable systematic comparison of key dynamic characteristics, such as switching losses, voltage and current overshoot, and di/dt and dv/dt rates, thereby improving the reliability of switching behavior prediction in high-speed GaN power converters.

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