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RESEARCH ARTICLE OPEN ACCESS

A Low-Power Cryogenic Low-Noise Amplifier for the Next-Generation Quantum Computers

Nelson Rebelo[1,2] | Johan Bergsten[1] | Arsalan Pourkabirian[1] | Niklas Wadefalk[1] | Jan Grahn[2]

[1]Low Noise Factory AB, Gothenburg, Sweden | [2]Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden

Correspondence: Nelson Rebelo (rebelo@lownoisefactory.com)

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ABSTRACT

Next generation of quantum computers calls for reduced dc power dissipation of the cryogenic low-noise amplifier (LNA) applied in reading out the superconducting qubits. This article reports on processing and evaluation of a 100-nm gate length indium phosphide high electron mobility transistor (InP HEMT) technology used in the design of such LNAs. InP HEMTs with size of 4 × 50 µm were measured on-wafer by DC and S-parameter characterization. Device noise performance was indirectly evaluated by measuring and modeling the gain and noise of a three-stage hybrid 4–8 GHz cryogenic LNA equipped with the InP HEMTs. When operating the LNA at a DC power of 2.1 mW, the InP HEMT LNA average noise temperature was 1.4 K with an average gain of 41.6 dB. The minimum noise temperature of the InP HEMT was estimated to be 1.1 K at 6 GHz. The performance achieved for the InP HEMT LNA is comparable to the LNAs currently used in quantum computing while requiring only 27% of the DC power consumption. Small-signal modeling of the InP HEMT suggested that this was due to a low output conductance associated with a large gate-recess length used in device fabrication.

1 | Introduction

The indium phosphide (InP) high-electron mobility transistor (HEMT) is used in cryogenic low-noise amplifiers (LNAs) for applications ranging from radio astronomy [1] to superconducting quantum computing [2]. For the latter case, the InP HEMT LNA is employed for reading out qubits at frequencies normally between 4 and 8 GHz at the 4 K stage in the cryostat [3]. As future quantum computers are foreseen to handle large numbers of qubits, many more InP HEMT LNAs are expected than today. Since these are the most power-hungry components in the dilution refrigerator, the DC power consumption of the InP HEMT LNA therefore risks limiting quantum system upscaling [4]. At present, InP HEMT LNAs operated at normal bias in quantum computing may consume up to 10 mW each [5]. Fortunately, there are several approaches to reduce the DC power of the InP HEMT LNA towards and even below 1 mW. Low-power operation for qubit readout has recently been reported based on optimization of the InP HEMT heterostructure, the LNA design itself, and the operation of the LNA [6–9]. However, amplifying qubits at low DC power normally comes at a cost in degraded gain and noise of the InP HEMT LNA, which cannot always be tolerated from a quantum system perspective.

This work presents a 100 nm gate-length InP HEMT technology for low-power cryogenic LNAs for reading out qubits in superconducting quantum computing. The 4 × 50 µm InP HEMTs were evaluated at 4 K in a three-stage hybrid LNA. Compared to industrial state-of-the-art, the InP HEMT LNA demonstrated similar performance in gain and noise at nearly fourfold reduction in DC power [5]. Small-signal analysis suggested that this was due to a low output conductance of the InP HEMT, which was a consequence of the use of a large gate-recess length in device fabrication.

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2 | Device Technology

The epitaxial structure was grown by molecular beam epitaxy on a 100-mm diameter semi-insulating InP substrate. The epitaxial stack, from bottom to top, consisted of a 500-nm thick $In_{0.52}Al_{0.48}As$ buffer, a 15-nm pseudomorphic $In_{0.65}Ga_{0.35}As$ channel, a 9-nm $In_{0.52}Al_{0.48}As$ barrier, a 4-nm InP etch stopper, and finally a 20-nm n^+ $In_{0.52}Ga_{0.47}As$ cap layer. In the barrier, a single Si δ-doping layer was introduced 5 nm from the top of the channel which defined the spacer thickness of the InP HEMT. The amount of Si δ-doping was calibrated to obtain a two-dimensional electron gas (2DEG) concentration of $3 \times 10^{12}\,cm^{-2}$ in the channel. The InP layer served the dual purpose of providing etch selectivity during gate-recess formation [10] and passivating the InAlAs barrier surface. More details of the design of the epitaxial stack can be found in Ref. [7].

The fabrication process is summarized in Figure 1. Device isolation was carried out by a mesa wet chemical etch using phosphoric acid (Figure 1a). Prior to ohmic contact deposition, the gate recess was wet etched using a succinic acid/H_2O_2 solution (Figure 1b). This so-called recess-first approach prevented adverse electrochemical etching of the semiconductor surface in the presence of metals resulting in a high uniformity of the gate-recess region [11]. Alloyed ohmic contacts for source and drain were formed by evaporation of a Ni/Ge/Au/Pt/Au sequence followed by a rapid thermal anneal (Figure 1c). At 300 K, the sample had a contact resistance of 0.02 Ω.mm and a sheet resistance of 60 Ω/□ using a source–drain distance of 1.2 μm.

T-shaped gates were defined by a two-step electron beam lithography process, which separately exposed the gate foot and the gate hat (Figure 1d). This enabled precise control of the 100-nm gate length. A gate metal stack of Pt/Ti/Pt/Au was deposited by electron-beam evaporation. A metal contact stack of Ti/Au was then evaporated. During the subsequent device passivation of 150 nm thick silicon nitride by plasma-enhanced chemical vapor deposition at 270°C (Figure 1e), the Pt gate metal diffused through the InP etch stop layer into the barrier thus defining the gate-to-channel distance. The process was finished with the electroplating of Au air bridges which allowed fabrication of multi-finger InP HEMTs (Figure 1f). Individual InP HEMTs were prepared by wafer thinning, scribing, and breaking.

In Figure 2, a scanning transmission electron microscope (STEM) image is shown for one of the four gate fingers of the 4 × 50 μm InP HEMT. A well-defined 100 nm-gate length is observed. From higher magnification pictures using STEM, the gate-to-channel distance was estimated to be 6 nm. The gate recess in Figure 2 shows a high uniformity with a length of almost 600 nm, which is twice as large as in our previous work [7]. Moreover, the gate alignment offset seen in Figure 2 is a consequence of the first-recess approach used in processing. Since two of the gate fingers will be aligned towards the source and two towards the drain, the slight offset in gate alignment of the InP HEMT is not believed to influence the results here.

3 | Characterization

3.1 | DC Measurements

DC characterization of 4 × 50 μm InP HEMTs was performed on-wafer at 300 and 4 K using a Lakeshore CRX-4K cryogenic probe

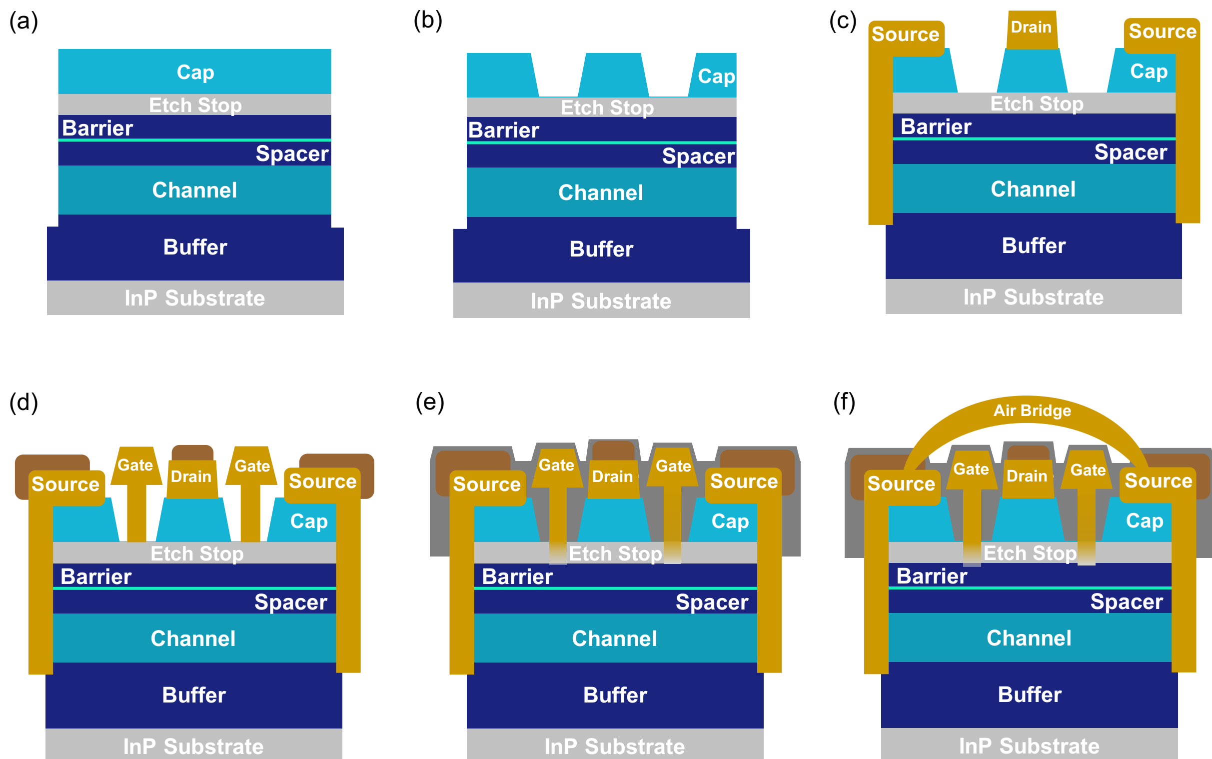

FIGURE 1 | Schematic of processing steps in 4 × 50 μm InP HEMT fabrication: (a) device isolation, (b) gate-recess etch, (c) ohmic deposition and annealing, (d) gate and metal contact deposition, (e) passivation, and (f) air bridge formation.

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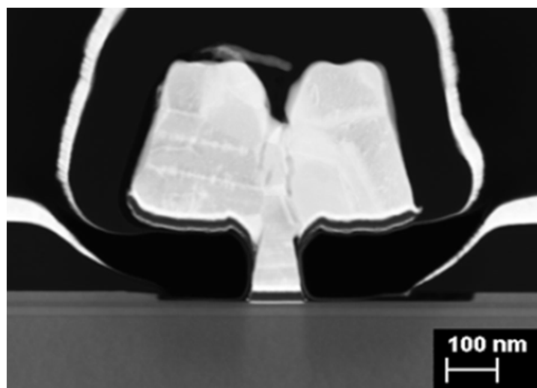

FIGURE 2 | STEM cross-section of a 100-nm gate length InP HEMT highlighting InGaAs channel, gate recess, gate stack, and device passivation.

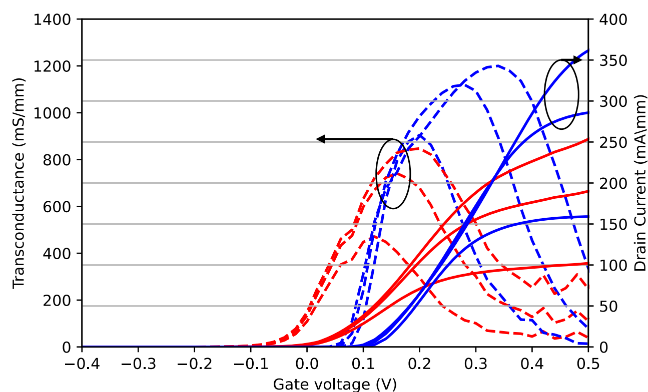

FIGURE 4 | Drain current (solid line) and transconductance (dashed line) versus gate voltage with drain voltage from 0.1 to 0.4 V in 0.1 V steps at 300 K (red) and 4 K (blue) for a 4 × 50 μm InP HEMT.

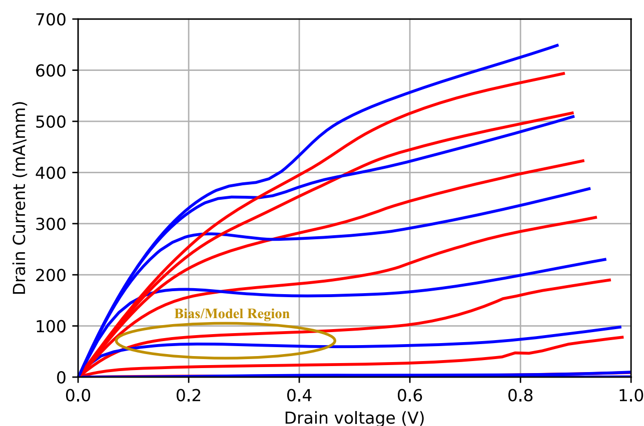

FIGURE 3 | Drain current versus drain voltage with gate voltage from 0 to 0.6 V in 0.1 V steps at 300 K (red line) and 4 K (blue line) for a 4 × 50 μm InP HEMT. The bias region used in modeling is shown.

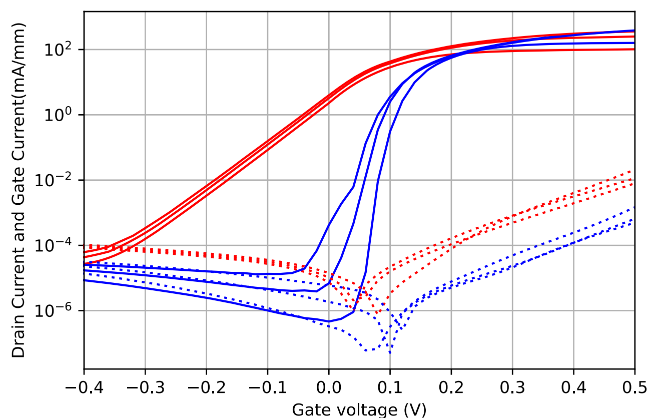

FIGURE 5 | Drain current (filled line) and gate current (dotted line) versus gate voltage with drain voltage of 0.1, 0.3, and 0.5 V at 300 K (red) and 4 K (blue) for a 4 × 50 μm InP HEMT.

station. In Figure 3, the drain current versus drain(-source) voltage for 300 and 4 K is plotted. The output characteristic shows a substantial change upon cooling, with maximum drain current rising from 520 to 650 mA/mm at a gate(-source) voltage of 0.6 V. The InP HEMT on-resistance decreases from 0.65 to 0.44 Ωmm which to a major part is due to the much higher mobility of InGaAs at 4 K compared to 300 K, 60,000, and 11,000 $cm^2V^{-1}s^{-1}$, respectively. At 4 K, a kink is seen at around 0.3 V drain voltage. Such behavior in output current at relatively high drain current densities is typical for cryogenic InP HEMTs in the absence of an InP etch stop layer [11]. The observation of a kink in Figure 3 is therefore probably related to the use of a large gate-recess length for the InP HEMT. As explained below in Sec. 3.2, the kink will not be of any concern in the cryogenic LNA testing.

Figure 4 shows the transfer characteristics and the DC transconductance of the InP HEMT. The threshold voltage is – 0.1 V at 300 K and 0.05 V at 4 K, meaning that there is a positive threshold voltage shift from depletion to enhancement mode upon cooling. For a drain voltage of 0.225 V when comparing 300 and 4 K, the transconductance increases by 33% from 800 to 1100 mS/mm, respectively. A peak transconductance of 1200 mS/mm is observed at 4 K for a drain voltage of 0.3 V. The steep rise in DC transconductance versus gate voltage at 4 K is typical for a low-noise transistor.

The drain current in logarithmic scale versus gate voltage is presented in Figure 5. A subthreshold swing of 12 mV/dec is found for a drain voltage of 0.1 V at 4 K. In Figure 5, the gate current is also plotted for 300 and 4 K. At a gate voltage of −0.4 V, the gate current is reduced by cooling, from 0.2 to 0.04 μA/mm. The influence from such a gate current level on the noise performance of the cryogenic InP HEMT is negligible at typical qubit readout frequencies [1].

In Figure 6, the drain current and output conductance for gate voltages of 0.15, 0.20, and 0.25 V are plotted at 4 K. Such biases are representative for the operation of the InP HEMT in the cryogenic LNA testing described in Section 3.2. A low drain current density and output conductance in Figure 6 are essential for low-noise operation of the InP HEMT LNA at reduced DC power [12].

3.2 | HEMT LNA Testing

The InP HEMT displays extremely low noise values under cryogenic conditions. Therefore, direct noise parameter

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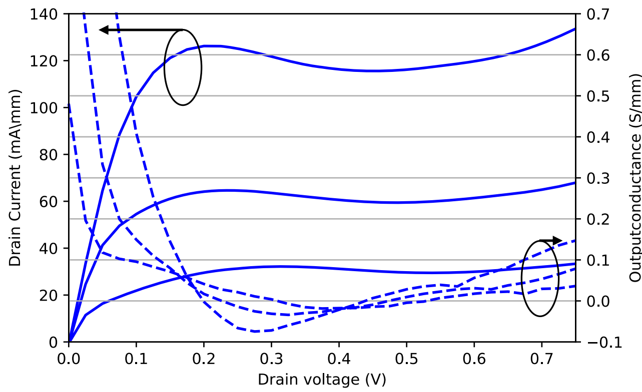

FIGURE 6 | Drain current (filled line) and output conductance (dashed line) versus drain voltage with gate voltage of 0.15, 0.2, and 0.25 V at 4 K for a 4 × 50 µm InP HEMT.

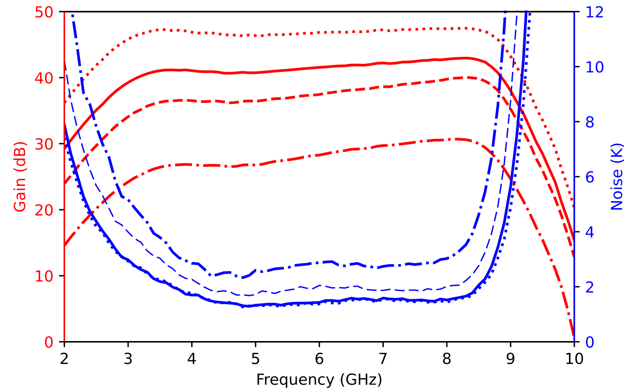

FIGURE 7 | Gain (red line) and noise (blue line) for a three-stage InP HEMT LNA at 4 K. LNA DC power of 0.3 mW (dotted-dashed line), 1 mW (dashed line), 2.1 mW (full line), and 7.8 mW (dotted line).

measurements are difficult and unreliable. In this study, the noise of the InP HEMT was instead evaluated indirectly by measuring gain and noise at 4 K for a three-stage 4–8 GHz hybrid LNA equipped with the 4 × 50 µm InP HEMTs. The noise of the InP HEMT could then be extracted by simulating the noise and gain of the LNA using a small-signal noise model (Sec. 3.3) [13].

The noise measurement of the cryogenic InP HEMT LNA was carried out by the Y-factor method using the cold attenuator technique [14]. This method provides a fast and relatively accurate determination of the (equivalent input) noise temperature for a wideband cryogenic LNA [15]. The largest uncertainty in noise temperature originates from the determination of the physical temperature of the attenuator just before the LNA in the cryostat. In the setup used here, the temperature sensor was attached to the 20 dB attenuator [11]. We estimate the total noise uncertainty to 0.3 K [16] with a measurement repeatability of 0.05 K. In Ref. [17], independent noise measurements carried out at National Institute of Standards and Technology for the same type of cryogenic LNA used here showed good agreement with the noise temperature obtained by our method.

The individual 4 × 50 µm InP HEMTs were mounted and then wire-bonded in the hybrid LNA. The three stages were biased identically at low gate voltages and drain current densities where no anomalies in output current were present, see circled region in Figure 3, thus permitting the use of the small-signal noise model. Since the gain for each stage was high, the noise of the LNA was dominated by the first InP HEMT [18].

Figure 7 demonstrates measured gain and noise at 4 K for the InP HEMT LNA biased at four different levels of DC power. At a DC power dissipation of 7.8 mW corresponding to a drain voltage of 0.44 V and drain current density of 22 mA/mm for each InP HEMT, the average gain and noise temperature for the LNA are 46.9 dB and 1.4 K, respectively. These numbers are comparable to state of the art [19]. At 2.1 mW (drain voltage of 0.22 V and drain current density of 12 mA/mm for each InP HEMT), the LNA still exhibits an average gain and noise temperature of 41.6 dB and 1.4 K, respectively. Compared to a DC power of 7.8 mW representative for LNAs in today's quantum computing [5], this implies that the InP HEMT LNA can be operated at 3.7 times lower DC power consumption without penalty in noise and only 5.3 dB reduction in gain. At 1 mW DC power, (drain voltage of 0.04 V and drain current density of 8.3 mA/mm for each InP HEMT), the LNA has average gain and noise of 38 dB and 2.2 K. At 0.3 mW (drain voltage of 0.07 V and drain current density of 5 mA/mm for each InP HEMT), the LNA average gain and noise temperature are 28.3 dB and 2.7 K, respectively. This is a slight improvement compared to our previous results reported in Ref. [20].

3.3 | InP HEMT Noise Extraction

S-parameter measurements were performed on wafer from 100 MHz to 67 GHz using the cryogenic probe station described in Section 3.1. The measurements were conducted at the same bias conditions and temperature as for the InP HEMTs in the LNA testing (Section 3.2). From the measured S-parameters, small-signal model parameters were extracted based upon the procedure in Ref. [21]. In short, the method uses three S-parameter measurements to extract all the model parameters: one-pinched cold HEMT measurement to obtain the parasitic capacitances, one forward cold HEMT measurement to extract the parasitic inductances and resistances, and finally, the active HEMT bias point measurement used in LNA operation. Intrinsic HEMT parameters in the model can then be extracted. These were used to build the Pospieszalski equivalent circuit noise model [22] as shown in Figure 8. In Figure 9, it is seen that the model agrees very well with the S-parameter measurements with an rms error of 3.45%. Numerical small-signal model parameters of a 4 × 50 µm InP HEMT at 4 K run at 12 mA/mm drain current density (corresponding to 2.1 mW DC power consumption of the LNA) are presented in Table 1.

The result from the equivalent circuit modeling was integrated into an AWR Microwave Office model of the InP HEMT LNA used to simulate the gain and noise. The simulations and measurements depicted in Figure 10 for the InP HEMT LNA run at 2.1 mW DC power show excellent agreement justifying the extraction of the minimum noise temperature [22], representing the noise in the InP HEMT. A value of 1.1 K at 6 GHz was found. The data from Figure 10 allowed us to extract the equivalent drain temperature [22], an empirical noise model parameter

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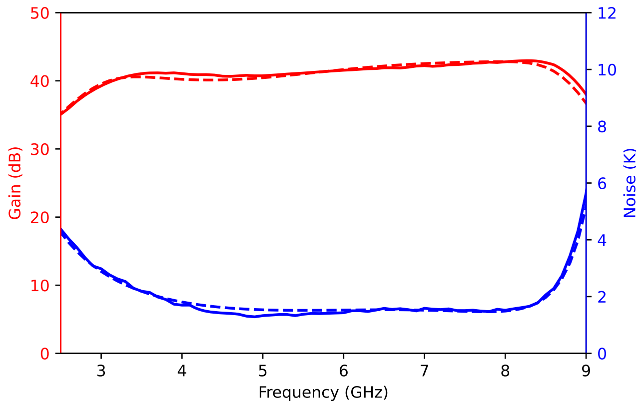

FIGURE 8 | Pospieszalski equivalent circuit model for the InP HEMT [22].

which was determined to be 230 K for the InP HEMT. Here, the equivalent gate temperature in the model was set to 10 K, considering the self-heating effect in the HEMT [13].

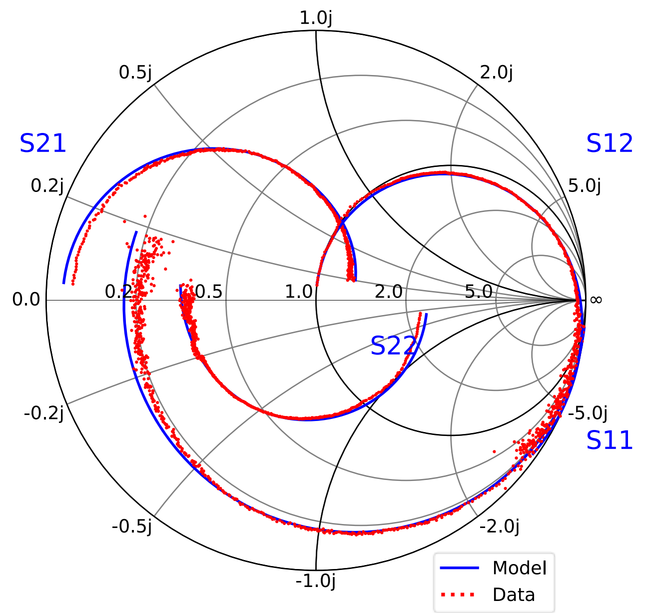

FIGURE 10 | Gain (red line) and noise (blue line) for a three-stage InP HEMT LNA at 4 K operated at 2.1 mW DC power operation. Measured (full line) and simulated (dashed line) curves from equivalent circuit model.

4 | Discussion

In Table 2, the gain and noise performance for the InP HEMT LNA in this work is compared with previously reported 4–8 GHz cryogenic LNAs [5, 19, 20, 23–26]. It is concluded that the LNA fabricated in this work exhibits gain and noise comparable or even somewhat better than state of the art. Compared to HEMT LNAs used in today's quantum computing [5], the LNA here demonstrates similar performance in gain and noise at 3.7 times lower power dissipation.

Compared to our previous studies [6, 12], Table 1 demonstrates a much lower (intrinsic) output conductance for the InP HEMTs fabricated here. This is also seen in the DC output conductance in Figure 6. As a result, the ratio of transconductance to output conductance was high at low drain current density (>16 at 12 mA/mm, and > 11 at 5 mA/mm) [12]. Because of its low output conductance, the InP HEMT in the cryogenic LNA can sustain a low noise temperature with high gain at low power dissipation, as seen in Table 2.

A plausible explanation for the low output conductance in this study is the use of a large gate-recess length in the HEMT. Here, 600 nm was used compared to 300 nm in Ref. [7]. As shown in Refs. [27] and [28], the output conductance of the InP HEMT decreases for increased gate-recess length, resulting in a higher transconductance-output conductance ratio. The disadvantage of

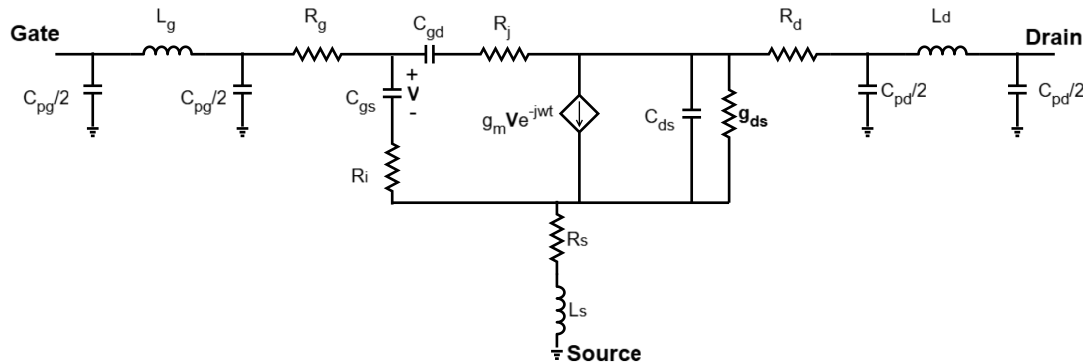

FIGURE 9 | S-parameter measurements for InP HEMT at 2.1 mW bias (red dots) and small-signal model (blue lines). S12 and S21 are scaled to better fit the Smith chart.

TABLE 1 | Intrinsic small-signal parameters of the equivalent circuit model for a 4 × 50 μm InP HEMT device at 12 mA/mm drain current density corresponding to an LNA DC power dissipation of 2.1 mW. Ambient temperature of 4 K.

R_s (Ω)	R_d (Ω)	R_g (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	g_m (mS)	g_{ds} (mS)	R_i (Ω)	R_j (Ω)
1.25	1.47	0.6	105.4	39.6	53.2	138.7	8.6	2.4	5.6

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TABLE 2 | Benchmarking of 4–8 GHz cryogenic LNAs.

Ref.	Technology	Average Gain (dB)	Average Noise Temp. (K)	DC Power (mW)
[5]	InP HEMT	42	1.5	7.8
[19]	InP HEMT	44.0	1.6	4.2
[20]	InP HEMT	23	3.2	0.3
[23]	InP HEMT	23.2	2.0	0.1
[24]	GaAs pHEMT	40	6.0	15.0
[25]	SiGe HBT	27.5	3.2	1.0
[26]	GaAs mHEMT	31	2.7	7.8
This work	**InP HEMT**	**28.3**	**2.7**	**0.3**
	InP HEMT	**41.6**	**1.4**	**2.1**
	InP HEMT	**46.9**	**1.4**	**7.8**

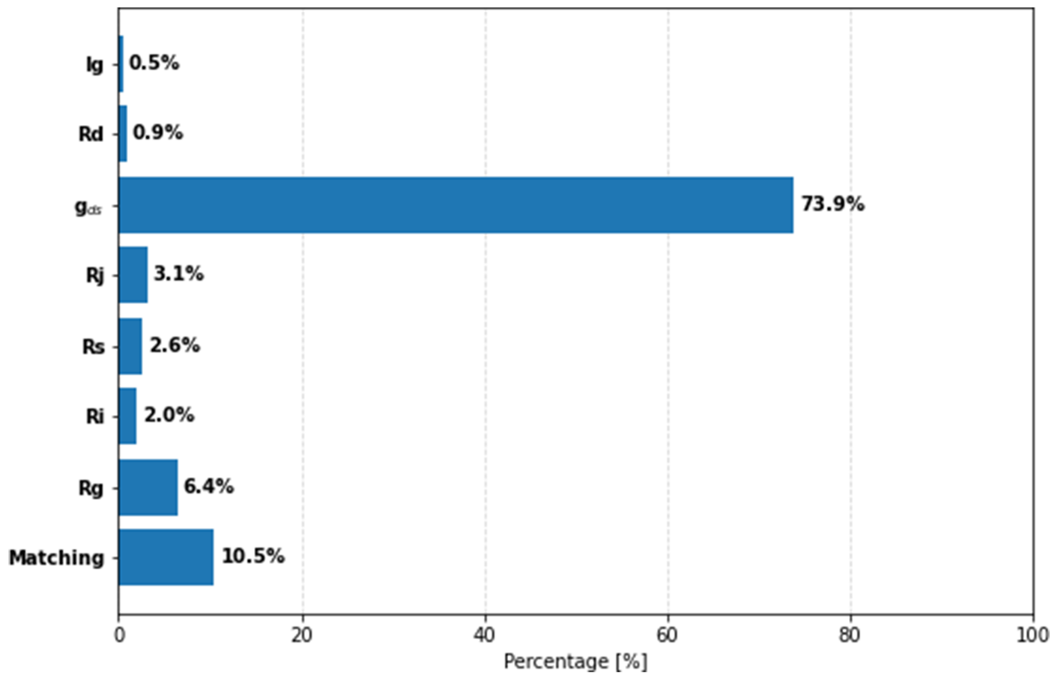

FIGURE 11 | Relative noise contributions in the InP HEMT LNA at 6 GHz and 4 K.

using an enlarged recess length in the gate region is an increased source resistance (R_s) which will be detrimental for noise performance. As mentioned in Section 3.3, R_s was obtained from a forward cold measurement [21] when recording the HEMT S-parameters at 4 K. The equivalent circuit is then simplified to a series combination of parasitic inductors and resistors where R_s can be derived by looking at the common-source configuration. The standard deviation of the extracted R_s was 0.06 Ω from 100 MHz to 50 GHz. We estimate that the increased gate-recess length used here doubled the source resistance from 0.64 to 1.25 Ω for the InP HEMT at 4 K. However, for a cryogenic InP HEMT, the noise contribution from parasitic elements such as source resistance is negligible compared to the HEMT channel noise [11]. The relative contributions of the noise sources in the InP HEMT LNA used in this work are shown in the histogram in Figure 11. The various noise contributions were obtained from simulations (in Microwave Office) at 6 GHz and at 4 K for the specific InP HEMT LNA used in this work. In Figure 11, the noise in the cryogenic InP HEMT LNA is dominated by the channel noise (g_{ds} in Figure 8). We simulated the noise for the InP HEMT LNA in Figure 10 using $R_s = 0.64\,\Omega$. Compared to $R_s = 1.25\,\Omega$, LNA noise was reduced with 0.048 K at 6 GHz, which is clearly within the noise uncertainty. As a result, device noise is expected to only marginally be affected by the larger gate-recess length. Nonetheless, it will result in a more surface-sensitive InP HEMT as confirmed in Figure 3 by a relatively small output current at large gate voltages together with the observation of the kink effect. This calls for an efficient device passivation process when using a large gate-recess length.

5 | Conclusion

A 100-nm gate length InP HEMT technology for cryogenic LNAs in superconducting quantum computing has been described.

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Discrete 4×50 μm devices were tested in a 4–8 GHz three-stage hybrid cryogenic LNA at a DC power of 2.1 mW. The InP HEMT LNA average gain and noise temperature at 4 K were 41.6 dB and 1.4 K, respectively. The minimum noise temperature of the InP HEMT was extracted to be 1.1 K at 6 GHz. It is proposed that the low-power operation yielding low noise and high gain for the InP HEMT LNA was due to a low device output conductance which was related to a large gate-recess length of 600 nm used in device fabrication. The InP HEMT LNA in this study was operated at 27% of the DC power used in today's superconducting quantum computing systems while maintaining essentially unchanged noise and almost the same gain.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The datasets generated and analyzed during this study are available from the corresponding authors upon reasonable requests.

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