Optimization of modular multilevel converter with half-bridge or full-bridge submodules for energy storage applications

Electric Power Systems Research 260 (2026) 113406

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

Optimization of modular multilevel converter with half-bridge or full-bridge submodules for energy storage applications

Sohrab Mohtat [a,*], Massimo Bongiorno [a], Mebtu Beza [a], Jan R. Svensson [b], Jon Rasmussen [c]

[a] Chalmers University of Technology, Hörsalsvägen 11, 41296, Göteborg, Sweden
[b] Hitachi Energy Research, Hitachi Energy, Forskargränd 7, 722 26, Västerås, Sweden
[c] Hitachi Energy Consulting, Hitachi Energy, Gårdatorget 1, 412 50, Göteborg, Sweden

ARTICLE INFO

Keywords:
Converter design optimization
Energy requirement calculation
Grid-connected converter
Modular multilevel converter
Power losses evaluation

ABSTRACT

The Double Wye Modular Multilevel Converter (YY-MMC) equipped with energy storage on the DC-link is increasingly used in grid applications, to provide grid support and favor integration of renewable energy sources. This paper presents a comprehensive optimization framework for the Half-Bridge (HB-YY-MMC) and Full-Bridge (FB-YY-MMC) topologies, to determine the optimal converter design by considering key design parameters such as number of submodules (SMs), power losses, semiconductor rating, and SM capacitor size. The YY-MMC design is formulated as a multi-objective optimization problem, where the pole-to-pole DC voltage and the second-order circulating current serve as decision variables. For this purpose, a normalized cost function is developed based on a representative base-case cost distribution, where each cost component scales with its corresponding physical quantity for both topologies. For a given converter power rating, the optimization is performed considering different ratios between the allowed active and reactive powers to determine the most suitable topology for each power level. Finally, experimental results validate the effectiveness of the proposed approach, demonstrating its potential for design optimization of YY-MMC in grid-connected applications.

1. Introduction

Modular Multilevel Converters (MMCs) have become the industrial standard for high-power and high-voltage grid applications in recent years. Wye- and delta-connected configurations are primarily used for reactive power compensation, while the Double Wye MMC (YY-MMC) topology, which features a common DC link, is widely implemented in High-Voltage DC (HVDC) transmission systems [1,2]. MMC offers high efficiency, modular structure, excellent dynamic performance, and robustness when connected to weak grids [3]. The YY-MMC configuration incorporating Energy Storage (ES) on the DC-link has been deployed in grid applications, particularly to facilitate the integration of renewable energy sources [4,5]. In a YY-MMC configuration, each phase-leg comprises of upper and lower arms, with multiple series-connected submodules (SM) in each arm. These SMs can either be half-bridge (HB) or full-bridge (FB) converters, forming a HB-YY-MMC and FB-YY-MMC, respectively.

YY-MMC presents several challenges, primarily due to its high number of components [6–8]. Compared to a single-wye MMC (Y-MMC or cascaded FB converter), the YY-MMC offers the advantage of connecting a centralized ES to the converter's common DC link. However, this configuration introduces a circulating current caused by the phase difference in the SM's capacitor voltage ripples between the upper and lower arms [9]. In most applications, this circulating current is actively suppressed using a circulating current controller to minimize losses and current rating. However, rather than simply eliminating it, this current can also be controlled to optimize the converter's design. Another degree of freedom for optimization, which depends on the type of SM used, is the pole-to-pole DC voltage. Unlike the HB-YY-MMC, where the minimum required pole-to-pole DC voltage is dictated by the AC grid voltage, the FB-YY-MMC configuration allows this parameter to be selected freely. This added flexibility enables further optimization of the converter.

In recent years, several studies have explored different aspects of YY-MMC optimization [1,6–8,10–20]. However, most of these investigations focus on optimizing a single design parameter or, at best, attempt to improve one parameter without significantly affecting another.

For example, [6] targets the semiconductor size reduction by minimizing the peak arm current while limiting the associated increase in SM capacitance. The works in [7] and [8] aim to reduce the SM capacitance without significantly affecting the semiconductor ratings. Similar goals are pursued in [10] and [11], which also focus on capacitor size

* Corresponding author.
E-mail address: sohrab.mohtat@chalmers.se (S. Mohtat).

https://doi.org/10.1016/j.epsr.2026.113406
Received 23 February 2026; Received in revised form 18 May 2026; Accepted 1 June 2026
Available online 5 June 2026

Table 1
Comparison with existing YY-MMC optimization studies.

Reference	Topology	Optimization Variables	Design Parameters	Multi-objective	P_r/Q_r Considered	Cost function
[1]	FB	V_{DC}, I_{c2}, φ_{c2}	W, I_n, P_l	Trade-off	No	No
[6]	HB	I_{c2}, φ_{c2}	W, I_n	Constrained	Partial	No
[7]	HB + FB	I_{c2}, φ_{c2}	W, I_n	Constrained	Partial	No
[8]	FB	I_{c2}, φ_{c2}	W, I_n	Constrained	Yes	No
[10,11]	HB	I_{c2}, φ_{c2}	W	No	No	No
[12]	HB	I_{c2}, φ_{c2}	W, P_l	Constrained	No	No
[13]	HB	I_{c2}, φ_{c2}	W, I_n, P_l	Constrained	No	No
[14–16]	HB	I_{c2}, φ_{c2}	P_l	No	No	No
[17]	FB	V_{DC}	W	No	No	No
[18,19]	FB	V_{DC}	W	No	Yes	No
[20]	Hybrid	V_{DC}, I_{c2}, φ_{c2}	W	No	No	No
This work	**HB + FB**	V_{DC}, I_{c2}, φ_{c2}	W, I_n, P_l, N	**Yes**	**Yes**	**Yes**

reduction. Studies such as [12] and [13] address both capacitance and loss reduction. Meanwhile, [14] and [15] focus on overall loss reduction, while [16] specifically targets conduction loss minimization. These approaches commonly employ the amplitude and phase adjustment of second-order circulating currents for optimization.

In contrast, a smaller number of studies have explored the optimization in FB-YY-MMCs. Works such as [17–19] investigate the SM capacitance reduction using the pole-to-pole DC voltage. Notably, [20] considers both pole-to-pole DC voltage and second-order circulating currents to reduce SM capacitor size in a hybrid YY-MMC configuration employing both HB and FB SMs.

Despite these contributions, most existing studies do not fully examine the relationships between different design parameters or provide a completely optimized converter design. While [1] considers the combined effects of second-order circulating current and pole-to-pole DC voltage on losses, semiconductor ratings, and SM capacitance in the FB-YY-MMC, it primarily focuses on achieving a trade-off among these parameters rather than providing a comprehensive optimization. In other words, it does not formulate the problem as a multi-objective optimization problem, where all relevant design parameters (i.e., SM capacitor size, semiconductor rating, power losses, and number of SMs per arm) are considered at the same time to achieve an overall optimal converter design for a given application. Furthermore, [1] does not extend its findings to the HB-YY-MMC topology. Another key limitation of previous studies is that, for a given converter power rating, they do not investigate how varying the active-power capability (defined as the ratio between active and reactive power for a given converter rating) affects the optimal design of HB-YY-MMC and FB-YY-MMC. As a result, these works do not determine which topology is more suitable for different application scenarios associated with varying active-power capabilities.

The comparison of existing studies is summarized in Table 1. In the table, the optimization variables are defined as the pole-to-pole DC voltage (V_{DC}) and the second-order circulating current amplitude and phase (I_{c2} and φ_{c2}). The design parameters considered for optimization are also defined: W corresponds to the arm energy variation (directly related to SM capacitor size), I_n is the semiconductor current rating, P_l represents the power losses, and N denotes the number of SMs per arm. The column Multi-objective indicates whether the study performs a complete multi-objective optimization. Entries labeled as Constrained correspond to studies that focus on optimizing a single design parameter while ensuring that the other design parameters are not significantly affected, rather than performing a full multi-objective optimization considering all objectives at the same time. The table highlights gaps in the literature, including limited consideration of both HB and FB topologies, incomplete multi-objective optimization, and the effect of varying active-power capabilities on design parameters.

The aim of this paper is to achieve a fully optimized design for both HB-YY-MMC and FB-YY-MMC by formulating a comprehensive cost function that incorporates all key design parameters: the number of SMs, semiconductor ratings, power losses, and SM capacitance. This cost function provides a unified metric for converter design, allowing the optimization of multiple objectives at the same time and guiding the selection of an overall optimal converter configuration.

Furthermore, the study compares the optimal solutions of HB-YY-MMC and FB-YY-MMC across different operating modes, characterized by the ratio of rated active power P_r to rated reactive power Q_r for a given converter rating. This parameter reflects the type of services provided by the converter, ranging from E-STATCOM operation, representing energy storage functionality with limited active-power capability and energy, to full energy storage applications requiring high active-power exchange. Note that $P_r/Q_r = 0$ represents a special case corresponding to pure STATCOM operation, where only reactive power support is provided. This interpretation allows the proposed framework to consistently cover the full range of applications within a unified formulation.

The paper is structured as follows. Section 1 introduces the topology and dynamics of the YY-MMC, while Sections 2 and 3 describe the design parameters for the HB-YY-MMC and FB-YY-MMC, respectively. Section 4 presents the optimization methodology, including the cost function and its optimization. Section 5 discusses the experimental results, and Section 6 concludes the paper.

2. YY-MMC Topology and dynamics

The grid-connected YY-MMC shown in Fig. 1 is composed of three phase-legs, each consisting of an upper and lower arm. There are N series-connected FB or HB SMs and a filter reactor with inductance L and resistance R in each arm. An ES with a constant pole-to-pole DC voltage, V_{DC}, is connected to the converter's DC side, and the upper arm and lower arm voltages and currents are denoted as v_u, v_l, i_u and i_l, respectively.

The main difference between HB and FB SMs in the design of YY-MMCs lies in their ability to generate negative voltage levels, which impacts the overall converter design. While FB SMs can generate both negative and positive voltage, HB SMs are only capable of generating positive voltage. Consequently, the total arm voltage given by:

$$v_{u,l} = \frac{V_{DC}}{2} \mp V_s \cos(\omega t) \tag{1}$$

should be positive for HB-YY-MMC. In (1), the second term is the internal voltage of the YY-MMC that drives the grid current (i_g). From (1), using V_s as the base voltage, the HB-YY-MMC requires $V_{DC} \geq 2$ pu for proper operation. In contrast, the FB-YY-MMC has no such constraint, allowing V_{DC} to be a decision variable in its design optimization.

The upper and lower arm currents of a generic phase can be written as:

$$i_{u,l} = \pm\frac{i_g}{2} + i_c \tag{2}$$

where i_g is the current exchanged between the converter and the grid, and i_c is the current that circulates between the phase-legs and the common DC link of the converter. In sinusoidal steady-state operation of the

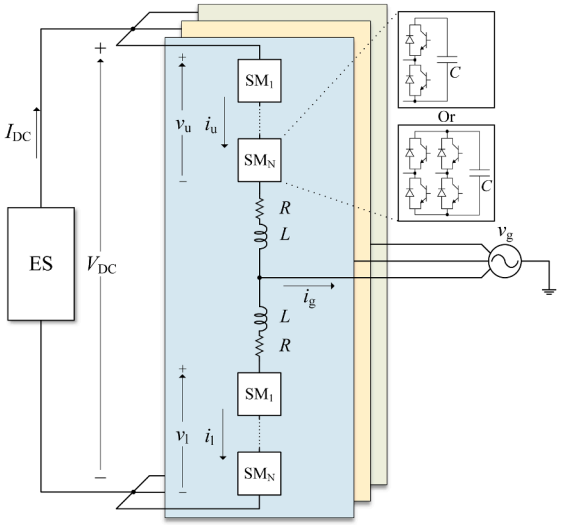

Fig. 1. Grid-connected YY-MMC scheme.

converter, the circulating current is composed of a DC term, which is 1/3 of the DC current coming from the ES (I_{DC}), and even order harmonics that originate from the phase difference between the upper arm and lower arm capacitors' voltage ripples [21]. Therefore, the circulating current can be written as:

$$i_c = \frac{I_{DC}}{3} + \sum_{\substack{k=1 \\ (n=2k)}}^{k=\infty} I_{cn}\cos(k\omega t + \varphi_{cn}) \tag{3}$$

where I_{cn} and φ_{cn} are the amplitude and phase of the n^{th} harmonic of the circulating current. It can be found that the dominating harmonic component of the circulating current is the second order; higher-order harmonics have much smaller amplitude [21]. Thus, in this analysis, it is assumed that circulating current is composed of a DC term and a second-order harmonic component. Considering this and assuming that i_g is pure sinusoidal with fundamental frequency and amplitude I_g and phase φ_{ig}, the upper and lower arm currents can be found by combining (2) and (3)

$$i_{u,l} = \pm\frac{I_g}{2}\cos(\omega t + \varphi_{ig}) + \frac{I_{DC}}{3} + I_{c2}\cos(2\omega t + \varphi_{c2}) \tag{4}$$

3. Design parameters

This section discusses the key design parameters that influence the cost of the HB-YY-MMC and FB-YY-MMC, including the number of SMs (N), power losses (P_l), SM capacitance (C), and semiconductor current ratings (I_n or I_{RMS}). The relationships between these parameters and the pole-to-pole DC voltage (V_{DC}), second-order circulating current amplitude (I_{c2}) and phase (φ_{c2}), as well as active and reactive power ratings, are investigated.

3.1. Number of submodules

The number of submodules (SMs) for the HB-YY-MMC and FB-YY-MMC configurations is determined by dividing the arm design voltage by the rated voltage of a single SM [22]. The arm design voltage is defined as:

$$V_{arm} = \frac{V_{DC}}{2} + 1.05\hat{V}_g\left(1 + \Delta V_g + I_{g,pu}\frac{Z_f}{2}\right) \tag{5}$$

where Z_f is the per-unit value of the arm filter impedance, $I_{g,pu}$ is the per-unit value of the output rated current (which is equal to 1), ΔV_g is the peak grid voltage variation, and $\hat{V}_g$ is the grid maximum voltage. It should be mentioned that in (5) a 5% margin is considered to guarantee

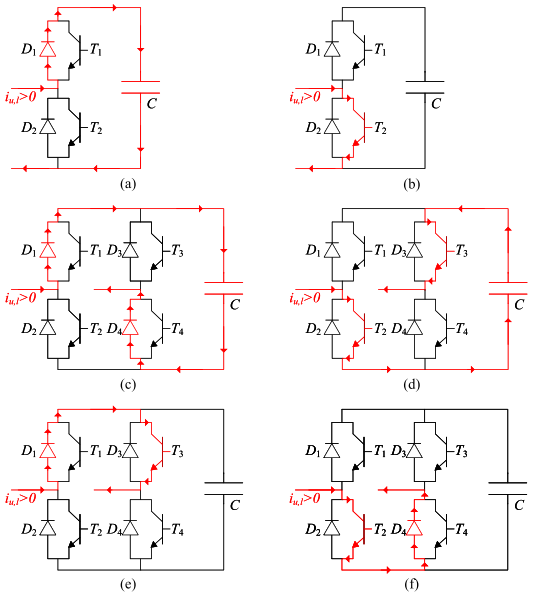

Fig. 2. Current path when HB SM is (a) inserted, and (b) bypassed or FB SM is (c) positively inserted, (d) negatively inserted, or (e) and (f) bypassed for positive arm current.

a suitable dynamic behavior in the current controller [4]. Considering (V_n) as the rated voltage of a single SM, the number of SMs is then determined as:

$$N = \text{ceil}\left(\frac{V_{arm}}{V_n}\right) \tag{6}$$

3.2. Power losses

The losses of a generic YY-MMC can be divided into three main parts: conduction and switching losses of the semiconductor devices, filter losses, and capacitance losses.

The conduction losses of a YY-MMC are due to the losses that occur in the transistors and diodes of the SMs when they are conducting. To calculate the instantaneous conduction losses of a single transistor and diode, they are usually modeled by an on-state voltage drop and an on-state resistor [23]. Defining p_{ct} and p_{cd} as the instantaneous conduction losses of a single transistor and diode, they are found to be:

$$\begin{aligned} p_{ct} &= V_{ce}i_{ce} + R_{ce}i_{ce}^2 \\ p_{cd} &= V_{f0}i_f + R_{f0}i_f^2 \end{aligned} \tag{7}$$

where V_{ce}, R_{ce}, V_{f0}, and R_{f0} are the on-state voltage drop and on-state resistance of the transistor and the diode, and i_{ce} and i_f are the transistor and diode currents. The conduction losses of the arm of the YY-MMC are dependent on the current path. The current path depends on the state of the switches, whether they are bypassed or inserted positively or negatively, and the direction of the current. Fig. 2 shows the current path for a single SM with different states of the switches and when the arm current is positive. The same practice can be repeated for the negative arm current. Table 2 summarizes all the possible cases for the conduction losses corresponding to each SM.

To calculate the total arm conduction losses, the number of inserted SMs should be determined; this is achieved by defining the upper and lower arm insertion indices as the following:

$$n_{u,l} = \frac{\frac{V_{DC}}{2} \mp V_s\cos(\omega t)}{V_C^{\Sigma}} \tag{8}$$

where V_C^{Σ} is the DC value of the sum of the capacitor voltage of the arm of the YY-MMC. For a HB-YY-MMC, the insertion indices is a number

Table 2
Instantaneous conduction losses for all switching states under positive and negative current.

SM Type	SM State	Transistor losses		Diode losses	
		$i_{u,l} > 0$	$i_{u,l} < 0$	$i_{u,l} > 0$	$i_{u,l} < 0$
HB	Inserted	0	p_{ct}	p_{cd}	0
	Bypassed	p_{ct}	0	0	p_{cd}
FB	Inserted positively	0	$2p_{ct}$	$2p_{cd}$	0
	Inserted negatively	$2p_{ct}$	0	0	$2p_{cd}$
	Bypassed	p_{ct}	p_{ct}	p_{cd}	p_{cd}

between 0 and 1 and determines the ratio between the inserted SMs and the total number of SMs in arm. Moreover, V_C^{Σ} is usually selected to be equal to V_{DC} in a HB-YY-MMC [21,22]. On the other hand, the insertion indices for a FB-YY-MMC is a number between −1 and 1, where negative values of the insertion indices mean that the SMs are inserted negatively.

From Table 2, the individual SM conduction losses can be calculated. Taking into account that the number of inserted SMs in an arm of the YY-MMC is $N|n_{u,l}|$, while the number of bypassed SMs is $N - N|n_{u,l}|$, the total arm conduction losses occurring in transistors and diodes of a HB-YY-MMC and FB-YY-MMC are found to be:

$$p_{ct,HB} = \begin{cases} N(1-|n_{u,l}|)(V_{ce}|i_{u,l}| + R_{ce}i_{u,l}^2) & i_{u,l} \geq 0 \\ N|n_{u,l}|(V_{ce}|i_{u,l}| + R_{ce}i_{u,l}^2) & i_{u,l} < 0 \end{cases}$$

$$p_{cd,HB} = \begin{cases} N|n_{u,l}|(V_{f0}|i_{u,l}| + R_{f0}i_{u,l}^2) & i_{u,l} \geq 0 \\ N(1-|n_{u,l}|)(V_{f0}|i_{u,l}| + R_{f0}i_{u,l}^2) & i_{u,l} < 0 \end{cases} \quad (9)$$

$$p_{ct,FB} = \begin{cases} N(1-|n_{u,l}|)(V_{ce}|i_{u,l}| + R_{ce}i_{u,l}^2) & n_{u,l}i_{u,l} \geq 0 \\ N(1+|n_{u,l}|)(V_{ce}|i_{u,l}| + R_{ce}i_{u,l}^2) & n_{u,l}i_{u,l} < 0 \end{cases}$$

$$p_{cd,FB} = \begin{cases} N(1+|n_{u,l}|)(V_{f0}|i_{u,l}| + R_{f0}i_{u,l}^2) & n_{u,l}i_{u,l} \geq 0 \\ N(1-|n_{u,l}|)(V_{f0}|i_{u,l}| + R_{f0}i_{u,l}^2) & n_{u,l}i_{u,l} < 0 \end{cases} \quad (10)$$

The total conduction losses of the HB-YY-MMC and FB-YY-MMC in steady-state are found by averaging the sum of the instantaneous conduction losses of the transistor and diode and multiplying it by the number of arms as following:

$$P_{co,HB} = \frac{6}{T}\int_T (p_{ct,HB} + p_{cd,HB})\,dt$$
$$P_{co,FB} = \frac{6}{T}\int_T (p_{ct,FB} + p_{cd,FB})\,dt \quad (11)$$

The switching losses of the YY-MMCs are due to the switching of the transistors and diodes and are composed of three main contributions: transistor turn-on loss, transistor turn-off loss, and diode reverse recovery loss. The switching losses are highly dependent on the adopted modulation technique and SM-balancing strategy. Here, the switching losses due to essential switching, as defined in [24] are considered. Assuming the Nearest Level Modulation (NLM), the number of inserted SMs and the number of switching in the fundamental period is found to be round($Nn_{u,l}$) and $2N$. Enery dissipated during switching at time instance t_k are defined as $E_{sw}(t_k)$, and are dependent on the amplitude and the direction of the current, and the switching state. For example, Fig. 3 shows the current path for three cases in which, an HB SM is bypassed from an inserted state and vice-versa or a FB SM is bypassed from a positively or negatively inserted state and vice-versa. It can be seen from Fig. 3(a) that when the state of the HB SM is changed from inserted to bypassed, the switching losses are due to the reverse recovery loss of diode D_1 and turn-on loss of transistor T_2. Furthermore, Fig. 3(b) shows that when the state of the FB SM varies from a positively inserted state to any of the bypassed states, the associated switching loss is due to turn-on loss of transistor T_3 (or T_2) and reverse recovery loss of diode D_4 (or D_1). Also, from Fig. 3(c) it can be seen that when it switches from a negatively inserted state to any of the bypassed states, the switching loss is due to turn-off loss of transistor T_2 or T_3.

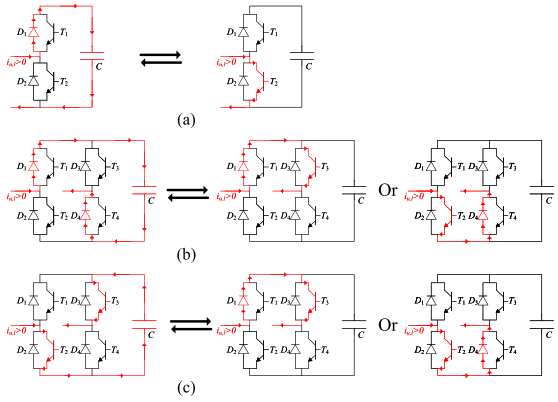

Fig. 3. Current path for (a) HB SM transition between inserted and bypassed states (b) FB SM transition between positively inserted and bypassed states and (c) FB SM transition between negatively inserted and bypassed states.

Table 3
SM switching dissipated energy as a function of switching state and current direction.

SM Type	$n_{u,l}$	$i_{u,l}$	$\frac{d\,\text{round}(Nn_{u,l})}{dt}$	Dissipated energy
HB	+	+	−	$E_{rec} + E_{on}$
	+	−	−	E_{off}
	+	+	+	E_{off}
	+	−	+	$E_{rec} + E_{on}$
FB	+	+	−	$E_{rec} + E_{on}$
	+	−	−	E_{off}
	+	+	+	E_{off}
	+	−	+	$E_{rec} + E_{on}$
	−	+	−	$E_{rec} + E_{on}$
	−	−	−	E_{off}
	−	+	+	E_{off}
	−	−	+	$E_{rec} + E_{on}$

The same analysis can be repeated for all the switching states and current direction and has been reported in Table 3, where E_{rec} is the reverse recovery loss of the diode, and E_{on} and E_{off} are the turn-on and turn-off loss of the transistor, which are found from the semiconductor device datasheet. It should be noted that in Table 3 the switching state is shown as the rate of change in the number of inserted SMs or $\frac{d\left(\text{round}(Nn_{u,l})\right)}{dt}$. A positive rate happens when SM is either being bypassed from a negatively inserted state or being inserted positively from a bypassed state. Conversely, a negative rate means that the SM is either being bypassed from a positively inserted state or being inserted negatively from a bypassed state.

From Table 3, it can be seen that the switching losses for an HB or FB SM at the switching instant t_k can be found from the same equation which is:

$$E_{sw}(t_k) = \begin{cases} E_{rec}(t_k) + E_{on}(t_k) & i_{u,l}\frac{d\left(\text{round}(Nn_{u,l})\right)}{dt} < 0 \\ E_{off}(t_k) & i_{u,l}\frac{d\left(\text{round}(Nn_{u,l})\right)}{dt} > 0 \end{cases} \quad (12)$$

The total switching losses of the HB-YY-MMC and FB-YY-MMC is calculated by summing the switching losses of the SMs in an arm of the HB-YY-MMC and FB-YY-MMC and multiplying it by the number of arms.

$$P_{sw} = \frac{6}{T}\sum_{k=1}^{2N} E_{sw}(t_k) \quad (13)$$

The filter losses (P_{fi}) are found by calculating the losses in the resistance of the filter. Taking into account a filter resistance of R as shown in Fig. 1 and calculating the Root Mean Square (RMS) of the arm current

in (4), the filter losses for the HB-YY-MMC and FB-YY-MMC are found to be:

$$P_{\mathrm{fi}} = 6RI^2_{\mathrm{u,l,RMS}} = R\frac{8I^2_{\mathrm{DC}} + 9Ig^2 + 36I^2_{c2}}{12} \tag{14}$$

Finally, to find the capacitance losses, the averaging principle introduced in [9] is deployed. Assuming the SM's capacitance losses are modeled by resistance R_{c}, the converter's capacitance losses are found by calculating the RMS current flowing through the Series Equivalent Capacitance (ESR) of the arm. According to [9] and [19], this current is equal to multiplication of the insertion indices, in (8), by the arm current in (4). Thus, the HB-YY-MMC and FB-YY-MMC capacitance losses are calculated as:

$$\begin{aligned} P_{\mathrm{ca}} =& \frac{6NR_{\mathrm{c}}}{T}\int_T (n_{\mathrm{u,l}} i_{\mathrm{u,l}})^2\,dt = NR_{\mathrm{c}}\Bigg(\frac{16m^2_{\mathrm{AC}}I^2_{\mathrm{DC}}}{192} \\ &+ \frac{9(4m^2_{\mathrm{DC}} + m^2_{\mathrm{AC}})I^2_{\mathrm{g}} + 72(2m^2_{\mathrm{DC}} + m^2_{\mathrm{AC}})I^2_{c2}}{192} \\ &+ \frac{-144m_{\mathrm{AC}}m_{\mathrm{DC}}\cos(\varphi_{\mathrm{ig}} - \varphi_{c2})I_{\mathrm{g}}I_{c2}}{192} \\ &+ \frac{+48m_{\mathrm{AC}}\left(m_{\mathrm{AC}}\cos(\varphi_{c2})I_{c2} - m_{\mathrm{DC}}\cos(\varphi_{\mathrm{ig}})I_{\mathrm{g}}\right)I_{\mathrm{DC}}}{192}\Bigg) \end{aligned} \tag{15}$$

where $m_{\mathrm{AC}} = \frac{2V_{\mathrm{s}}}{V^{\Sigma}_{\mathrm{C}}}$ and $m_{\mathrm{DC}} = \frac{V_{\mathrm{DC}}}{V^{\Sigma}_{\mathrm{C}}}$ are the AC and DC modulation index, respectively.

The total losses of HB-YY-MMC and FB-YY-MMC are found by summing the losses in (11), (13), (14), and (15).

$$\begin{aligned} P_{\mathrm{l,FB}} &= P_{\mathrm{co,FB}} + P_{\mathrm{sw,FB}} + P_{\mathrm{fi,FB}} + P_{\mathrm{ca,FB}} \\ P_{\mathrm{l,HB}} &= P_{\mathrm{co,HB}} + P_{\mathrm{sw,HB}} + P_{\mathrm{fi,HB}} + P_{\mathrm{ca,HB}} \end{aligned} \tag{16}$$

3.3. Semiconductor rating

The rated current of the semiconductors for the FB-YY-MMC and HB-YY-MMC configurations is determined by the peak of the current flowing through them. Therefore, assuming steady-state operation in (4), the semiconductor rated current is calculated as in (17).

$$I_{\mathrm{n}} = \max\left(\left|\frac{I_{\mathrm{g}}}{2}\cos(\omega t + \varphi_{\mathrm{ig}}) + \frac{I_{\mathrm{DC}}}{3} + I_{c2}\cos(2\omega t + \varphi_{c2})\right|\right) \tag{17}$$

Alternatively, the rated current of the semiconductor can also be determined by the RMS value of the current flowing through the semiconductor device as:

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{T}\int_T (i_{\mathrm{u,l}})^2\,dt} = \sqrt{\frac{I^2_{\mathrm{g}}}{4} + \frac{I^2_{\mathrm{DC}}}{9} + \frac{I^2_{c2}}{2}} \tag{18}$$

3.4. Submodule capacitor size

The size of the SM capacitance is obtained by finding the peak-to-peak value of the arm energy variation and setting a threshold for the capacitor's voltage ripple (ΔV). The arm energy variation is calculated by integrating the multiplication of the arm voltage in (1) and arm current in (4), and is found to be:

$$\begin{aligned} w_{\mathrm{u,l}} =& \int_T v_{\mathrm{u,l}} i_{\mathrm{u,l}}\,dt = \pm\frac{V_{\mathrm{DC}}I_{\mathrm{g}}}{4\omega}\sin(\omega t + \varphi_{\mathrm{ig}}) \mp \frac{V_{\mathrm{s}}I_{\mathrm{DC}}}{3w}\sin(\omega t) \\ &\mp \frac{V_{\mathrm{s}}I_{c2}}{2\omega}\sin(\omega t + \varphi_{c2}) + \frac{V_{\mathrm{DC}}I_{c2}}{4\omega}\sin(2\omega t + \varphi_{c2}) \\ &- \frac{V_{\mathrm{s}}I_{\mathrm{g}}}{8\omega}\sin(2\omega t + \varphi_{\mathrm{ig}}) \mp \frac{V_{\mathrm{s}}I_{c2}}{6\omega}\sin(3\omega t + \varphi_{c2}) \end{aligned} \tag{19}$$

Defining the peak-to-peak value of the variation of the arm energy as:

$$W_{\mathrm{u,l}} = \max(w_{\mathrm{u,l}}) - \min(w_{\mathrm{u,l}}) \tag{20}$$

The SM capacitance value is then calculated as [19]:

$$C = \frac{W_{\mathrm{u,l}}}{N\Delta V V^2_{\mathrm{n}}} \tag{21}$$

where V_{n} is the SM rated voltage.

Table 4
Base-case cost contributions for HB-YY-MMC (normalized to $J_{\mathrm{b}} = 1$ pu).

Term	Value [pu]	Description
$J_{0,b}$	0.30	Fixed mechanical frame and base cooling cost.
$J_{1,b}$	0.10	SM mechanical structure and SM-level cooling.
$J_{2,b}$	0.15	Installation-area cost associated with accommodating all SMs.
$J_{3,b}$	0.05	Semiconductor rating cost based on RMS current requirement.
$J_{4,b}$	0.20	SM capacitor energy-storage cost derived from required arm energy.
$J_{5,b}$	0.20	Lifetime loss-related cost computed from the operational profile.

4. Design optimization

In this section, the design optimization of the FB-YY-MMC and HB-YY-MMC, formulated as a multi-objective optimization problem, is thoroughly investigated. This optimization problem considers the design parameters introduced in Section 3, namely the number of SMs (N), power losses (P_{l}), semiconductor rating (I_{n} or I_{RMS}), and SM capacitor (C or $W_{\mathrm{u,l}}$), as the objective functions. The pole-to-pole DC voltage (V_{DC}), the second-order circulating current amplitude (I_{c2}), and its phase (φ_{c2}) are treated as decision variables. As discussed in Section 2, V_{DC} can be considered a decision variable. In the HB-YY-MMC, its feasible range is limited by the inability of HB SMs to generate negative voltage. Therefore, the DC-link voltage must satisfy $V_{\mathrm{DC}} \geq 2$ pu.

A central factor in the optimization is the active-power capability, defined as the ratio of rated active power P_{r} to rated reactive power Q_{r} for a given converter rating. This parameter determines the intended application of the YY-MMC and influences the optimal design; in particular:

- STATCOM operation: $P_{\mathrm{r}}/Q_{\mathrm{r}} = 0$, representing a special case with purely reactive power support.
- E-STATCOM operation: enabling reactive power support with limited active-power capability, corresponding to energy storage functionality with restricted energy exchange.
- Energy storage applications: requiring high active-power exchange and higher energy capacity.

To ensure a consistent comparison between the two converter configurations, a base-case cost reference is defined as an HB-YY-MMC operating with fully suppressed circulating current and an active-power capability of $P_{\mathrm{r}}/Q_{\mathrm{r}} = 0.3$ in capacitive mode. This rating is representative of typical E-STATCOM applications, where reactive power support is dominant and only limited active power exchange is required.

The base-case cost is decomposed into the six components used in the general cost formulation, denoted $J_{0,b}$ through $J_{5,b}$, and summarized in Table 4. These represent, respectively, the fixed structural cost, SM mechanical cost, installation-area cost, semiconductor rating cost, capacitor energy-storage cost, and losses cost.

The total cost of the base case is defined as the sum of these contributions and is normalized to 1 pu:

$$J_{\mathrm{b}} = J_{0,b} + J_{1,b} + J_{2,b} + J_{3,b} + J_{4,b} + J_{5,b} = 1\ \mathrm{pu}. \tag{22}$$

The distribution of the base-case cost contributions reflects typical converter cost breakdowns reported in the literature [25,26]. While these sources provide indicative references for the relative significance of structural, semiconductor, capacitor, and loss-related costs, the final shares listed in Table 4 have been adapted to better reflect practical large-scale MMC implementations.

In particular, the loss-related contribution $J_{5,b}$ corresponds to the net present cost of converter power losses evaluated over a 25-year

Table 5
Converter specifications and base values.

Parameter	Symbol	Value
Grid voltage (L–L)	V_g	33 kV
Grid frequency	f	50 Hz
Rated (base) power	S_b	112 MVA
Arm filter impedance	Z	0.15 pu
Arm filter X/R ratio	X/R	20
Maximum capacitor voltage ripple	ΔV	10%
SM capacitor ESR	R_c	20 $\mu\Omega$
Semiconductor breakdown voltage	V_{bk}	4500 V
Semiconductor 100 FIT voltage*	V_{100FIT}	2500 V
Transistor on-state voltage drop	V_{ce}	0.8 V
Transistor on-state resistance	R_{ce}	0.7 mΩ
Diode forward voltage drop	V_{f0}	0.9 V
Diode forward resistance	R_{f0}	0.4 mΩ

* Nominal voltage corresponding to 100 FIT (100 failures in 10^9 hours) [28].

operating period, assuming an electricity cost of 10 k€/kW, which represents a typical European value [27]. The converter is not assumed to operate continuously at rated capacity; instead, a representative operational profile is considered. Specifically, the converter operates in idle mode for 40% of the time, injects 20% of its rated apparent power for 20% of the time, absorbs 20% of its rated apparent power for 20% of the time, and injects 60% of its rated apparent power during the remaining 20% of the operating period.

The general cost function used for optimization is constructed by scaling the normalized base-case contributions of Table 4 according to the actual converter design variables. Each cost component is assumed to scale with its corresponding physical quantity, resulting in the following expression:

$$J = J_{0,b} + J_{1,b}\frac{N}{N_b} + J_{2,b}\frac{N}{N_b} + J_{3,b}\frac{N\,I_{\mathrm{RMS}}}{N_b I_{\mathrm{RMS},b}} + J_{4,b}\frac{W_{\mathrm{u,l}}}{W_b} + J_{5,b}\frac{P_{\mathrm{l}}}{P_{l,b}} \tag{23}$$

Here, the subscript b denotes quantities corresponding to the base-case configuration. By construction, the cost function evaluates to $J = 1$ pu for the base case.

It should be noted that the base-case cost distribution corresponds to the HB-YY-MMC configuration. For the FB-YY-MMC, the same normalized base contributions are used, except that the mechanical and semiconductor-related components scale differently due to the structural differences of FB SMs. In particular, the SM mechanical contribution scales approximately 30% higher for FB-YY-MMC due to the increased physical size and cooling requirements of FB SMs [25,26]. Likewise, the semiconductor-related contribution scales by a factor of two, as each FB SM contains twice the number of semiconductor devices compared to a half-bridge SM.

Using the normalized cost contributions from Table 4, the general cost function in (23) is evaluated for a range of active-power capabilities (P_r/Q_r) as follows.

First, each cost component $J_{i,b}$ is scaled according to the actual converter design variables (number of SMs N, arm energy W, RMS current I_{RMS}, and losses P_l) relative to the base case, ensuring that $J = 1$ pu for the base-case configuration.

For each P_r/Q_r, the decision variables V_{DC}, I_{c2}, and φ_{c2} are optimized using Particle Swarm Optimization algorithm [29] to minimize the total cost J for both HB-YY-MMC and FB-YY-MMC. The rated apparent power is 1 pu, while P_r/Q_r is swept from -1 to 1 in two scenarios: capacitive (injection) and inductive operation (absorption).

At each point, the optimized decision variables are used to compute the corresponding cost. The resulting curves, shown in Fig. 4, represent the minimized cost as a function of P_r/Q_r, illustrating how the optimal cost of each converter topology changes with active-power capability.

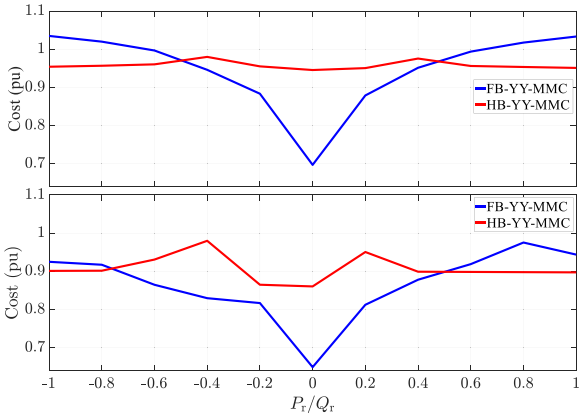

Fig. 4. Optimized cost of HB-YY-MMC and FB-YY-MMC as a function of the ratio between rated active and reactive power, presented for capacitive (top) and inductive (bottom) rated reactive power.

In this way, Fig. 4 explicitly links Table 4 and (23) to the final optimized cost results.

The lower limit of the DC-link voltage is constrained by both topology and practical device ratings. For the HB-YY-MMC, V_{DC} must satisfy $V_{\mathrm{DC}} \geq 2$ pu due to the inability of half-bridge SMs to generate negative voltage, as discussed in Section 2.

In the FB-YY-MMC, no such topological limitation exists, and V_{DC} can theoretically take lower values. However, reducing V_{DC} increases the DC current, which may exceed the rating of the semiconductor devices. The peak arm current is determined from (17) and consists of three main components: the DC current, the fundamental AC current from the grid, and the second-order circulating current. If V_{DC} is too low, I_{DC} becomes excessive, potentially violating device limits. For instance, for a system with specifications listed in Table 5 and a rated active power of 50 MW, the lowest feasible V_{DC} is calculated to be approximately 0.17 pu when the semiconductor device with the highest current rating reported in [30] is used.

The same principle applies to the second-order circulating current amplitude I_{c2}: it must be limited to avoid exceeding the available device current rating. Additional assumptions in the analysis also constrain I_{c2}; for example, the circulating current is assumed to consist only of the DC and second-order components, and the arm voltage model in (1) neglects the voltage injected by the circulating current controller. Exceeding these limits would invalidate the assumptions, introduce additional even-order harmonics [21], and require higher arm and SM voltages to inject large second-order currents. Consequently, the second-order circulating current is limited to 0.2 pu in the proposed optimization framework.

It can be observed from Fig. 4 that the cost of the HB-YY-MMC shows only moderate variation as P_r/Q_r changes. In contrast, the cost of FB-YY-MMC exhibits significant variations when changing the ratio P_r/Q_r. Specifically, it can be observed that the cost decreases when the reactive power is dominant. This is because, as shown in [19], a lower V_{DC} leads to a reduction in the required SM capacitor size. Additionally, a lower V_{DC} reduces the number of SMs, as indicated by (6), further lowering the cost of the FB-YY-MMC. At the same time, a decrease in V_{DC} leads to an increase of the losses and semiconductor ratings as I_{DC} rises. Nevertheless, when the active power is not significant, this increase is relatively small compared to the cost reduction in SMs and capacitors. It is evident that when the rated active power is 0 (indicating the exchange of reactive power only), the cost for both configurations reaches its minimum. This is due to zero active-power injection with minimal DC current drawn from the DC side, where the losses and semiconductor cost decreases.

To illustrate the impact of the proposed optimization framework, the active-power capability is set to $P_r/Q_r = 0.3$ (capacitive mode),

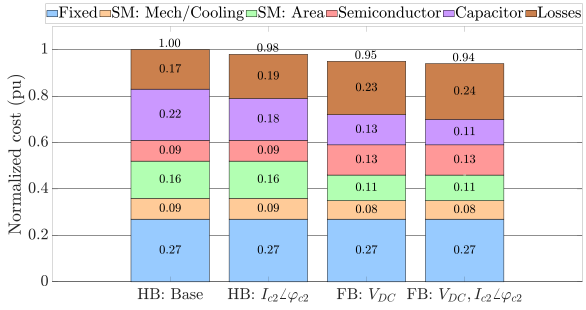

Fig. 5. Normalized cost of two configurations of MMC for base case and three different optimization scenarios with cost contribution of design parameters when $P_r/Q_r = 0.3$ in capacitive mode of operation.

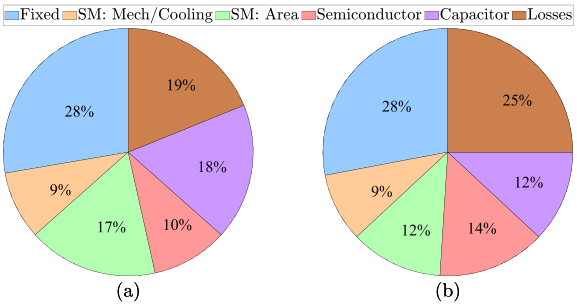

Fig. 6. Contribution of different design parameters in cost of (a) HB-YY-MMC and (b) FB-YY-MMC when active and reactive power ratings are set at $P_r/Q_r = 0.5$.

corresponding to a rated active power of 32 MW and a rated reactive power of 107 MVar, which is considered here just as example. The HB-YY-MMC operating at this power rating with fully suppressed circulating current is taken as the base case for normalization.

The cost function in (23), constructed from the base-case contributions in Table 4, is optimized for both FB-YY-MMC and HB-YY-MMC under the following scenarios:

1. HB-YY-MMC with V_{DC} fixed at 2 pu, optimized using the circulating current amplitude and phase.
2. FB-YY-MMC optimized using only the pole-to-pole DC voltage as the decision variable.
3. FB-YY-MMC optimized using both V_{DC} and the amplitude and phase of the second-order circulating current.

The results of these optimizations are visualized in Fig. 5 as a stacked-bar chart, where each bar represents the normalized total cost and is divided into contributions from SM capacitor energy, semiconductor rating, losses, and number of SMs.

The cost reductions achieved are as follows: for the FB-YY-MMC, using only V_{DC} reduces the total cost by approximately 5% relative to the base case, primarily by decreasing the SM capacitor and SM count contributions. Including I_{c2} and φ_{c2} as additional decision variables achieves a further 1% reduction. For the HB-YY-MMC, optimizing the circulating current amplitude and phase decreases the total cost by around 2%, mainly by reducing the capacitor contribution, while the loss-related component slightly increases. It can be observed that optimizing V_{DC} provides the largest reduction in cost, while adjusting the circulating current results in smaller improvements, indicating that V_{DC} is the more effective variable for YY-MMC design optimization.

It should be noted that for lower active-power capabilities, i.e., when the rated active power is small compared to the reactive power, the difference in cost between FB-YY-MMC and HB-YY-MMC increases, further favoring the FB-YY-MMC configuration. Overall, Fig. 5 demonstrates how the optimization of V_{DC}, I_{c2}, and φ_{c2} can systematically reduce the total cost while providing insight into the contribution of the considered design parameter.

One intersection point between the cost of the HB-YY-MMC and FB-YY-MMC in Fig. 4 occurs at a P_r/Q_r ratio of 0.5, where the costs of both configurations are equal. A detailed breakdown of the cost contributions from each design parameter at this power rating is illustrated in Fig. 6. In addition, Table 6 presents the selected decision variables that result in the optimal design for each configuration at this power rating, along with the corresponding values of the design parameters. It should be noted that in Table 6, V_{DC} and I_{c2} are normalized based on V_s and $I_g/2$, respectively.

The numerical values reported in Table 6 are obtained by evaluating the cost function in (23) for the specified $P_r/Q_r = 0.5$, where the decision variables V_{DC}, I_{c2}, and φ_{c2} are optimized to minimize the total cost for each MMC configuration. These values correspond to the optimal settings for the chosen active and reactive power scenario.

From Fig. 6 and Table 6, it can be seen that the FB-YY-MMC achieves lower cost primarily through a reduced pole-to-pole DC voltage, which decreases the number of required SMs and thereby lowers the total SM-related cost. As discussed in [19], a lower DC voltage also reduces the required SM capacitor size, further contributing to the cost reduction. However, this benefit is accompanied by higher arm currents, which increase both conduction losses and semiconductor-related cost contributions. Consequently, the FB-YY-MMC tends to be more cost-effective in applications deployed in regions with relatively low electricity prices, where the lifetime loss-related contribution $J_{5,b}$ is reduced relative to the SM- and capacitor-related cost components. Moreover, in cases where the optimized cost values for both topologies are equal or similar, the FB-YY-MMC remains the preferred choice, as it additionally provides inherent DC short-circuit handling capability [22].

Based on the optimized cost results illustrated in Figs. 4–6 a practical guideline for topology selection can be inferred. For low active-power capability ($P_r/Q_r \lesssim 0.5$), where reactive power dominates, the FB-YY-MMC configuration yields a lower total cost due to reduced SM count and capacitor requirements. Conversely, for high active-power capability ($P_r/Q_r \gtrsim 0.5$), the HB-YY-MMC becomes more cost-effective. Note that these observations refer primarily to positive P_r/Q_r values, representing active power injection; negative ratios follow a slightly different trend but are less relevant for typical operation. Therefore, for a given set of operational and economic conditions, the selection of the MMC topology can be systematically guided by the active-power capability: FB-YY-MMC is preferred for predominantly reactive-power applications (e.g., STATCOM or low active-power E-STATCOM operation), while HB-YY-MMC is advantageous for applications requiring substantial active-power delivery, such as energy storage integration. These guidelines take into account typical electricity cost assumptions, operational requirements, and the normalized cost contributions of each design parameter.

Since the cost evaluation relies on an assumed base-case cost distribution that reflects typical converter implementations, it is important to assess how sensitive the optimization results are to variations in these assumptions. To this end, a sensitivity analysis of the cost contributions is performed for both configurations. Fig. 7 illustrates how the total cost varies when each normalized base-case contribution in Table 4 is individually perturbed by −20% to +20%, while the remaining contributions are held constant. It can be observed that, aside from the fixed structural cost, the loss-related component exhibits the strongest influence on the overall cost for both configurations. This analysis verifies that the observed trends and topology preferences remain valid under different cost assumptions.

Table 6
Optimized MMC design parameters for $P_r/Q_r = 0.5$.

Config.	V_{DC}	I_{c2}	φ_{c2}	N	I_{RMS}	W	P_l
HB-YY-MMC	2.00	0.19	287	24	1.5	205.33	734.97
FB-YY-MMC	0.95	0.19	258	17	1.5	137.88	996.47

Units: I_{RMS} [kA], W [kJ], P_l [kW].

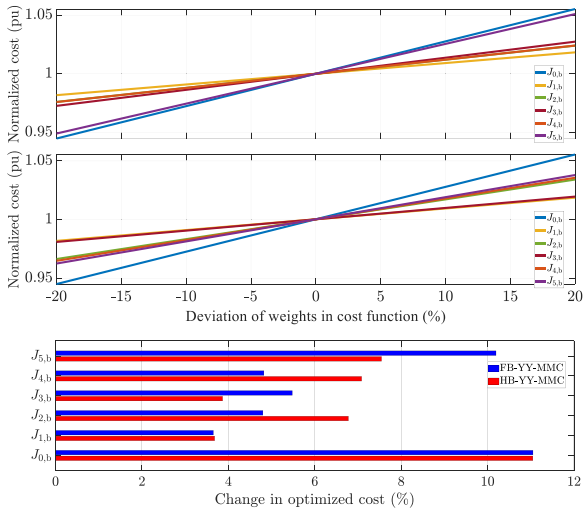

Fig. 7. Sensitivity analysis of the cost function with respect to the normalized base-case cost contributions. (Top) FB-YY-MMC and (Middle) HB-YY-MMC: Each curve shows the cost variation as one base-case contribution from Table 4 is varied from −20% to +20% of its nominal value, while the remaining contributions are held constant. (Bottom) Total cost change for each contribution ($\Delta J = J_{+20\%} - J_{-20\%}$) for both configurations.

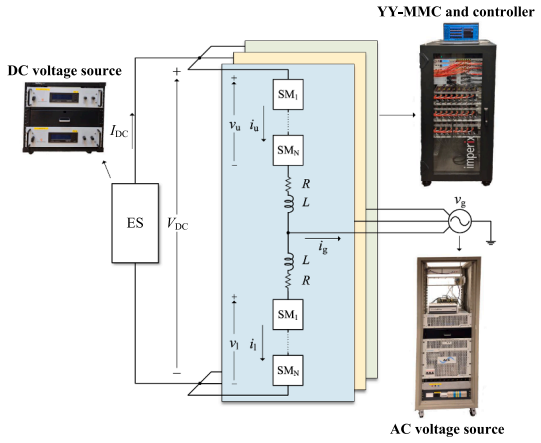

Fig. 8. Laboratory setup.

5. Experimental validation

In this section, the effectiveness of the proposed optimization approach is evaluated for both FB-YY-MMC and HB-YY-MMC configurations by analyzing two key design parameters: the SM capacitor and the semiconductor rating. The experiments are conducted using the setup shown in Fig. 8. In this setup, a REGATRON four-quadrant controllable AC power source emulates the grid, while an Imperix MMC bundle is used to implement the YY-MMC, with its SMs configurable as either FB or HB modules. A bi-directional Delta Elektronika SM1500-CP-30 DC power supply provides the pole-to-pole DC voltage. The complete specifications of the setup are presented in Table 7.

Table 7
Experimental setup parameters.

Parameter	Value
Base power	2000 VA
Grid voltage (L–L RMS)	200 V
Grid frequency	50 Hz
Filter inductance	2.3 mH
Filter resistance	60 mΩ
SM capacitor	5 mF
SM voltage	100 V

First, the effect of the pole-to-pole DC voltage on arm energy variation, as described in (20), is tested for the FB-YY-MMC when the circulating current is fully suppressed. The results for two power levels, $P = 0.5$ pu, $Q = 0.5$ pu; and $P = 0.1$ pu, $Q = 0.7$ pu, are shown in Fig. 9. The experimental results closely follow the trend of the theoretical predictions, confirming that for each power level there exists a pole-to-pole DC voltage that minimizes arm energy variation. It is noted that for the HB-YY-MMC, the optimal pole-to-pole DC voltage is approximately 2 pu; therefore, this test is not repeated for HB, as it is mainly used to validate FB trends. Fig. 10 also presents the waveform of the capacitor voltage ripple for a single SM capacitor at the two power levels, each with three different pole-to-pole DC voltages. The voltage ripple is minimized at the optimal pole-to-pole DC voltage (indicated by the red curves and as confirmed by Fig. 9), confirming that an optimal V_{DC}, always below 2 pu, results in a lower SM capacitance requirement.

The discrepancies between the theoretical and experimental results arise from practical nonidealities that are not considered in the simplified theoretical model. In particular, at lower V_{DC}, fewer SMs per arm are effectively contributing to the total AC voltage, resulting in a synthesized arm voltage with coarser steps. Additionally, for a given power level, lower V_{DC} leads to higher DC and arm currents, which magnify the effects of practical nonidealities such as conduction voltage drops, parasitic elements, and switching deadtime. Since the deviations introduced by these factors scale with current, the combined effect produces larger differences between experimental and theoretical arm voltages. These trends are consistent with observations reported in [31], where higher discrepancies were also observed at lower DC voltages.

In addition to the low V_{DC} effects, several other nonideal factors contribute to differences between experimental and theoretical results across all operating points. These include semiconductor forward voltage drops, inaccurate knowledge of the filter inductors, parasitic elements, switching deadtime, and variations in the AC source voltage. Such factors, identified in [31], are not captured by the theoretical model and further explain the remaining deviations observed in the experiments.

As V_{DC} increases, a larger number of SMs are inserted in each arm, and the DC and arm currents decrease for a given power level, improving the approximation of the arm voltage to the ideal waveform. Consequently, the experimental results converge more closely with the theoretical predictions at higher V_{DC} values.

Moreover, as mentioned, the theoretical analysis does not consider low-amplitude even-order circulating current harmonics, which are evident in the experimental results shown in Fig. 11. These deviations are expected to diminish in large-scale MMCs with a higher number of SMs.

The energy values in Fig. 9 are expressed in milliseconds (ms) because the arm energy is normalized by the system rating (VA), i.e., arm energy (J)/rating (VA), yielding a quantity with time units.

To further reduce the required capacitor size, the amplitude and phase of the second-order circulating current, previously discussed in earlier sections, can be adjusted. These parameters can also be used to reduce the peak arm current. Fig. 12 illustrates one SM capacitor voltage ripple for FB-YY-MMC at $P = 0.5$ pu and $Q = 0.5$ pu, with $V_{DC} = 1.21$ pu for three scenarios: (i) the circulating current is fully suppressed, (ii) it is

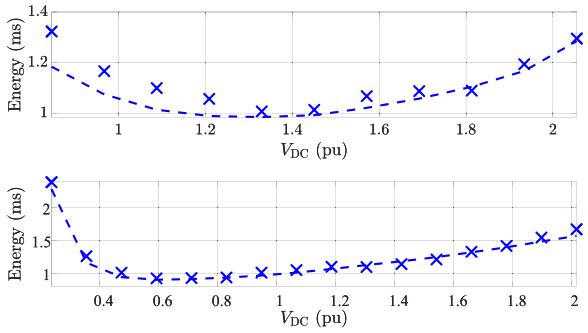

Fig. 9. Theoretical (dashed line) and experimental results (crosses) of the arm energy variation for FB operation when the circulating current is fully suppressed as a function of V_{DC} for $P = 0.5$ pu, $Q = 0.5$ pu (top), and $P = 0.1$ pu, $Q = 0.7$ pu (bottom).

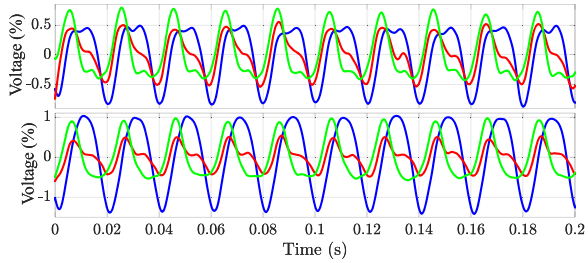

Fig. 10. Experimental results for FB operation, top: filtered capacitor voltage ripple of one SM (DC part removed) for $P = 0.5$ pu, $Q = 0.5$ pu, when $V_{DC} = 0.85$ pu (blue), $V_{DC} = 1.33$ pu (red), and $V_{DC} = 1.83$ pu (green), and bottom: $P = 0.1$ pu, $Q = 0.7$ pu, when $V_{DC} = 0.24$ pu (blue), $V_{DC} = 0.6$ pu (red), and $V_{DC} = 1.83$ pu (green).

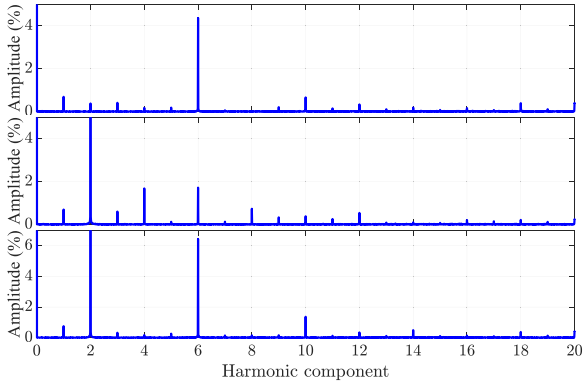

Fig. 11. Experimental results for the circulating current harmonic components for FB operation for $I_{c2}\angle\varphi_{c2} = 0$ pu (top), $I_{c2}\angle\varphi_{c2} = 0.12\angle 45°$ pu (middle), and $I_{c2}\angle\varphi_{c2} = 0.12\angle 225°$ pu (bottom).

optimized for capacitor size reduction, and (iii) it is optimized for peak arm current reduction.

The results indicate that optimizing the circulating current for capacitor size reduction decreases the peak-to-peak capacitor voltage ripple by 14% compared to the fully suppressed case. However, this comes at the cost of an 11% increase in the arm current peak. Conversely, optimizing the circulating current to reduce the arm peak current results in an 11% decrease in the arm current peak, but causes a 16% increase in the capacitor voltage ripple.

For the HB-YY-MMC, the power rating of $P = 0.1$ pu and $Q = 0.7$ pu is considered as an illustrative example. Three operating scenarios are examined, similar to the FB-YY-MMC: (i) circulating current fully suppressed, (ii) tuned to minimize capacitor voltage ripple, and (iii) tuned

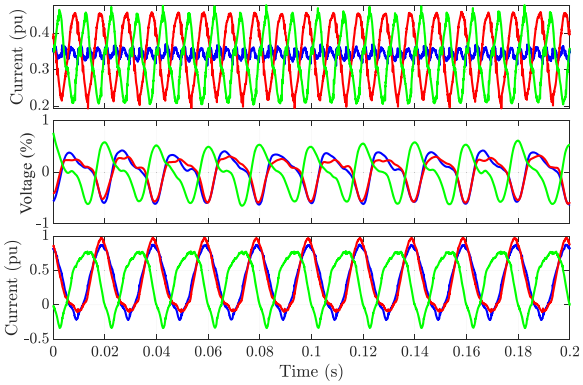

Fig. 12. Experimental results for FB operation, top: circulating current, middle: filtered capacitor voltage ripple of one SM (DC part removed), and bottom: arm current for $V_{DC} = 1.21$ pu, when $I_{c2}\angle\varphi_{c2} = 0$ pu (blue), $I_{c2}\angle\varphi_{c2} = 0.12\angle 45°$ pu (red), and $I_{c2}\angle\varphi_{c2} = 0.12\angle 225°$ pu (green).

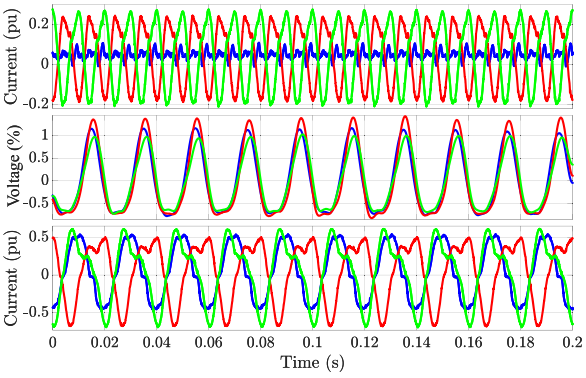

Fig. 13. Experimental results for HB operation, top: circulating current, middle: filtered capacitor voltage ripple of one SM (DC part removed), and bottom: arm current when $I_{c2}\angle\varphi_{c2} = 0$ pu (blue), $I_{c2}\angle\varphi_{c2} = 0.17\angle 135°$ pu (red), and $I_{c2}\angle\varphi_{c2} = 0.17\angle -45°$ pu (green).

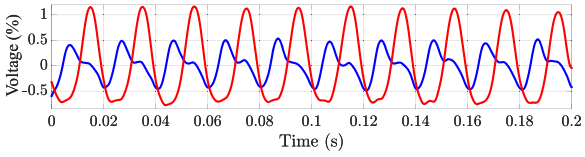

Fig. 14. Experimental results for filtered capacitor voltage ripple of one SM (DC part removed) for FB operation when $V_{DC} = 0.6$ pu (blue), and for HB operation when $V_{DC} = 2$ pu (red).

to reduce peak arm current. The experimental results, measured for the setup in Table 7 and shown in Fig. 13, validate the theoretical predictions for the arm peak current from (17) and the arm energy variation from (20). Adjusting the circulating current to minimize capacitor voltage ripple reduces the peak-to-peak ripple by 12%, accompanied by a 14% increase in the arm current peak. Conversely, tuning for peak arm current reduction decreases the arm current by 7%, while causing a 16% increase in the capacitor voltage ripple, illustrating the trade-offs between different objectives and motivating the need for a multi-objective optimization to achieve a balanced converter design.

These observations highlight the inherent trade-off between capacitor size and semiconductor current rating. It is important to note that, if (18) is used for optimization, the lowest semiconductor rating is achieved when the circulating current is fully suppressed. This further supports the conclusion that second-order circulating current has a limited impact on reducing the overall converter cost. These findings

further highlights the importance of full optimization as demonstrated in this paper.

Finally, Fig. 14 compares the arm energy variation for HB-YY-MMC and FB-YY-MMC at $P = 0.1$ pu and $Q = 0.7$ pu when the circulating current is fully suppressed. For the FB-YY-MMC, the pole-to-pole DC voltage corresponds to the optimized case for voltage ripple reduction. The figure confirms that FB-YY-MMC achieves significantly lower arm energy variation, demonstrating that this optimized voltage leads to smaller capacitor voltage ripples and consequently smaller required capacitance.

6. Conclusion

This paper presented a comprehensive optimization framework for the YY-MMC with energy storage, focusing on the HB-YY-MMC and FB-YY-MMC topologies. By formulating the design process as a multi-objective optimization problem, the study considered key design parameters, namely, the number of SMs, power losses, semiconductor rating, and SM capacitance, as objective functions. The pole-to-pole DC voltage and the amplitude and phase of the second-order circulating current were selected as decision variables.

The proposed cost function was optimized across varying rated active and reactive power exchange scenarios. The ratio between active and reactive power reflects the intended application of the converter in the grid and the type of services it is expected to provide, ranging from STATCOM operation focused on reactive-power support, to E-STATCOM operation with a mix of active and reactive power exchange, and up to applications involving substantial active-power delivery such as energy storage integration. The results showed that when the rated exchanged power is predominantly active, the HB-YY-MMC is the more favorable topology, leading to a lower value of the optimized cost function due to reduced semiconductor requirements and lower losses. In contrast, for predominantly reactive power exchange, the FB-YY-MMC becomes the better choice, offering benefits such as fewer SMs and reduced SM capacitance.

For power ratings where the optimized cost values for both topologies are equal or similar, the FB-YY-MMC is preferred, as it provides additional advantages such as DC short-circuit handling capability. Finally, experimental validations confirmed the effectiveness of the proposed optimization approach, and any discrepancies between the theoretical analysis and experimental results were identified and attributed to practical nonidealities.

CRediT authorship contribution statement

Sohrab Mohtat: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Project administration, Methodology, Investigation, Formal analysis, Data curation, Conceptualization; **Massimo Bongiorno:** Writing – review & editing, Visualization, Supervision, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization; **Mebtu Beza:** Writing – review & editing, Visualization, Validation, Supervision, Methodology, Investigation, Formal analysis, Conceptualization; **Jan R. Svensson:** Writing – review & editing, Supervision, Investigation, Formal analysis, Conceptualization; **Jon Rasmussen:** Writing – review & editing, Formal analysis, Data curation.

Data availability

No data was used for the research described in the article.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] S. Mohtat, M. Bongiorno, M. Beza, J. Svensson, Investigation of pole-to-pole DC voltage and circulating current on design requirements of full-bridge modular multilevel converter, in: Proc IEEE Energy Convers Congr Expo (ECCE), 2024, pp. 3296–3303. https://doi.org/10.1109/ECCE55643.2024.10860799

[2] M. Perez, S. Ceballos, G. Konstantinou, J. Pou, R. Aguilera, Modular multilevel converters: recent achievements and challenges, IEEE Open J. Ind. Electron. Soc. 2 (2021) 224–239. https://doi.org/10.1109/OJIES.2021.3060791

[3] H. Akagi, Classification, terminology, and application of the modular multilevel cascade converter (MMCC), in: Proc Int Power Electron Conf (ECCE Asia), 2010, pp. 508–515. https://doi.org/10.1109/IPEC.2010.5543243

[4] M. Vasiladiotis, A. Rufer, Analysis and control of modular multilevel converters with integrated battery energy storage, IEEE Trans. Power Electron 30 (1) (2015) 163–175. https://doi.org/10.1109/TPEL.2014.2303297

[5] A. July, M. Savaghebi, G. Li, N. Cutululis, Comparative analysis of grid-forming controls impact on stability of energy islands, in: Proc IEEE Int Power Electron Motion Control Conf, IEEE, 2024, pp. 1232–1237. https://doi.org/10.1109/IPEMC-ECCEAsia60879.2024.10567801

[6] G.A. Reddy, A. Shukla, Circulating current optimization control of MMC, IEEE Trans. Ind. Electron. 68 (4) (2021) 2798–2811. https://doi.org/10.1109/TIE.2020.2977565

[7] G.A. Reddy, N.P. Rao, A. Shukla, Improved circulating current control method to reduce energy storage and current rating requirements in MMC, IEEE Trans. Ind. Appl. 60 (5) (2024) 7182–7192. https://doi.org/10.1109/TIA.2024.3427050

[8] C.D. Townsend, et al., Identifying circulating currents and zero-sequence voltages for reduction in stored capacitor energy in modular multilevel converters, IEEE Trans. Ind. Electron. 68 (1) (2021) 454–465. https://doi.org/10.1109/TIE.2020.2965504

[9] K. Sharifabadi, et al., Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems, John Wiley & Sons, 2016.

[10] Q. Li, et al., A novel design of circulating current control target to minimize SM capacitance in MMC, Int J. Electr. Power Energy Syst. 143 (2022) 108432. https://doi.org/10.1016/j.ijepes.2022.108432

[11] R. Picas, et al., Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization, in: Proc IEEE ECCE Asia Downunder, 2013, pp. 318–324. https://doi.org/10.1109/ECCE-Asia.2013.6579115

[12] X. Xie, H. Li, H. Tan, Y. Wu, T. Yang, J. Zheng, W. Yang, A second-order harmonic circulating current injection method for MMC capacitance reduction in offshore DC wind turbine, Int. J. Electr. Power Energy Syst. 133 (2021) 107264. https://doi.org/10.1016/j.ijepes.2021.107264

[13] B. Li, et al., An improved circulating current injection method for modular multilevel converters in variable-speed drives, IEEE Trans. Ind. Electron. 63 (11) (2016) 7215–7225. https://doi.org/10.1109/TIE.2016.2547899

[14] L. Yang, Y. Li, Z. Li, P. Wang, S. Xu, R. Gou, Loss optimization of MMC by second-order harmonic circulating current injection, IEEE Trans. Power Electron. 33 (7) (2018) 5739–5753. https://doi.org/10.1109/TPEL.2017.2751068

[15] J. Zhao, et al., Harmonic circulating current injection based power loss optimization control of bottom switch/diodes for modular multilevel converters, CSEE J. Power Energy Syst. 7 (6) (2021) 1213–1226. https://doi.org/10.17775/CSEEJPES.2020.03110

[16] R. Chakraborty, A. Dey, Circulating current control of modular multilevel converter with reduced conduction loss for medium-voltage applications, IEEE Trans. Ind. Electron. 68 (10) (2021) 9014–9023. https://doi.org/10.1109/TIE.2020.3021641

[17] C. Zhao, Y. Li, Z. Li, P. Wang, X. Ma, Y. Luo, Optimized design of full-bridge modular multilevel converter with low energy storage requirements for HVDC transmission system, IEEE Trans. Power Electron. 33 (1) (2018) 97–109. https://doi.org/10.1109/TPEL.2017.2660532

[18] L. Baruschka, A. Mertens, Comparison of cascaded H-bridge and modular multilevel converters for BESS application, in: Proc IEEE Energy Convers Congr Expo (ECCE), 2011, pp. 909–916. https://doi.org/10.1109/ECCE.2011.6063868

[19] S. Mohtat, M. Bongiorno, M. Beza, J.R. Svensson, Impact of pole-to-pole DC voltage on energy requirement of FB YY-MMC, in: Proc Eur Conf Power Electron Appl (EPE ECCE Europe), 2023, pp. 1–8. https://doi.org/10.23919/EPE23ECCEEurope58414.2023.10264684

[20] C. Zhao, et al., Energy storage requirement optimization of hybrid modular multilevel converter with circulating current injection, IEEE Trans. Ind. Electron. 66 (9) (2019) 6637–6648. https://doi.org/10.1109/TIE.2018.2877088

[21] K. Ilves, A. Antonopoulos, S. Norrga, H. Nee, Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters, IEEE Trans. Power Electron. 27 (1) (2012) 57–68. https://doi.org/10.1109/TPEL.2011.2159809

[22] S. Chaudhary, A. Cupertino, R. Teodorescu, J. Svensson, Benchmarking of modular multilevel converter topologies for ES-STATCOM realization, Energies 13 (2020) 3384. https://doi.org/10.3390/en13133384

[23] U. Drofenik, J. Kolar, A general scheme for calculating switching and conduction losses of power semiconductors in numerical circuit simulations of power electronic systems, in: Proc Int Power Electron Conf, 2005.

[24] Z. Zhang, Z. Xu, Y. Xue, Valve losses evaluation based on piecewise analytical method for MMC-HVDC links, IEEE Trans. Power Deliv. 29 (3) (2014) 1354–1362. https://doi.org/10.1109/TPWRD.2014.2304724

[25] G. Wang, et al., A review of power electronics for grid connection of utility-scale battery energy storage systems, IEEE Trans. Sustain Energy 7 (4) (2016) 1778–1790. https://doi.org/10.1109/TSTE.2016.2586941

[26] G. Tsolaridis, H. Pereira, A. Cupertino, R. Teodorescu, M. Bongiorno, Losses and cost comparison of DS-HB and SD-FB MMC based large utility grade STATCOM, in: Proc IEEE Int Conf Environ Electr Eng, 2016, pp. 1–6. https://doi.org/10.1109/EEEIC.2016.7555715

[27] E. Commission, Commission staff working document: Impact assessment accompanying the proposal for a Council regulation on the Fuel Cells and Hydrogen 2 Joint Undertaking, Technical Report SWD(2013) 108 final, European Commission, 2013.

[28] B. Backlund, M. Rahimo, S. Klaka, J. Siefken, Topologies, voltage ratings and state of the art high power semiconductor devices for medium voltage wind energy conversion, in: Proc IEEE Power Electron Mach Wind Appl, 2009, pp. 1–6. https://doi.org/10.1109/PEMWA.2009.5208365

[29] J. Kennedy, R. Eberhart, Particle swarm optimization, in: Proc IEEE Int Conf Neural Netw, 1995, pp. 1942–1948.

[30] Hitachi Energy, STAKPAK™Power Semiconductors, 2023, (https://www.hitachienergy.com/products-and-solutions/semiconductors/stakpak.

[31] B. E., B. M., S.J. R., M. A, A novel capacitor-voltage balancing strategy for double-y statcom under unbalanced operations, IEEE Trans. Ind. Appl. 57 (3) 2692–2701.