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Deep Learning-Driven Inverse Design of Doherty Power Amplifiers Using Pixelated Combiners and Dual-State Impedance Synthesis

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***Abstract* — The output combiner of a Doherty power amplifier (PA) integrates load modulation, impedance matching, and phase compensation within a single network, making its design and synthesis highly challenging. In this paper, we propose a three-port Doherty combiner design methodology that combines deep convolutional neural networks (CNNs), pixelated layout representations, and genetic algorithms (GA) with dual-state impedance synthesis to address both peak and back-off power conditions. As a proof of concept, two GaN HEMT Doherty PA prototypes incorporating three-port pixelated combiners are designed and fabricated. Both prototypes achieve a measured saturated output power exceeding 44.2 dBm with peak drain efficiency above 71.2% within 2.6–2.8 GHz. Furthermore, a drain efficiency as high as 64% is measured at the 6-dB back-off level. After applying digital predistortion, each prototype achieves an adjacent channel leakage ratio (ACLR) better than -51.3 dBc.**

***Keywords* — CNN, combiner synthesis, deep learning, Doherty PA, energy efficiency, GaN, genetic algorism, load modulation.**

I. Introduction

The growing demand for higher data throughput in modern communication systems has driven the adoption of complex modulation schemes, resulting in signals with high peak-to-average power ratios (PAPR). To efficiently transmit these high-PAPR signals, power amplifiers (PA) must employ efficiency enhancement techniques such as load modulation. Among the various load-modulated PA architectures proposed both historically [1], [2] and in recent years [3], [4], [5], [6], [7], Doherty PAs remain one of the most attractive solutions due to their simple implementation, decent linearity, and excellent efficiency under back-off conditions.

A critical aspect of Doherty PA design is the synthesis of its output combiner network. This network must simultaneously provide essential functionality such as load modulation, impedance transformation, and phase compensation, while also maintaining low loss and compact size to achieve high efficiency and enable miniaturization. The traditional Doherty design approach relies on parameterized models with pre-selected topologies composed of lumped or distributed components, such as transmission lines, inductors, and capacitors, followed by optimization through electromagnetic (EM) parameter sweeps. While this approach can be effective, it is often iterative, time-consuming, and prone to converging on local optima.

In recent years, deep learning–based inverse design approaches using pixelated EM structures have gained traction in radio frequency (RF) circuit design, demonstrating potential for expanding the design space and reducing design time [8]. However, these methods have so far been largely limited to relatively simple PA architectures, such as wideband class B PAs [8], harmonic-tuned class F/F^{-1} PAs [9], [10], and template-based multi-layer differential PAs [11] etc. Applying deep learning techniques with pixelated layouts to the design of Doherty combiners has remained unexplored, owing to the inherent complexity of synthesizing three-port load-modulated networks. Nevertheless, this capability is highly desirable, as the combiner fundamentally governs Doherty PA behavior and ultimately sets the limits on achievable back-off efficiency.

In this paper, we introduce a dual-state impedance synthesis framework for efficient Doherty combiner design. A deep convolutional neural network (CNN)-based surrogate model is developed to capture the nonlinear relationships between pixelated layout structures and frequency-dependent S-parameters. Combined with a genetic algorithm (GA) for dual-state impedance optimization, this approach bridges the gap between deep learning-driven pixelated design and Doherty combiner synthesis, enabling rapid design space exploration and efficient Doherty network realization. The proposed methodology is validated through two GaN HEMT Doherty PA prototypes employing pixelated combiners, both achieving excellent measured performance.

II. Deep Learning-Driven Combiner Synthesis

In this study, circuit layouts are represented as binary matrices, where "1" indicates the presence of a metal pixel and "0" non-metal. The design area is discretized into a 15×15 grid, each cell sized $1.8\,\mathrm{mm} \times 1.8\,\mathrm{mm}$ (a pixel), with element size expanded by 20% to allow diagonal paths. Exhaustive exploration of all pixel combinations would require 2^{225} possibilities, making brute-force search infeasible. We, therefore, train a deep CNN based on pixelated layouts and their corresponding S-parameters to act as a fast EM surrogate model, delivering sub-millisecond predictions. Integrated with a GA, it enables rapid design-space exploration and generation of pixelated layouts that meet Doherty combiner specifications.

A. Data Generation, Model Architecture, and Training Details

To train the neural network, we first generate a dataset of approximately 75K circuits, later augmented to 600K samples. Each training circuit is created by assigning a random metal

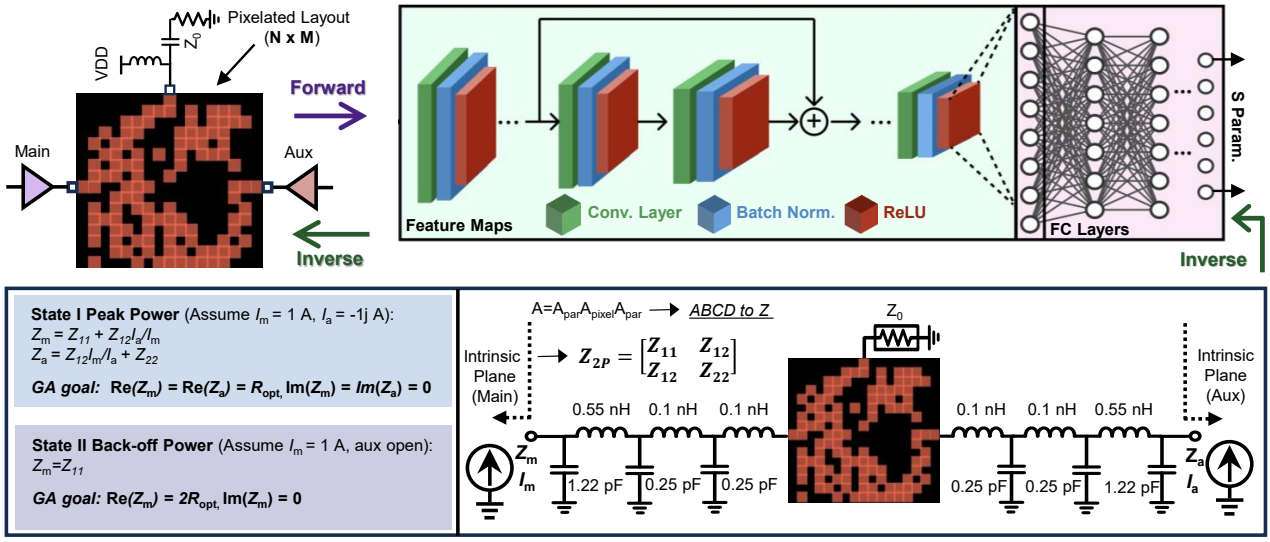

Fig. 1. Inverse design workflow for pixelated Doherty combiners using deep convolutional neural networks (CNN) and the proposed dual-state impedance synthesis approach integrated with genetic algorithms (GA).

coverage to the layout, drawn from a normal distribution centered at 50% with a 15% standard deviation. The initial data is then obtained through EM simulations in ADS Momentum, using frequencies within $2.4-3.0$ GHz with 0.05 GHz spacing. The layout includes four ports positioned at the center of each side, and during augmentation, one port is terminated with an open circuit while another is terminated with a 50 Ω load.

The employed deep CNN architecture is illustrated in Fig. 1. It begins with an input layer for the circuit matrices, followed by 12 convolutional blocks. Each block consists of 32 convolutional filters, and batch normalization layers. To address the vanishing gradient problem and improve stability, we incorporate a deep residual network structure [12]. After the convolutional layers, six fully connected (FC) layers are employed, each with 2048 neurons and dropout applied at a rate of 25% to prevent overfitting. Both convolutional and dense layers use Leaky ReLU (LeReLU) activations, enabling the network to learn complex nonlinear relationships. The output layer predicts the S-parameters, including real and imaginary parts, across 13 discrete frequencies within the 2.4–3.0 GHz range. The network is trained for 300 epochs using the mean absolute error (MAE) loss function and the Adam optimizer with a learning rate of 0.001.

B. Dual-State Doherty Combiner Synthesis

We use a GA to synthesize pixelated EM layouts based on target specifications. An initial population of binary matrices is generated, and in each generation, a CNN surrogate predicts S-parameters while fitness scores quantify deviation from the target. The top 10 individuals are retained as elites, while up to 30% of the population is replaced with random layouts. Parents are selected via tournament, and mutation flips pixels to introduce variability. This process evolves the population toward layouts that meet the desired performance.

A key challenge in Doherty combiner synthesis is defining targets that accurately represent Doherty operation. To address this, we propose a dual-state impedance synthesis method. The combiner is modeled as a three-port network: ports 1 and 2 connect to the main and auxiliary amplifiers, while port 3 is terminated with a 50 Ω load. Transistor parasitics and packaging elements are de-embedded and incorporated following the approach in [9]. The overall network is represented by cascaded ABCD matrices, which are then converted into an impedance matrix Z_{2P}, representing the pixelated combiner with parasitics. The impedance at the main and auxiliary current-source planes is expressed as

$$Z_m = Z_{11} + Z_{12}\frac{I_a}{I_m} \tag{1}$$

$$Z_a = Z_{22} + Z_{12}\frac{I_m}{I_a} \tag{2}$$

For different back-off levels, the ratio I_a/I_m varies. In this work, we consider a symmetrical Doherty configuration with two operating states:

- **State I (Peak Power):** At peak power, $|I_a| = |I_m|$ and $\angle(I_a, I_m) = 90°$, so
$$I_a = -jI_m$$
- **State II (Back-Off Power):** At back-off, the auxiliary PA is off ($I_a = 0$), giving
$$Z_m = Z_{11} \tag{3}$$

To synthesize the pixelated Doherty combiner, we first compute the Z_{2P} parameters. With three unknowns and three equations (1)–(3), the system can be solved. At peak power, the target impedance for both main and auxiliary amplifiers is $R_{opt} = (V_{BR} - V_{knee})/I_{max}$ and at back-off power, the main amplifier's impedance becomes $2R_{opt}$. Our GA goal is thus to ensure that, within $2.6 - 2.8$ GHz band:

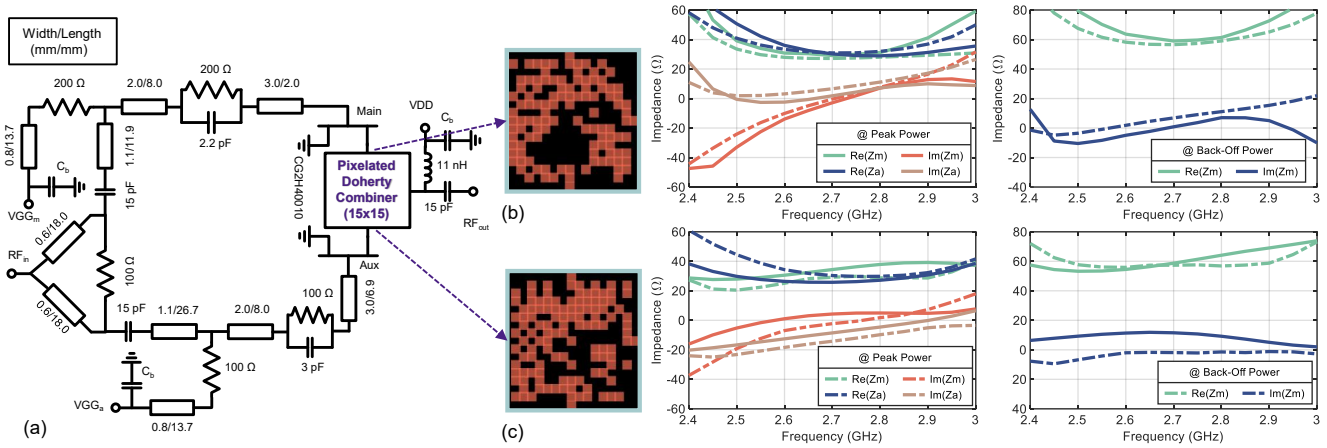

Fig. 2. (a) Circuit schematic of the proposed Doherty PA prototype with two synthesized combiners: Combiner 1 (b) and Combiner 2 (c), along with CNN-based emulator evaluation comparing predicted impedances (dashed) at the main and auxiliary current-source planes for peak and back-off power against full-wave EM simulated results (solid) from ADS Momentum.

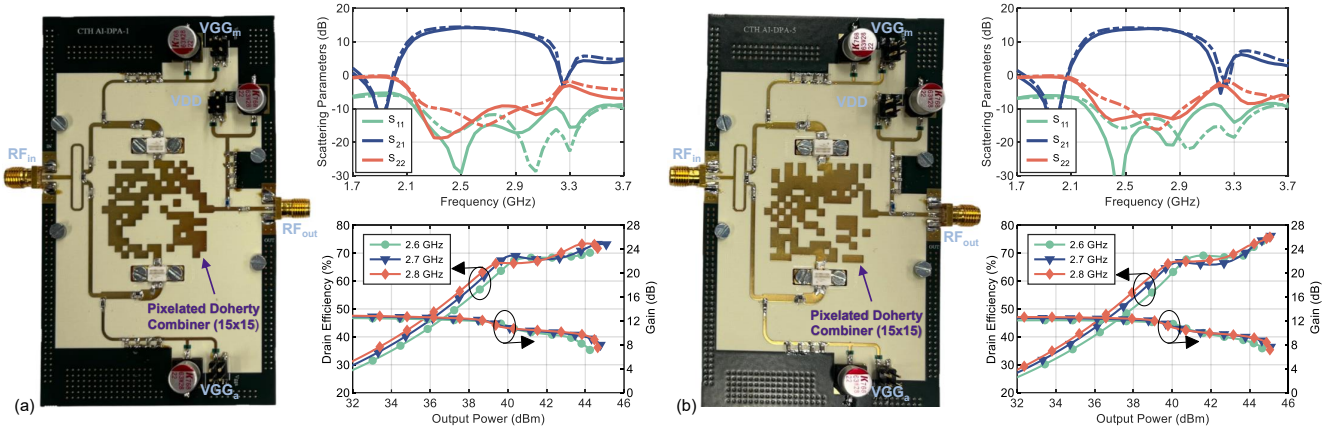

Fig. 3. Two fabricated Doherty PAs with Combiner 1 (a) and Combiner 2 (b), showing simulated (dashed) and measured (solid) small-signal results, along with large-signal continuous-wave (CW) measurements over 2.6–2.8 GHz.

- $\Re(Z_{\mathrm{m,peak}})$ & $\Re(Z_{\mathrm{a,peak}})$ remain within $\pm 10\%$ of R_{opt},
- $\Re(Z_{\mathrm{m,bo}})$ remains within $\pm 10\%$ of $2R_{\mathrm{opt}}$,

while minimizing the imaginary components.

III. Doherty PA Prototype Circuit Design

To validate the proposed inverse design methodology, we developed two Doherty PA prototypes using pixelated combiners synthesized by the deep learning approach. The complete schematics are shown in Fig. 2(a). Both prototypes share the same circuit topology except for the combiners, demonstrating the diversity and robustness of the synthesis method. The designs are implemented on a 20-mil Rogers 4350B substrate using 10-W packaged GaN HEMT transistors (Macom CG2H40010F) for both main and auxiliary devices. As shown in Fig. 1, the employed transistor's output parasitics and packaging elements are well characterized, and its estimated optimal load is $R_{\mathrm{opt}} = 30\ \Omega$ [13].

Fig. 2(b) and (c) present CNN-based emulator evaluations comparing predicted Doherty impedances at the main and auxiliary current-source planes for peak and back-off power against full-wave EM simulated results from ADS Momentum. While minor discrepancies exist in the predicted impedances, its profile closely matches EM results across 2.6–2.8 GHz.

IV. Measurement Results

The photograph of the two fabricated Doherty PAs is shown in Fig. 3. During measurement, for both prototypes, we conduct three types of tests: small-signal, large-signal with continuous-wave (CW), and modulated signal with digital predistortion (DPD). The drain bias is set to $V_{\mathrm{DD}} = 28$ V. The main amplifier is biased with a quiescent current of 40 mA, while the auxiliary gate bias is fixed at -7 V.

A. Small-Siganl and Large-Siganl CW Measurement

The proper response of both Doherty prototypes is confirmed by the good agreement between S-parameter simulations and measurement results, as shown in Fig. 3. Across the 2.2–3.0 GHz band, the measured small-signal gain ranges from 11.8–14.3 dB for prototype 1 and 10.1–13.9 dB for prototype 2. The measured input return loss remains below -11.9 dB and -11.4 dB for prototype 1 and 2, respectively. The CW results, including drain efficiency and gain versus power

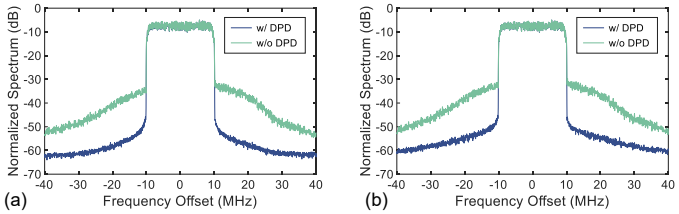

Fig. 4. Normalized spectrum of Doherty prototypes 1 (a) and 2 (b) measured under 20 MHz 7 dB PAPR OFDM signals at 2.7 GHz with and without DPD.

Table 1. Summary of State-of-the-art Load-modulated PAs.

Ref.	Arch.	Freq (GHz)	η_{SAT} (%)	$\eta_{BO\text{-}6dB}$ (%)	P_{SAT} (dBm)	ACLR (dBc)
[15]'25	3-DPA	0.7–0.8	56–62	38–49	43	N.A.
[16]'23	2-DPA	3.3–3.9	48–53	34–45	45.6	N.A.
[17]'20	2-DPA	3.4-3.6	63-70	44-55	41.8	N.A.
[18]'22	LMBA	2.4	54	47	44.1	-48.0
[19]'24	CLMA	3.3–3.5	52–57	51–53	42.2	-51.6
This Work	**DPA 1**	2.6–2.8	71–73	57–64	44.2	-52.7
	DPA 2	2.6–2.8	75–76	56–64	44.3	-51.3

over 2.6–2.8 GHz, are depicted in Fig. 3. Clearly, distinct Doherty profiles with significant efficiency enhancement are observed for both circuits. Within the 2.6–2.8 GHz band, the measured peak drain efficiency ranges from 71.2–73.1% for prototype 1 and 75.2–76.5% for prototype 2. The measured back-off efficiency is 57.3–64.6% and 56.3–63.8% for prototype 1 and prototype 2, respectively. Furthermore, the measured output power exhibits 44.2–44.8 and 44.3–44.7 dBm for prototype 1 and 2, respectively.

B. Modulated-Signal Measurement

The performance of both prototypes are also examined using a 20-MHz orthogonal frequency division multiplexing (OFDM) signal with a 7-dB PAPR signal. As shown in Fig. 4, the adjacent channel leakage ratio (ACLR) improves from -29.8 to -52.7 dBc for prototype 1 and from -31.2 to -51.3 dBc for prototype 2 after applying DPD [14].

As summarized in Table 1, the two fabricated Doherty PAs demonstrate excellent CW performance compared to state-of-the-art designs, along with strong linearizability under modulated signal testing.

V. Conclusion

We propose a dual-state impedance synthesis approach that integrates deep CNNs, pixelated layout representations, and GAs for the design of three-port Doherty combiners. Two GaN Doherty PA prototypes are implemented, achieving peak drain efficiency above 71.2% and saturated output power exceeding 44.2 dBm within the 2.6–2.8 GHz band. Furthermore, a drain efficiency of up to 64% is measured at the 6-dB back-off level. The proposed deep learning-driven design methodology offers a scalable and efficient solution for advancing multi-port load-modulation RF PA architectures.

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References

[1] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng.*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[2] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.

[3] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, 2016.

[4] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-input load modulated balanced amplifier with octave bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5181–5191, 2017.

[5] Y. Cao and K. Chen, "Pseudo-Doherty load-modulated balanced amplifier with wide bandwidth and extended power back-off range," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3172–3183, 2020.

[6] J. Pang, Y. Li, M. Li, Y. Zhang, X. Y. Zhou, Z. Dai, and A. Zhu, "Analysis and design of highly efficient wideband RF-input sequential load modulated balanced power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 5, pp. 1741–1753, 2020.

[7] H. Zhou, J.-R. Perez-Cisneros, B. Langborn, T. Eriksson, and C. Fager, "A wideband and highly efficient circulator load modulated power amplifier architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 8, pp. 3117–3129, 2023.

[8] E. A. Karahan, Z. Liu, and K. Sengupta, "Deep-learning-based inverse-designed millimeter-wave passives and power amplifiers," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3074–3088, 2023.

[9] H. Zhou, H. Chang, D. Widén, L. Fornstedt, G. Melin, and C. Fager, "AI-assisted deep-learning-based design of high-efficiency class F power amplifiers," *IEEE Microw. Wireless Technol. Lett.*, vol. 35, no. 6, pp. 690–693, 2025.

[10] H. Zhou, H. Chang, and C. Fager, "Deep learning driven design of highly efficient harmonic-tuned class F-1 power amplifiers," in *Proc. 55th Eur. Microw. Conf. (EuMC)*, 2025, pp. 208–211.

[11] C. Chu et al, "AI-assisted template-seeded pixelated design for multi-metal-layer high-coupling EM structures: A Ku-band 6G FR3 PA in 22nm FDX+," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2025, pp. 922–925.

[12] K. He, X. Zhang, S. Ren, and J. Sun, "Deep residual learning for image recognition," in *Proc. IEEE Conf. Comput. Vis. Pattern Recognit. (CVPR)*, Las Vegas, NV, USA, Jun. 2016, pp. 770–778.

[13] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing bandwidth and back-off range of Doherty power amplifier with modified load modulation network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2291–2303, 2021.

[14] J. Chani-Cahuana et al, "Iterative learning control for RF power amplifier linearization," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 9, pp. 2778–2789, 2016.

[15] M. G. Becker, R. Krämer, M. Gunia, and F. Ellinger, "Design of a fast-switchable three-stage GaN Doherty PA for high DC-to-RF efficiency," in *Proc. 55th Eur. Microw. Conf. (EuMC)*, 2025, pp. 1905–1908.

[16] M. Shahmoradi, S.-H. Javid-Hosseini, V. Nayyeri, R. Giofrè, and P. Colantonio, "A broadband Doherty power amplifier for sub-6GHz 5G applications," *IEEE Access*, vol. 11, pp. 28 771–28 780, 2023.

[17] H. Lyu and K. Chen, "Balanced-to-Doherty mode-reconfigurable power amplifier with high efficiency and linearity against load mismatch," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 5, pp. 1717–1728, 2020.

[18] K. Vivien, P. E. de Falco, O. Venard, G. Baudoin, P. Pierre-Charles-Félix, and T. Barton, "Load modulated balanced amplifier design method based on complex impedance trajectories," *IEEE Microw. Mag.*, vol. 2, no. 1, pp. 199–213, 2022.

[19] H. Zhou, H. Chang, and C. Fager, "Analysis and design of RF-input Doherty-like circulator load modulated amplifier," in *Proc. 54th Eur. Microw. Conf. (EuMC)*, 2024, pp. 27–30.