CHALMERS
UNIVERSITY OF TECHNOLOGY

Optical Degradation of 845 nm VCSELs with Different Oxide Apertures for Silicon Photonics

Optical Degradation of 845 nm VCSELs With Different Oxide Apertures for Silicon Photonics

Michele Zenari, Matteo Buffolo, *Senior Member, IEEE*, Filippo Perale, Carlo De Santi, *Senior Member, IEEE*, Jeroen Goyvaerts, Alexander Grabowski, Johan S. Gustavsson, Roel Baets, *Life Fellow, IEEE*, Günther Roelkens, *Senior Member, IEEE*, Gaudenzio Meneghesso, *Fellow, IEEE*, Enrico Zanoni, *Life Fellow, IEEE*, and Matteo Meneghini, *Fellow, IEEE*

***Abstract*—In this work, we analyzed the optical degradation of 845 nm VCSELs designed for silicon photonics (SiPh) applications as a function of the oxide aperture. First, we investigated the optical degradation in relation to the stress current. The experimental results showed that devices with a larger oxide aperture exhibit better reliability. From the analysis of the degradation kinetics, we found that the current at which the highly accelerated degradation process occurs depends inversely on the aperture radius. This result was explained by showing that devices with a larger aperture have lower thermal impedance, and therefore operate at lower internal temperatures at similar bias points. This interpretation is supported by isothermal constant current stress tests, which show that when the same internal temperature is maintained during ageing, for all VCSEL geometries under study the onset of degradation occurs at the same time. The equivalent activation energy of the degradation process was found to fall between 0.43 and 0.68 eV. Our analysis demonstrated that using a larger aperture can improve device reliability.**

***Index Terms*—Degradation, silicon photonics, VCSEL, thermal impedance.**

I. Introduction

In RECENT years, data centers and computing applications have been experiencing bottlenecks in data transmission and energy efficiency [1], [2]. Due to the limitations of electrical signals transmitted through copper wires, electrical transmission has largely been replaced by optical communication for long-haul transmission. However, this shift has not yet been implemented for short-range communications (i.e., board- and chip-level data communications) due to the cost and size of optical transceivers. Silicon photonics (SiPh) aims to bridge this gap by providing highly scalable and low-cost optical devices [3].

To achieve this goal, SiPh leverages the standard CMOS process to fabricate all the required photonic components, except for laser diodes. Due to its indirect bandgap, silicon is not suitable as an optical source [4]. Instead, III-V materials such as GaAs and InP are employed to develop IR sources. Nonetheless, the material mismatch between the substrate (silicon) and the active materials results in poor material quality [5], [6], [7] that lead to suboptimal optical performance and short-lifetime lasers. In the last two decades, various alternatives to the direct growth of III-V layers onto silicon have been proposed. The most common approaches include flip-chip integration [8], bonding [9], and, more recently, micro-transfer printing [10], which has recently gained significant momentum. Micro-transfer printing involves picking up a pre-processed device coupon from a source wafer, which is then printed onto the host photonic integrated circuit (PIC) wafer using a stamp [11]. Consequently, III-V devices do not exhibit extended defects due to materials mismatch.

The most common laser diodes integrated in PICs are edge-emitting devices such as Fabry-Pérot (FP), Distributed Bragg Reflector (DBR), and Distributed Feedback (DFB). These lasers all have extended planar cavities and exhibit relatively high threshold currents, ranging from 10 to 100 mA. In short-reach communications, such as in data centers, there are strict requirements in terms of energy consumption [12]. The most promising optical sources for high-speed, low-power communication are the vertical-cavity surface-emitting lasers (VCSELs). Compared to other types of lasers, VCSELs offer high-throughput wafer-level testing, easy interfacing with optical fibers, and, most importantly, sub-mA threshold currents and high slope efficiencies, making them excellent candidates as light sources for PICs [13]. In the past few years, several studies have addressed the degradation modes of infrared VCSELs [14], [15], [16]. However, there is a lack of studies on photonic integrated

Received 16 January 2026; revised 30 April 2026 and 31 May 2026; accepted 3 June 2026. Date of publication 10 June 2026; date of current version 13 July 2026. *(Corresponding author: Matteo Buffolo.)*

Michele Zenari, Matteo Buffolo, Filippo Perale, Carlo De Santi, Gaudenzio Meneghesso, and Enrico Zanoni are with the Department of Information Engineering, University of Padova, 35131 Padova, Italy (e-mail: michele.zenari@dei.unipd.it; matteo.buffolo.1@unipd.it; filippoperale@gmail.com; carlo.desanti@unipd.it; gauss@dei.unipd.it; zanoni@dei.unipd.it).

Jeroen Goyvaerts is with LIGENTEC SA, EPFL Innovation Park Bâtiment L, 1024 Ecublens, Switzerland (e-mail: jeroen.goyvaerts@ligentec.com).

Alexander Grabowski is with Solinide Photonics AB, 433 34 Partille, Sweden (e-mail: agrabowski@solinide.com).

Johan S. Gustavsson was with the Photonics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden. He is now with the Nvidia corp., Santa Clara, CA 95052 USA (e-mail: jgustavsson@nvidia.com).

Roel Baets and Günther Roelkens are with Photonics Research Group, Technologiepark-Zwijnaarde, Ghent University-imec, 9052 Gent, Belgium (e-mail: roel.baets@ugent.be; gunther.roelkens@ugent.be).

Matteo Meneghini is with the Department of Information Engineering, University of Padova, 35131 Padova, Italy, and also with the Department of Physics and Astronomy, University of Padova, 35131 Padova, Italy (e-mail: matteo.meneghini@unipd.it).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSTQE.2026.3702031.

Digital Object Identifier 10.1109/JSTQE.2026.3702031

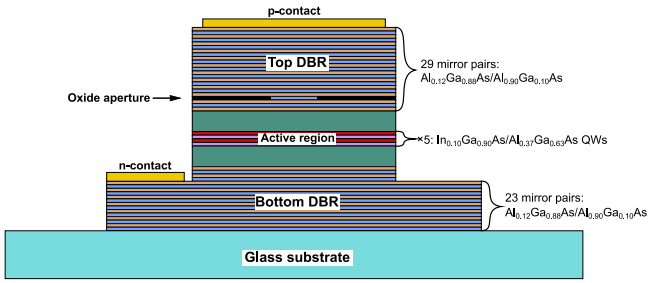

Fig. 1. Cross-sectional schematic of the VCSEL structure used in this work.

lasers, which could suffer from higher thermal impedance due to integration on silicon-on-insulator (SOI) or other thermally insulating platforms. To fill this gap, in this paper we investigated the optical reliability of 845 nm VCSELs suitable for integration into SiN platforms for silicon photonics [17], [18] with a new set of experiments testing devices with different oxide aperture. The oxide aperture diameter is a key design parameter in VCSELs, as it directly affects the threshold current, series resistance, and optical mode profile. In general, larger oxide apertures reduce the resistance and thermal impedance, leading to lower internal temperatures during operation for a given current, but potentially bring the device into potential multi longitudinal modes operation [19] However, the aperture size also influences device reliability: a lower thermal impedance slows down temperature-activated degradation processes, such as impurity diffusion, which ultimately limits the device lifetime. Therefore, for VCSELs the choice of oxide aperture involves a trade-off between optical performance and long-term reliability.

Firstly, we studied optical degradation using current step stress and constant current stress experiments on devices with three different apertures (4, 5, and 6 μm). Then, we evaluated the thermal impedance of the three geometries through pulsed measurements. Finally, we repeated the constant current experiments for the 4 μm aperture lasers at different ambient temperatures to determine the activation energy of the main degradation process.

Based on the experimental results of our study, we demonstrate that i) in devices with larger aperture, the onset of high-accelerated degradation occurs at higher currents; ii) this feature is directly related to the lower thermal impedance, which decreases with increasing diameter; iii) the onset of critical threshold current increase is thermally-activated, with an activation energy of 0.43 to 0.68 eV.

II. Devices Under Test

The devices analyzed within this work are vertical-cavity surface-emitting laser diodes emitting at 845 nm. The structure (Fig. 1), starting from the top, includes a Ti/Pt/Au disk-shaped p-contact that serves both as electrode and as a top reflector. The top DBR is p-doped with carbon and consists of 29 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. At the bottom of the p-DBR, within the layer closest to the separate confinement heterostructure (SCH) region, a 30-nm $Al_{0.98}Ga_{0.02}As$ layer is included. This layer enables the formation of a 4–6 μm oxide aperture through selective wet oxidation. The presence of this aperture laterally confines the current, and consequently the optical mode to the center of the circular VCSEL structure. The active area of the laser is located below the aperture and consists of a $1-\lambda$ thick SCH and a multi-quantum-well (MQW) structure containing five 4 nm thick $In_{0.10}Ga_{0.90}As/Al_{0.37}Ga_{0.63}As$ QWs. The bottom DBR is n-doped and is composed of 23 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. A Ni/Ge/Au n-contact is positioned a few DBR mirror pairs below the active volume. At the bottom of the n-DBR, a 527 nm $Al_{0.12}Ga_{0.88}As$ buffer layer is purposely included to tune the cavity length between the bottom DBR and the substrate, which is supposed to include a diffraction grating in the final application [13]. Underneath this layer, a 4 nm GaAs layer serves as an etch stop layer with respect to an $In_{0.49}Ga_{0.51}P$ sacrificial layer, which is required for the micro-transfer-printing process. Further information regarding the device epitaxy, growth, and fabrication can be found in [21]. The devices are meant to be transferred onto a SiN platform, thus allowing the fabrication of vertical-cavity silicon-integrated lasers (VCSILs) [21]. The samples analyzed in this work were transferred onto a glass substrate to characterize the optical emission from the bottom side.

The glass substrate not only enables bottom-side characterization, which is useful from a research and a diagnostic perspective, but also has a refractive index similar to that of SiO_2, leading to minimal perturbation of the optical mode compared to the target application on SiN platform.

III. Methodology

To measure the optical degradation of the devices, we tested representative VCSELs with 4, 5, and 6 μm oxide apertures. The samples were aged and characterized at a fixed temperature using a source meter. The temperature control was maintained by a TEC-controlled baseplate.

First, to evaluate degradation as a function of the stress current, the devices were submitted to a current step stress experiment.

In this aging test, the stress current was increased by 50 μA every hour, starting from 50 μA. After each stage of the step-stress, an optical characterization (L-I) was performed.

To evaluate the degradation kinetics over time, the devices were then subjected to a constant-current stress experiment. The aging test was interrupted at various stages to evaluate the effect of device degradation by performing L-I characterization. In this work, we analyze the results of various current stress tests carried out up to 7 mA.

Regarding the measurement of the thermal impedance, we employed a pulsed setup to map the device internal temperature following Xi's forward voltage method [20]. To this aim, we applied square waveforms featuring 2 μs pulse width and a repetition period of 1 ms, resulting in a 0.2% duty cycle to minimize device self-heating. The results of these analyses are reported in the following section.

IV. Optical Degradation

A. Current Step-Stress Results

During the current step-stress test, we recorded the L-I characteristics every hour before increasing the stress current by

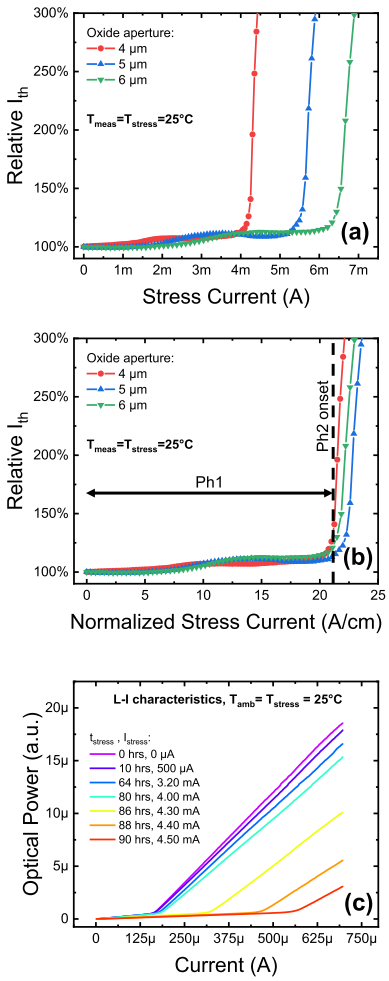

Fig. 2. (a) Relative threshold current kinetics for three different geometries (4, 5, and 6 μm oxide aperture width) during a current step-stress experiment (b) the stress current was normalized for the oxide radius. The graph shows that the onset of Ph2 degradation process is related to the oxide aperture width. (c) Representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the current step-stress experiment.

50 μA. This experiment was carried out for all device geometries under investigation (4, 5, and 6 μm oxide apertures). From the experimental data, we extracted the degradation kinetics of the threshold current (I_{th}) as a function of the stress current (Fig. 2(a))). Each curve exhibits two distinct phases: initially, I_{th} shows a mild degradation (an overall 10-15% increase), referred to as Ph1. This is followed by the onset of a second, faster degradation process, indicated as Ph2. The degradation process observed in the devices under investigation has been previously reported. In particular, in [17] we demonstrated that, regardless of the final substrate [18], devices based on such III-V epitaxy are affected by the diffusion of impurities, which initially move across the top DBR, causing a limited worsening in optical performance (Ph1). Subsequently, when these impurities reach the active region, they lead to significant optical degradation (Ph2).

By looking at the kinetics, we can see that the 6 μm aperture device shows the onset of Ph2 at higher currents (≈6.5 mA) compared to the other two devices (≈5.5 mA for the 5 μm aperture and ≈4 mA for the 4 μm aperture device). Generally speaking, these results indicate that, for comparable operating current levels, devices with larger diameters have better reliability. To investigate the origin of these results, we normalized the stress current of the three devices by the radius of the oxide aperture, obtaining degradation kinetics as a function of the stress current per unit length (A/cm). The outcome of this normalization is shown in Fig. 2(b): remarkably, now the three degradation curves are nearly superimposed, and, in addition to that, the onset of Ph2 occurs at the same current per unit length (i.e., ≈21 A/cm). Fig. 2(c) shows representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the current step-stress experiment, from which the threshold current kinetics were extracted. Noticeably, the relative variation in threshold current is stronger than the change in slope efficiency. In order to look for correlation between device geometry and specific driving forces of the ageing process, we decided to evaluate device temperature in the three different scenarios, first. To do this, we leveraged the expression for the VCSELs' thermal impedance, R_{th} [22]:

$$R_{th} = \frac{1}{2\xi S} \tag{1}$$

where ξ is the material's thermal conductivity and S is the device diameter. This formula was derived by considering the 3D heat flow from a disk-shaped heat source of diameter S on a half-space. Therefore, it is valid for a small-diameter VCSEL mounted on the top side of a relatively thick substrate, as in our case. Equation (1) shows an inverse dependence on the aperture radius, as indicated by normalized degradation kinetics in Fig. 2(b)). Based on this observation, we hypothesize that the onset of Ph2 (and consequently the degradation) depends on the thermal impedance of the devices, i.e., to its operating temperature. Since the degradation phenomena are related to a diffusion process, it is reasonable to assume that the internal temperature plays a fundamental role in determining the speed of the degradation process. To confirm this, we measured the thermal impedance of the three devices to figure out the dependence of this quantity with respect to the aperture radius.

B. *Thermal Impedance Measurement*

To probe the internal temperature, we measured the voltage drop across the device over short time periods at specific currents and temperatures. Details on the method used to assess the thermal impedance can be found in [20]. To determine the dependence of the voltage drop on temperature, we measured this quantity before the device began self-heating. For this purpose, we employed a voltage pulser to apply short pulses (≈2 μs) to observe the voltage drop before it decreases due to the rise in internal temperature. To limit self-heating, we set a pulse repetition period of 1 ms (the maximum allowed by the instrument), resulting in a duty cycle of 0.2%. Under this configuration, we can assume that the measured voltage drop, V_j, can be directly related to the internal temperature $T_j = T_{amb}$ (where T_{amb} is the baseplate temperature). We decided to map the currents between 1 to 4 mA over the 20–70 °C range. The results of the thermal maps for the 5 μm aperture

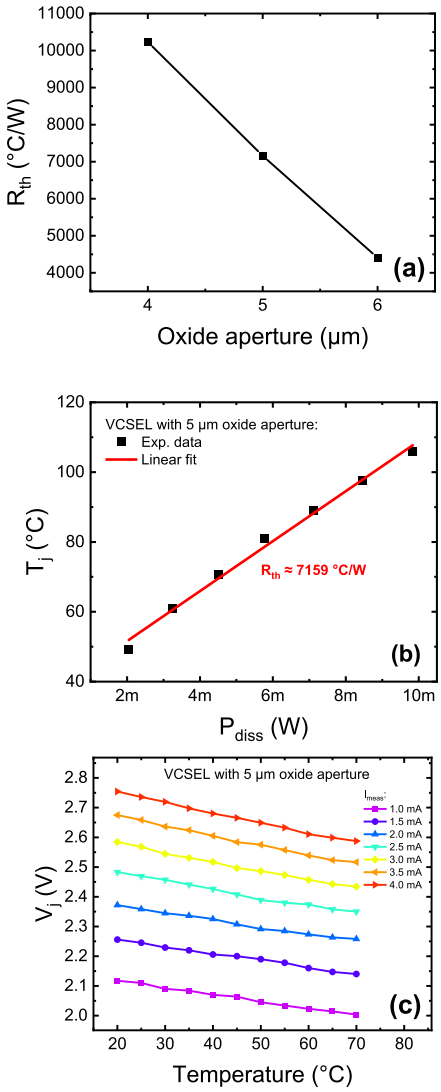

Fig. 3. (a) Dependence of thermal impedance on the oxide aperture. The trend appears to represent a linear approximation of a 1/rox function. (b) Extrapolation of R_{th} from junction temperature estimation for different dissipated power values (4 μm oxide aperture VCSEL). (c) Thermal map extrapolated for seven currents (from 1 to 4 mA) in a 5 μm oxide aperture VCSEL.

device are shown in Fig. 3(c)). Subsequently, we recorded the CW voltage drop after internal temperature stabilization for the same set of currents. These measurements were carried out at T_{amb} = 25 °C (i.e., equal to T_{stress}). By comparing the steady-state voltage drops after the thermal transients (caused by the device's self-heating) with the previously calculated thermal maps, we determined the internal temperature T_j by fitting the experimental data. Finally, to calculate the thermal impedance R_{th}, we extrapolated the corresponding dissipated power, P_{diss}, for each current:

$$P_{diss} = P_{el} - P_{opt} = V_j^{CW} \times I - P_{opt} \quad (2)$$

Equation (2) shows that the dissipated power, P_{diss}, is determined by subtracting the emitted optical power, P_{opt}, from electrical power, P_{el}, which is the product of the current (I) and the CW voltage drop (V_j^{CW}). Fig. 3(b)) shows the T_j vs. P_{diss} graph for the 5 μm aperture device, from which a thermal impedance of about $7 \cdot 10^3$ °C/W was calculated. The numerical results of the R_{th} for the three devices are consistent with previous reports on VCSELs [23]. We eventually compared results for the three geometries under test (Fig. 3(a)), confirming that the thermal impedance decreases with increasing the aperture diameter. This feature can be physically explained by noting that the oxide aperture confines the current within the III-V stack. In VCSELs with a larger aperture, the current density is distributed over a larger volume. Consequently, power is dissipated over this larger volume, resulting in a lower internal temperature. A 2D simulation of current density distribution across a similar VCSEL stack is illustrated in [18].

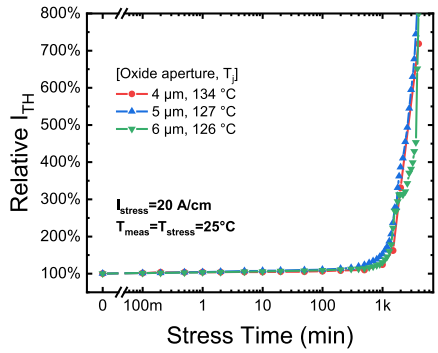

Fig. 4. Threshold current kinetics for constant current stress experiments carried out at 20 A/cm (i.e., for the current normalized by the aperture radius). The outcome of the aging test confirms that the degradation of the devices depends on the oxide aperture.

C. Constant Current Stress Results

Based on the results of the current step stress experiments, we hypothesized that the speed of the degradation process (impurity diffusion) depends on the internal temperature of the devices. Since the thermal impedance is inversely related to the aperture radius, we conducted the constant current stress tests with the same current per unit length to ensure that the experiments were carried out at similar internal temperatures, T_j. To observe the worsening of the threshold current within a reasonable time period (≈5 kmin), we selected a stress current of 4 mA for the 4 μm aperture device based on our previous results [17]. This stress current corresponds to 20 A/cm (i.e., 4 mA normalized to a radius of 2 μm), which means that the 5 μm aperture device will be stressed at 5 mA, and the 6 μm aperture device at 6 mA.

The experimental results shown in Fig. 4 indicate that the devices exhibit the same degradation kinetics, confirming our hypothesis on the role of internal temperature in the diffusion process. The legend in the graph indicates the T_j calculated from the resulting R_{th} obtained in Section IV-B. The calculated internal temperatures are approximately 130 °C. Minor differences between the three temperatures may arise from the fact that the thermal maps presented in Section IV-B were based on experimental measurements carried out between 20 °C and 70 °C. Consequently, the estimated T_j values, which exceed the

experimental range of mapping, suffer from a certain level of uncertainty.

D. Constant Current Stress Results: Temperature Dependence

In this section, we report the results of constant current stress tests carried out at fixed stress current for various temperatures. We chose to test the 4 μm aperture device with a stress current of 3.5 mA (≈27 kA/cm^2) at $T_{stress} = 40, 55$, and 70 °C. The 3.5 mA stress condition used for the 4 μm oxide aperture VCSEL is about 20 times its threshold current (≈180 μA, see figure Fig. 2(c)) and lies well beyond the thermal rolloff point. Such high current densities are not relevant for practical operation, but they are useful from a reliability perspective because they accelerate degradation and allow Ph2 failure mechanisms to be observed within a reasonable experimental timeframe. The degradation kinetics of I_{th} are shown Fig. 5(a)). Clearly, the onset of Ph2 occurs at shorter stress times as the baseplate temperature, and consequently, the internal temperature, is increased.

To better illustrate the impact of temperature on the degradation rate, we built an Arrhenius plot of the time-to-failure (TTF), defined as the time required for the aging procedure to increase the initial threshold current of the device by specific amounts: 25%, 50%, and 75%. The resulting Arrhenius plot is shown in Fig. 5(b)). Depending on the failure criterion considered, the resulting activation energy ranges from 0.43 to 0.68 eV. The observed spread in activation energy reflects the limited statistical sampling in this study. Nevertheless, the data unambiguously show that higher temperatures accelerate the onset of Ph2 degradation, consistent with a thermally activated process. For a representative visualization of the device degradation during this experiment, Fig. 5(c) shows the evolution of the L-I characteristics collected throughout the constant current stress test. The trends of threshold current and slope efficiency are analogous to the ones discussed for Fig. 2(c).

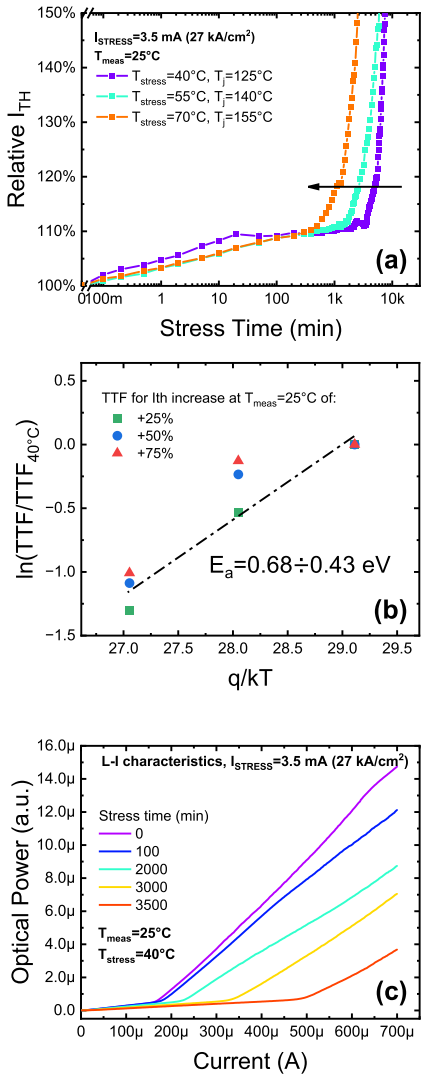

Fig. 5. (a) Constant current stress results at 3.5 mA for different stress temperatures (40, 55, and 70 °C): The Ph2 onset is activated for shorter stress time at increasing operating temperature. (b) Arrhenius plot extrapolated for three different TTF conditions: +25%, +50%, and +70% degradation of the I_{th}. The resulting activation energy hovers between 0.43 eV and 0.68 eV. (c) Representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the constant current stress experiment.

V. Conclusion

In summary, we analyzed the reliability of 845 nm VCSELs for silicon photonics featuring three different widths of the oxide aperture, by means of accelerated aging experiments. First, we examined the optical degradation of the devices as a function of the stress current through current step stress experiments. As the oxide aperture increased, the devices demonstrated improved reliability with respect to the stress current. The experimental curves revealed a dependence of the second (main) degradation phase on the stress current normalized by the aperture radius, leading us to hypothesize that degradation is influenced by the internal temperature of the devices. To confirm this hypothesis, we measured the thermal impedance using pulsed characteristics, and determined that its value decreases with increasing oxide aperture diameter, approximately following a $1/r_{ox}$ relation. Additionally, a constant current stress experiment carried out at 20 A/cm, to maintain the same internal temperature across all three devices, verified our hypothesis by showing that the Ph2 onset occurs at the same stress time for all three geometries. Finally, additional stress tests carried out at different T_j allowed us to identify the thermal activation energy of the main optical degradation, which falls within the 0.43 to 0.68 eV range.

The reported data ultimately demonstrate that VCSELs featuring larger apertures exhibit higher optical reliability. This improvement is closely related to the resulting thermal impedance: as the oxide aperture increases, the thermal impedance decreases, which in turn reduces the internal temperature during stress for the same current. This is beneficial for reliability because a lower internal temperature slows the diffusion process that eventually causes the severe optical degradation occurring for longer stress times. However, the choice of oxide aperture affects not only the thermal impedance but also the threshold current, series resistance and the optical behavior of the laser diode. This indicates the presence of a tradeoff between performance and reliability.

ACKNOWLEDGMENT

The authors would like to thank Prof. Anders Larsson for his participation and support during the development of this work.

REFERENCES

[1] J. Meng, M. Miscuglio, J. K. George, A. Babakhani, and V. J. Sorger, "Electronic bottleneck suppression in next-generation networks with integrated photonic digital-to-analog converters," *Adv. Photon. Res.*, vol. 2, no. 2, Feb. 2021, Art. no. 2000033, doi: 10.1002/adpr.202000033.

[2] N. Margalit et al., "Perspective on the future of silicon photonics and electronics," *Appl. Phys. Lett.*, vol. 118, no. 22, 2021, Art. no. 220501, doi: 10.1063/5.0050117.

[3] A. Rahim et al., "Open-access silicon photonics platforms in Europe," *IEEE J. Sel. Topics Quantum Electron.*, vol. 25, no. 5, Sep./Oct. 2019, Art. no. 8200818, doi: 10.1109/JSTQE.2019.2915949.

[4] T. Trupke, M. A. Green, and P. Würfel, "Optical gain in materials with indirect transitions," *J. Appl. Phys.*, vol. 93, no. 11, pp. 9058–9061, 2003, doi: 10.1063/1.1571223.

[5] C. S. C. Barrett et al., "Dissolution of antiphase domain boundaries in GaAs on Si(001) via post-growth annealing," *J. Mater. Sci.*, vol. 54, no. 9, pp. 7028–7034, 2019, doi: 10.1007/s10853-019-03353-7.

[6] D. Jung et al., "Impact of threading dislocation density on the lifetime of InAs quantum dot lasers on Si," *Appl. Phys. Lett.*, vol. 112, no. 15, Apr. 2018, Art. no. 153507, doi: 10.1063/1.5026147.

[7] J. Selvidge et al., "Defect filtering for thermal expansion induced dislocations in III-V lasers on silicon," *Appl. Phys. Lett.*, vol. 117, no. 12, 2020, Art. no. 122101, doi: 10.1063/5.0023378.

[8] A. Moscoso-Mártir et al., "Hybrid silicon photonics flip-chip laser integration with vertical self-alignment," in *Proc. Conf. Lasers Electro-Opt. Pacific Rim*, 2017, pp. 1–4, doi: 10.1109/CLEOPR.2017.8118971.

[9] A. W. Fang et al., "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," *Opt. Exp.*, vol. 14, no. 20, Oct. 2006, Art. no. 9203, doi: 10.1364/oe.14.009203.

[10] G. Roelkens et al., "Micro-transfer printing for heterogeneous Si photonic integrated circuits," *IEEE J. Sel. Topics Quantum Electron.*, vol. 29, no. 3, May/Jun. 2023, Art. no. 8200414, doi: 10.1109/JSTQE.2022.3222686.

[11] G. Roelkens et al., "Present and future of micro-transfer printing for heterogeneous photonic integrated circuits," *APL Photon.*, vol. 9, no. 1, Jan. 2024, Art. no. 010901, doi: 10.1063/5.0181099.

[12] A. Malik et al., "Low power consumption silicon photonics datacenter interconnects enabled by a parallel architecture," presented at the*Opt. InfoBase Conf. Papers*, Washington, DC, USA, Jun. 06–11, 2021, Paper W6A.3, doi: 10.1364/ofc.2021.w6a.3.

[13] S. Kumari et al., "Vertical-cavity silicon-integrated laser with in-plane waveguide emission at 850 nm," *Laser Photon. Rev.*, vol. 12, no. 2, pp. 1–7, 2018, doi: 10.1002/lpor.201700206.

[14] S. Xie et al., "Failure mode analysis of oxide VCSELs in high humidity and high temperature," *J. Lightw. Technol.*, vol. 21, no. 4, pp. 1013–1019, Apr. 2003, doi: 10.1109/JLT.2003.809546.

[15] K. H. Rhew, S. C. Jeon, D. H. Lee, B. S. Yoo, and I. Yun, "Reliability assessment of 1.55-μm vertical cavity surface emitting lasers with tunnel junction using high-temperature aging tests," *Microelectronics Rel.*, vol. 49, no. 1, pp. 42–50, Jan. 2009, doi: 10.1016/J.MICROREL.2008.10.008.

[16] R. W. Herrick et al., "Corrosion-based failure of oxide-aperture VCSELs," *IEEE J. Quantum Electron.*, vol. 49, no. 12, pp. 1045–1052, Dec. 2013, doi: 10.1109/JQE.2013.2285572.

[17] M. Zenari et al., "Understanding the optical degradation of 845nm micro-transfer-printed VCSILs for photonic integrated circuits," *IEEE J. Quantum Electron.*, vol. 59, no. 4, Aug. 2023, Art. no. 2400210, doi: 10.1109/JQE.2023.3283514.

[18] M. Zenari et al., "Impact of the oxide aperture width on the degradation of 845 nm VCSELs for silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 31, no. 2, Mar./Apr. 2025, Art. no. 1500209, doi: 10.1109/JSTQE.2024.3415674.

[19] J. Mu et al., "A novel metal-mode-filtered vertical-cavity surface-emitting laser with 8 μm oxide aperture and single mode output," *Results Phys.*, vol. 54, 2023, Art. no. 107107, doi: 10.1016/j.rinp.2023.107107.

[20] Y. Xi and E. F. Schubert, "Junction-temperature measurement in GaN ultraviolet light-emitting diodes using diode forward voltage method," *Appl. Phys. Lett.*, vol. 85, no. 12, pp. 2163–2165, 2004, doi: 10.1063/1.1795351.

[21] J. Goyvaerts et al., "Enabling VCSEL-on-silicon nitride photonic integrated circuits with micro-transfer-printing," *Optica*, vol. 8, no. 12, 2021, Art. no. 1573, doi: 10.1364/optica.441636.

[22] L. A. Coldren, "Diode lasers and photonic integrated circuits," *Opt. Eng.*, vol. 36, no. 2, 1997, Art. no. 616, doi: 10.1117/1.601191.

[23] S. Mishkat-Ul-Masabih, J. Leonard, D. Cohen, S. Nakamura, and D. Feezell, "Techniques to reduce thermal resistance in flip-chip GaN-based VCSELs," *Phys. Status Solidi A*, vol. 214, 2017, Art. no. 1600819, doi: 10.1002/pssa.201600819.

Michele Zenari was born in Soave, Italy, in 1996. He received the M.Sc. degree in electronic engineering from the University of Padua, Padua, Italy, in 2020, with a thesis focused on the analysis and modeling of InAs quantum dot lasers epitaxially grown on silicon, and the Ph.D. degree in information and communication science and technology from the Department of Information Engineering, University of Padua, in 2024, where his research interests include the characterization and reliability of quantum dot lasers and vertical-cavity surface-emitting lasers for silicon photonics. He is currently a Postdoctoral Researcher with Ghent University–imec, Ghent, Belgium, where he conducts research on device reliability and modeling for silicon photonics

Matteo Buffolo (Senior Member, IEEE) was born in Vittorio Veneto, Italy, in 1986. He received the master's degree in electronic engineering from the University of Padova, Padua, Italy, with a thesis focusing on the analysis of the degradation mechanisms of GaN-based mid-power white LEDs and the Ph.D. degree from the Department of Information Engineering, University of Padova, in 2018. He is currently a Postdoc with the University of Padova. His research interests include the reliability of lighting systems employing GaN-based devices (lasers and LEDs) and on the investigation of the degradation mechanisms that affect modern IR laser sources for integrated telecommunication applications.

Filippo Perale received the M.Sc. degree in electronic engineering from the University of Padua, Padua, Italy, in 2023. His master's thesis focused on the characterization, reliability, and degradation modeling of infrared laser diodes for silicon photonics fabricated by micro-transfer printing.

Carlo De Santi (Senior Member, IEEE) was born in Verona, Italy, in 1985. He received the Ph.D. degree in 2014. He is currently a Postdoc with Microelectronics Group, University of Padova, Padua, Italy. He is the author of more than 30 peer-reviewed journal papers, 50 contributions in conference proceedings and four book chapters. His main research interests include characterization, physical modeling and reliability of various GaN-,GaAs-, InP-, Ga2O3-, CdTe- and Si-based electronic, and optoelectronic devices.

Jeroen Goyvaerts received the M.Sc. degree in nanoscience and nanotechnology from the Catholic University of Leuven, Leuven, Belgium, the second M.Sc. degree in photonics from the Polytechnic University of Catalunya, Barcelona, Spain, and the Ph.D. degree from the Department of Information Technology, Ghent University, Ghent, Belgium, in 2021, for his work on integrating GaAs opto-electronic components onto SiN waveguide circuits by means of micro-transfer-printing. Since 2021, he has joined the LIGENTEC SA team as a Design Engineer and Project Leader, to further commercialise low-loss SiN waveguide technology for applications in computing, metrology and sensing.

Alexander Grabowski received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Chalmers University of Technology, Göteborg, Sweden, in 2017 and 2022, respectively. He is currently a Postdoc with the Department of Microtechnology and Nanoscience, Chalmers. He was on GaAs-based vertical-cavity surface-emitting lasers (VCSELs) in high-speed short-reach optical interconnects, mainly focusing on modeling of the VCSEL. He has also done work on fabrication of GaAs-based VCSELs for micro-transfer-printing integration on a silicon nitride PIC platform.

Johan S. Gustavsson received the M.Sc. degree in electrical engineering and the Ph.D. degree in photonics from the Chalmers University of Technology, Gothenburg, Sweden, in 1998 and 2003, respectively. His Ph.D. thesis was focused on mode dynamics and noise in vertical-cavity surface-emitting lasers (VCSELs). Since 2003, he has been a Researcher with the Photonics Laboratory, Chalmers, an Assistant Professor from 2004 to 2008 and has been an Associate Professor since 2011. From September 2009 to October 2009, he was a Visiting Scientist with the CNR Polytechnico, Turin, Italy. In 2016, he co-founded the spin-off company OptiGOT AB, which was acquired by Nvidia Corporation in 2020. In 2017, he co-organized the European Semiconductor Laser Workshop in Copenhagen. He has authored or coauthored more than 250 scientific journals and conference papers and two book chapters. His research interests include semiconductor lasers for short to medium reach communication and sensing applications. This has included surface relief techniques for mode and polarization control in VCSELs, 1.3 μm InGaAs VCSELs/GaInNAs ridge waveguide lasers for access networks, 2.3–3.5 μm GaSb VCSELs for CO, CO2, and NH3 sensing, and tunable VCSELs via moveable mirror for reconfigurable optical interconnects. He is currently working on energy efficient 56 Gbaud GaAs-based VCSELs for next generation datacom links, UV/blue AlGaN/GaN VCSELs for sterilizing/illumination, high contrast gratings as feedback/wavelength setting/focusing elements in micro-cavity lasers, and heterogeneous integration of III/V-based VCSEL material on a Si platform. He is also exploring photon-photon resonance effects to boost the modulation bandwidth in GaAs-based VCSELs.

Roel Baets (Life Fellow, IEEE) is currently a Full Professor with Ghent University, Ghent, Belgium, where he leads a mixed UGent – imec team. For about 40 years Roel Baets has worked in the field of integrated photonics, in multiple material platforms (silicon, silicon nitride, III-V). He has made diverse scientific contributions to this field, and to its applications and spin-off creation in telecom, datacom and sensing. He has led major research projects in silicon photonics in Europe and founded ePIXfab, the globally first Multi-Project-Wafer service for silicon photonics and the European Silicon Photonics Alliance. His current research interests include medical and environmental sensing applications of silicon photonics. He is a Fellow of the European Optical Society and Optical Society. He was the recipient of the 2018 PIC-International Lifetime Achievement Award and the 2020 John Tyndall award.

Günther Roelkens (Senior_Member, IEEE) received the degree in electrical engineering from Ghent University, Ghent, Belgium, in 2022 and the Ph.D. degree from the Department of Information Technology, Ghent University. where he is currently a Full Professor. In 2008, he was a Visiting Scientist with IBM TJ Watson Research Center, New York, NY, USA. His research interests include the heterogeneous integration of III-V semiconductors and other materials on top of silicon waveguide circuits and electronic/photonic co-integration. He was holder of an ERC staring grant (MIRACLE), to start up research in the field of integrated mid-infrared photonic integrated circuit.

Gaudenzio Meneghesso (Fellow, IEEE) received the graduation in electronics engineering from the University of Padova, Padua, Italy, in 1992, working on the failure mechanism induced by hot-electrons in MESFETs and HEMTs. Since 2011, he has been with the University of Padova as a Full Professor. He has authored or coauthored more than 800 technical papers, of which more than 100 invited papers in his research fields, which include electrical characterization, modeling, and reliability of microelectronics devices. He was nominated to IEEE Fellow class 2013, with the following citation, for contributions to the reliability physics of compound semiconductors devices. He was the recipient of the 12 Best Paper awards for his authored or coauthored papers.

Enrico Zanoni (Life Fellow, IEEE) was born in Verona, Italy, in 1956. He received the Laurea (cum laude) degree in physics from the University of Modena and Reggio Emilia, Modena, Italy, in 1982. Since 1997, he has been a Full Professor of digital electronics with the Department of Information Engineering, University of Padua, Padua, Italy.

Matteo Meneghini (Fellow, IEEE) received the Ph.D. degree from the University of Padua, Padua, Italy, in 2008. He is currently an Associate Professor with the Department of Information Engineering, University of Padua, where he is involved in the electro-optical characterization and modeling of the performance and reliability of LEDs, lasers, HEMTs, and advanced solar cells.

Open Access funding provided by 'Universita degli Studi di Padova' within the CRUI CARE Agreement