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Ku-Band Doherty Power Amplifier with Differential Power Combiner in an Advanced GaN-on-Si HEMT Technology for 6G FR3 Applications

Abdolhamid Noori[$#], Jorge Moreno Rubio[*], Christoph Wagner[$], Christian Fager[#], Gregor Lasser[#]
[$]Millimeter Wave Technologies, Intelligent Wireless Systems, Silicon Austria Labs GmbH, Austria
[#]Department of Microtechnology and Nanoscience, Microwave Electronics Laboratory,
Chalmers University of Technology, Sweden
[*]Department of Electronics, Universidad Pedagógica y Tecnológica de Colombia, Colombia
{abdolhamid.noori, christoph.wagner}@silicon-austria.com, jorgejulian.moreno@uptc.edu.co,
{christian.fager, gregor.lasser}@chalmers.se

***Abstract*— This paper presents a fully monolithic Ku-band Doherty power amplifier (DPA) employing differential power combiner cells as main and auxiliary amplifier in Infineon's RF GaN-on-Si HEMT MMIC technology. The differential power combiner absorbs the intrinsic output capacitance, C_{out}, of the transistors while implementing the Doherty combining network with a simplicity close to the original concept, which eases high-frequency design and integration. The DPA is characterized under pulsed-RF conditions and achieves a maximum small-signal gain of 9.4 dB at 15.1 GHz, a saturated output power of about 37.7 – 38.7 dBm with a peak PAE of 28.7 – 32.3 %, and a 6-dB OBO PAE of 22.5 – 25 % over 14.3 – 15.3 GHz, corresponding to a 6.7% fractional bandwidth, in 4 mm × 4 mm die with a power density of 0.47 W/mm^2.**

***Keywords*— Differential power combiner, Doherty power amplifier, fully integrated MMIC, GaN on Si HEMT, Ku-Band, 6G FR3.**

I. Introduction

In modern communication systems, and with the evolution toward 6G FR3 bands, the demand for high power power amplifiers capable of maintaining high efficiency under complex modulation schemes with large peak-to-average power ratios (PAPR) is steadily increasing. The Doherty PA is a well-known output power back-off (OBO) efficient architecture to handle high PAPR modulation schemes [1]. The effect of the parasitic output capacitances of the transistors becomes increasingly severe as the operating frequency increases, leading to degradation the amplifier efficiency and output power. Furthermore, with the physical scaling of transistors, the intrinsic device efficiency tends to decrease as frequency increases, which motivates the use of power combining of smaller transistors to achieve higher output power while maintaining improved overall performance. In parallel combining structures, Parasitic elements can introduce phase and impedance mismatch, which may degrade the overall performance. In stacked configurations, managing the voltage distribution becomes even more challenging, as uneven voltage sharing can lead to reduced efficiency or device failure [2]. To address these limitations in power combining, this work provides a chip-level verification of the differential power combiner proposed in [3] by implementing a single-stage Ku-band MMIC DPA fabricated using Infineon's GaN-on-Si HEMT technology. Moreover, the effect of the connection point of the high-impedance drain bias line has been considered. The fabricated DPA ranked well among the current state-of-the-art GaN MMIC DPAs in a similar frequency range and power class, demonstrating competitive efficiency and gain performance.

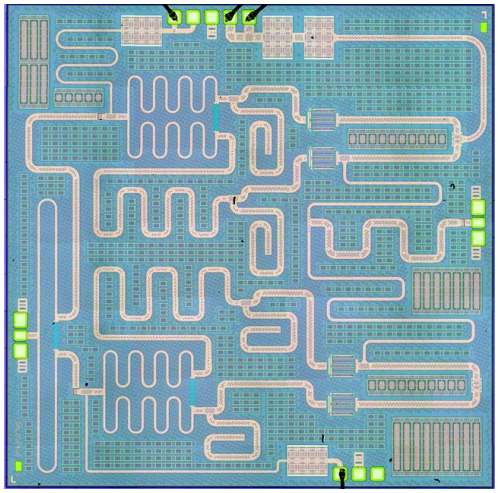

Fig. 1. MMIC chip photograph, Chip size is 4 mm × 4 mm.

II. Theoretical Analysis and Circuit Design

An improved version of Infineon's GaN-on-Silicon RF technology is utilized in this work. The process is implemented on high-resistivity 8-inch silicon substrates using a CMOS-compatible fabrication line, where the resistivity is preserved in the kΩ·cm range throughout epitaxy and processing to minimize RF losses in active and passive components. A scaled source-connected field plate is employed to enhance gain by reducing feedback and parasitic output capacitances. Furthermore, substrate thinning combined with a dense array of through-silicon vias provides efficient heat removal and a low-loss backside source connection. The measurement verified design kit ensures strong agreement between simulations and fabricated devices, enabling reliable circuit development and full exploitation of the technology's capabilities [4].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}}\left(1-\omega C_{\mathrm{OUT}} Z_0\right) & j\,\frac{1}{\sqrt{2}} Z_0 \\ j\,\frac{1}{\sqrt{2}}\left(2\omega C_{\mathrm{OUT}} - \omega^2 C_{\mathrm{OUT}}^2 Z_0 + \frac{1}{Z_0}\right) & \frac{1}{\sqrt{2}}\left(1-\omega C_{\mathrm{OUT}} Z_0\right) \end{bmatrix}^2 \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1}$$

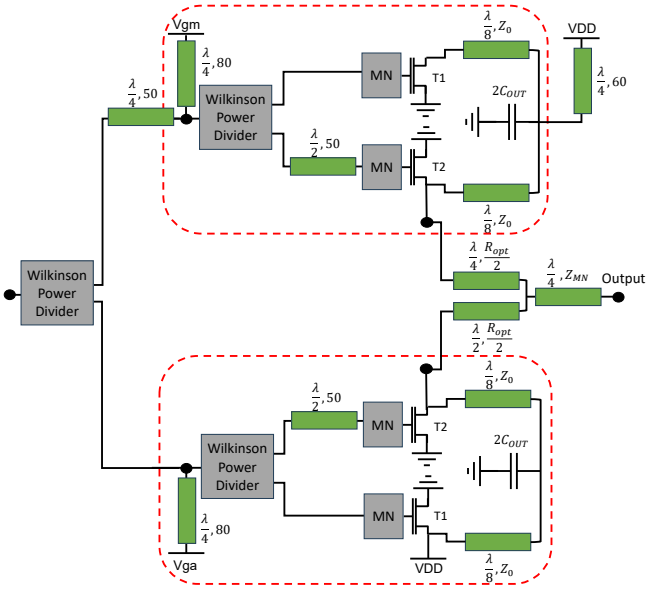

Fig. 2. Doherty Power Amplifier Architecture with Differential Power Combiner Cells as Main and Auxiliary Devices.

In this work, a Doherty power amplifier depicted in Fig. 2 is designed in which the main and auxiliary amplifiers are implemented using two identical transistors combined through the differential power combiner proposed in [3]. The effectiveness of this combiner is demonstrated through the fabrication and characterization of a prototype DPA.

Each transistor in the power combiner cell is modeled as a current source with an output parasitic capacitance, C_{out}. The differential power combiner consists of two $\lambda/8$ transmission lines with a characteristic impedance of Z_0 and a shunt capacitance of $2C_{\mathrm{out}}$ between them. The relationship for the drain voltages and currents of each device, represented by V_1, V_2, I_1, and I_2 in Equ. 1 is obtained from the ABCD matrix of each network element. By selecting the characteristic impedance Z_0 of the $\lambda/8$ transmission lines to match the impedance of the output capacitor C_{OUT}, $Z_0 = (\omega C_{\mathrm{OUT}})^{-1}$, the ABCD matrix expression simplifies considerably to:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ -\frac{1}{R} & -1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{2}$$

The corresponding Z-matrix of Equ. 2 shows that when $I_2 = -I_1$, each transistor sees an impedance of $2R$, effectively absorbed the parasitic C_{OUT} at the chosen frequency. However, practical implementation may be limited if the characteristic impedance Z_0 becomes excessively high or low. The $I_2 = -I_1$ condition is achieved by introducing a 180° phase delay in one branch after the Wilkinson power divider. While a Lange coupler with a 90° delay could provide a more compact implementation, the Wilkinson-based approach was used, allowing both transistors to be biased through the same divider. This eliminates the need for a separate bridge to bias the second branch, ensuring identical gate bias for both devices, and reduces mismatch.

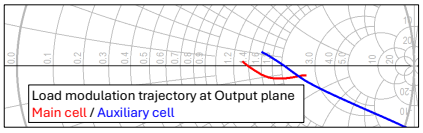

Fig. 3. Load modulation trajectory at the output of power combiner cell, main in red and auxiliary in blue.

Each branch employs a transistor with an active periphery of 4×160 μm. The corresponding device exhibits an output capacitance of $C_{\mathrm{OUT}} = 0.19$ pF. The operating frequency for the design is set to $f = 15$ GHz. Based on this value, the characteristic impedance required for the transmission lines in the combiner becomes $Z_0 = (\omega C_{\mathrm{OUT}})^{-1} = 55.8\ \Omega$. Furthermore, the total capacitance between the two lines is $2C_{\mathrm{OUT}} = 0.38$ pF. Assuming an optimal load impedance of $R_{\mathrm{opt}} = 130\ \Omega$ for each device, the impedance inverter in the Doherty architecture is designed with a characteristic impedance of $R_{\mathrm{opt}}/2 = 65\ \Omega$, resulting in an common load of $R_{\mathrm{opt}}/4 = 33.5\ \Omega$ for the DPA. A final post matching impedance inverter is required if the common load is not equal to $50\ \Omega$.

The load modulation trajectory of Doherty operation at output plane of combiner cells presented in Fig.3. The red trajectory represents the load modulation of the main amplifier, starting from approximately $131\ \Omega$ at low output power levels and moving toward $62.5\ \Omega$ at high power. This behavior is fully consistent with the values predicted during the DPA design.

The drain-bias line is implemented as a quarter-wavelength line at the operating frequency of 15 GHz. This bias line can, in principle, be connected at any node of the power combiner; however, when it is placed between the two $\lambda/8$ lines, exactly at the position of $2C_{\mathrm{OUT}}$, it yields an improvement of approximately 2.5 % in PAE together with a slight increase in output power. In Fig. 4, the impedance looking into the combiner at point 1 is equal to $R_{\mathrm{opt}}/2$, which in the equivalent implemented design corresponds to $(56.6 - j6.9)\ \Omega$, whereas the impedance seen from the middle of the combiner at point 2 is $(5.4 + j0.5)\ \Omega$, which is significantly lower than at point 1. Since the drain bias line is realized as a high impedance $\lambda/4$ transmission line, and it is short circuited with shunt capacitor, it generate a high impedance network with a large resistive component ($825\,\Omega$ in this design), connecting it at point 2 places the bias line in parallel with a much smaller impedance, which effectively reduces the overall loss contribution of the bias network and thereby improves the efficiency and output power.

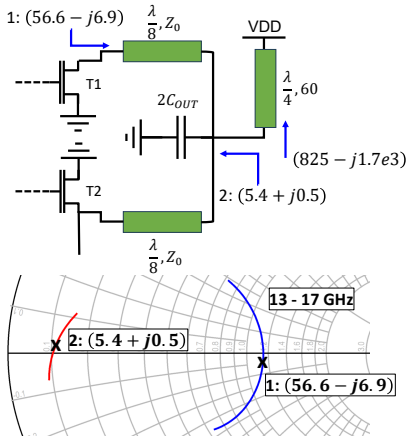

Fig. 4. Impedance seen at the input (point 1) and at the midpoint (point 2) of the differential combiner, illustrating the effect of connecting the high-impedance drain bias line at point 2.

III. Fabrication and Characterization

The fabricated MMIC DPA was mounted on an aluminum heatsink using a conductive epoxy to ensure proper thermal and electrical contact. The DC pads were wirebonded to a PCB and external bypass capacitors were added on the bias lines to improve low frequency stability and isolation. The amplifier was biased at $V_{DD} = 28$ V with a quiescent drain current of $I_{DD} = 31$ mA, while the auxiliary combiner cell operated at a gate voltage of $V_{ga} = -5$ V. RF measurements were performed by directly probing the MMIC pads, avoiding wirebond losses or mismatch. No stability issues were observed under either small- or large-signal excitation. Continuous-wave S-parameters were measured from 8 to 20 GHz and compared with simulations, as shown in Fig. 5. The results exhibit close agreement, confirming that the accurate EM stack-up definition provides highly correlated simulated and measured responses. Minor deviations only appeared in the input and output return losses. The input match stayed better than -10 dB from 8.5 to 17 GHz, and the DPA exhibited a maximum linear gain of approximately 9.4 dB at

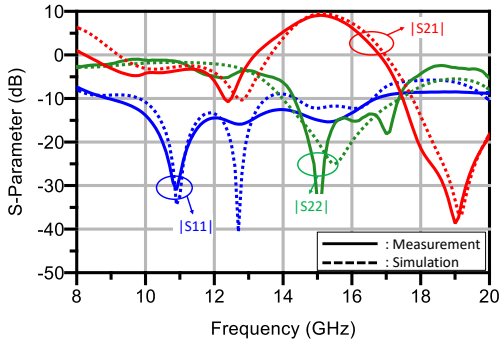

Fig. 5. Comparison between simulated (dash lines) and on wafer CW S-parameter measurement (solid lines).

15.1 GHz.

The large signal performance of the chip was characterized using a dual RF-pulse-width technique, where two pulse widths, $W_2 = 10$ μs and $W_1 = 5$ μs, were applied for each input power level, with a pulse period of $T_{\text{pulse}} = 200$ μs. The corresponding currents, I_2 and I_1, together with the quiescent current I_q, were measured. The DC current at each input power level was then calculated using the following equation:

$$I_{\text{DC}}(P_{in}) = (I_2(P_{in}) - I_1(P_{in})) \cdot \frac{T_{\text{pulse}}}{W_2(P_{in}) - W_1(P_{in})} + I_q(P_{in}) \tag{3}$$

Single-tone RF-pulsed power sweeps were performed across the 14.3 to 15.3 GHz band, with the corresponding results shown in Fig. 6. The efficiency profile over frequency indicates that the intended Doherty load modulation is correctly realized. Figure 7 presents the RF-pulse measured output power, PAE, and gain at saturation and at 6-dB OBO versus frequency from 14.3 to 15.3 GHz. A comparison with other MMIC DPAs operating in a similar frequency range is reported in Table 1. The DPA delivers more than 7.4 dB small-signal gain and above 37.7 dBm saturated power, while maintaining a PAE higher than 22.5 % at saturation and

Table 1. Comparison with state-of-the-art GaN MMIC DPAs with Similar Frequency Range

Item	**[5] / IMS 2022**	**[6] / MWCL 2017**	**[7] / TMTT 2025**	**[8] / MWTL 2025**	**This Work**
Technology	GaN/SiC	GaN/SiC	GaN/SiC	GaN/SiC	GaN/Si
Architecture	DPA	DPA	DPA	SLMBA	DPA
Supply Voltage (V)	20	25	22	20 & 24	28
Frequency (GHz)	14.5–17.2	13.7–15.3	14–16	14.5–15.5	14.3–15.3
Fractional BW (%)	17	11	13.3	6.6	6.7
Stages	2	1	1	1	1
Linear gain (dB)	13–18	5–7.4	6–8.5	5–7.4	7.4–9.4
P_{sat} (dBm)	34–34.5	34–36.5	35.4–36.1	35.2–35.9	37.7–38.7
PAE_{sat} (%)	20–26	20.3–32.8	27–30	18.5–21.1	28.7–32.3
PAE @ 6 dB OBO (%)	20–25	DE: 16–29	23–25	16.9–10.9	22.5–25
Chip size (mm^2)	3.6×2.9	3.1×1.6	2.5×3.6	3.1×3.6	4×4
Power density (W/mm^2)	0.27	0.9	0.44	0.34	0.47

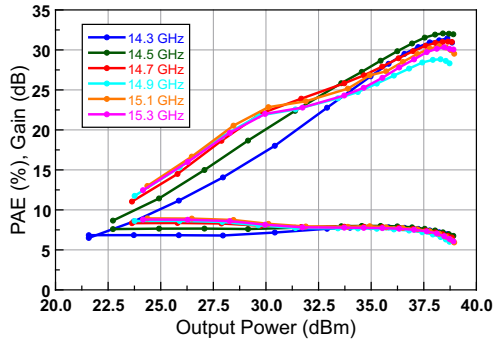

Fig. 6. Measured PAE (%) and Gain (dB) versus output power (dBm) at different frequencies from 14.3 to 15.3 GHz.

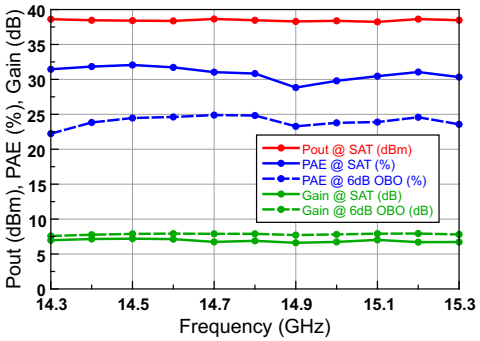

Fig. 7. Measured Output power at saturation (dBm), PAE (%), and gain (dB) at saturation and 6 dB OBO versus frequency (GHz).

at 6 dB OBO. The DPA demonstrates a maximum output power of 38.7 dBm at 14.7 GHz and a peak PAE of 32.3 % at 14.5 GHz. Overall, the achieved efficiency, gain, and power density demonstrate competitive performance relative to state-of-the-art GaN-SiC DPAs, indicating that GaN-Si technology is a viable platform for high performance MMIC power amplifiers.

IV. Conclusion

This paper has demonstrated the chip-level verification of a new differential power combiner capable of absorbing the parasitic output capacitance of the transistors in a Doherty power amplifier architecture. The proposed DPA was implemented using Infineon's GaN-on-Si MMIC process and achieves a peak output power of 38.7 dBm with a maximum PAE of 32.3 %. Measurements in the Ku-band from 14.3 GHz to 15.3 GHz show an output power between 37.7 and 38.7 dBm, saturation PAE ranging from 28.7 % to 32.3 %, and a 6-dB OBO PAE of 22.5 % to 25 %, corresponding to a 6.7 % fractional bandwidth. The measured performance shows good agreement with simulation results. These results confirm that the proposed differential power combiner, when implemented in GaN-on-Si technology, delivers competitive performance compared to state-of-the-art GaN-on-SiC DPAs. This demonstrates that GaN-on-Si is a strong and cost-effective candidate for realizing high-performance MMIC power amplifiers.

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