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Citation for the original published paper (version of record):
Domínguez-Hernàndez, M., Muñoz-Peña, P., Beza, M. et al (2026). Design of Multiport Converters for Distribution Grids: Sizing, Topologies and Control for Low and Medium Voltage Applications. IEEE Open Journal of Industry Applications, 7: 971-994.
http://dx.doi.org/10.1109/OJIA.2026.3720717

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IEEE Open Journal of
Industry Applications

Received 9 January 2026; revised 30 April 2026 and 24 July 2026; accepted 2 August 2026. Date of publication 6 August 2026;
date of current version 18 August 2026.

Digital Object Identifier 10.1109/OJIA.2026.3720717

Design of Multiport Converters for Distribution Grids: Sizing, Topologies, and Control for Low and Medium Voltage Applications

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This work was supported by the European Union's Horizon Europe research and innovation programme in the framework of the project "iPLUG" with Grant 101069770.

ABSTRACT The escalating penetration of distributed energy resources (DERs) presents significant operational challenges to low-voltage (LV) and medium-voltage (MV) distribution networks (DNs), particularly in terms of voltage stability and bidirectional power management. Multiport converters (MPCs) are an efficient, unified solution to aggregate diverse resources and enhance system resilience. This article proposes a multistage design of MPCs. An optimization-based methodology is presented for optimally sizing the MPC terminals, minimizing total economic cost while simultaneously optimizing technical indicators such as annual line losses and voltage stability. This methodology is validated across two distinct utility use cases: a four-terminal MPC in an LV network, which successfully integrates photovoltaic (PV) generation and EV charging, and a two-terminal MPC in an MV network thateffectively mitigates voltage imbalances between parallel feeders. Furthermore, the work reviews suitable MPC topologies for these grid applications and proposes a qualitative comparison technique implemented in a MV application. Finally, some control architectures for the proposed topologies are thoroughly verified through control hardware-in-the-loop (CHIL) and experimental converter prototype testing.

INDEX TERMS Multiport converters (MPCs), distribution grids, optimization, control.

I. INTRODUCTION

A. CONTEXT

The increasing penetration of distributed energy resources (DERs) throughout the distribution network (DN) is associated with significant operational issues, as well as some promising opportunities. New bidirectional power flows are impacting DN capacity. The low correlation and uncontrollability of renewable energy sources with respect to demand profiles are driving voltage deviations that push DNs to their limits [1], [2]. However, if the energy profiles can be better matched, DERs offer the local supply of load, which could improve efficiency and minimize network utilization. In addition, effective allocation and use of the DERs could improve DN resilience, which is becoming particularly desirable considering the increased frequency of extreme events that can isolate consumers from energy supply [3].

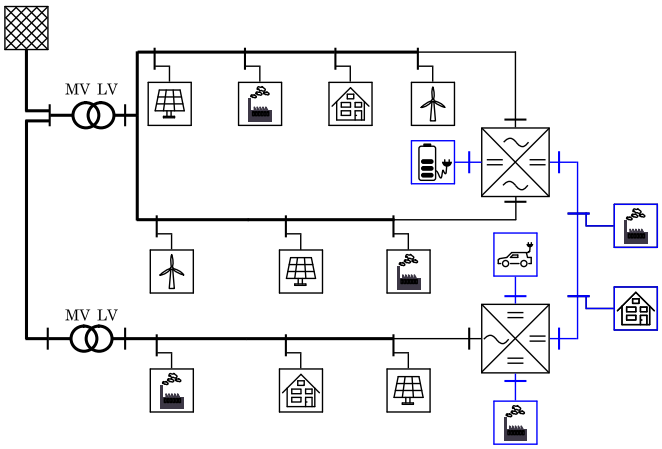

FIGURE 1. Example of application of a MPC in a DN.

The increased utilization of renewable energy sources and DC-connected devices (e.g., energy storage systems or electric vehicle chargers) requires a large number of conversion stages [4]. The conversion stages are conventionally implemented distinctly for each DER, each of which are associated with additional cost, losses, and space requirements. Aggregating the energy sources with different characteristic profiles to share converters could reduce these costs as well as increasing the utilization of the low carbon energy [5].

Multiport converters (MPCs) are a technology that can resolve many of these issues by integrating multiple resources into a single collocated device, as shown in Fig. 1. By sharing active and passive components between ports MPCs can reduce the number of components and improve the efficiency of multiple conversion applications [6]. As well as sharing components, MPCs can encourage the aggregation of energy between the integrated ports to reduce the use of DN capacity and maximize low carbon energy utilisation. This enhanced performance can be achieved with a low dependence on communication (and therefore minimizes the degradation of system resilience via cyber-attack) due to the collocation of energy sources.

MPCs require high port controllability to manage the energy flows internally and to maximize the benefit that the large energy capacity can provide to the connected DN [6]. The large energy capacities make MPCs suitable to operate as distributed grid-following or -formers, which could improve DN stability margins and offer islanded and black-start functionality to further improve the system's operating characteristics [7].

B. LITERATURE REVIEW

MPCs for DNs can be categorized into three main topologies: isolated, partially isolated, and nonisolated configurations [8]. MPCs with isolated ports are usually an extension of dual active bridge (DAB) configurations, where a high frequency transformer provides the galvanic isolation [9]. Partially isolated MPCs combine ports that are galvanically isolated with others that are directly connected to a common DC bus [10]. MPCs with nonisolated ports are typically an extension of back-to-back voltage source converter (VSC) configurations, where the ports are connected to a common DC bus, which can also be used as an additional DC port [11]. MPC control strategies are typically based on port-level control architectures while incorporating an additional control layer dedicated to the power sharing among N ports. This power-sharing layer plays a key role in coordinating energy flows depending on the converter topology [12], [13], [14].

MPC as a concept aims to integrate two existing power electronic solutions for DNs: soft open points (SOPs) [15], [16] and solid-state transformers (SSTs) [17]. SOPs are used in both LV [15] and MV DNs [18]. They typically serve to interconnect feeders and replace conventional normally open points in the network. SOPs can be implemented in either isolated or nonisolated configurations; however, the most common approach is based on back-to-back VSC topologies without galvanic isolation [11]. This is because galvanic isolation is usually not critical in these applications, and eliminating it reduces costs and complexity. SSTs mainly replace traditional transformers by enabling the interconnection of different voltage levels between LV and MV networks or within MV networks [19]. SSTs typically provide galvanic isolation through a medium-frequency transformer, as isolation is an essential feature for ensuring safety, compliance with regulations, and achieving functional equivalence to conventional transformers [20].

C. RESEARCH GAPS AND ASSUMPTIONS

It should be noted that a comprehensive review of MPC topologies for DN applications has been presented in [8]. In addition, this work presented a methodology to qualitatively compare MPCs for DNs applications. However, the methodology presented is purely conceptual and does not consider real DN conditions.

Therefore, this article addresses the entire design chain in real DNs, encompassing sizing, a precise qualitative topology selection, and experimental validation. While prior work has investigated individual aspects of MPC design [8], [21], [22], integrated methodologies that cover the full development process implemented in real DN conditions remain limited in the literature. In particular, existing studies typically focus either on converter sizing, topology assessment, or control implementation. In contrast, this work, as shown in Fig. 2 proposes an application-driven design framework in which network operating conditions are first translated into MPC power and voltage ratings through optimization, these requirements are then used to guide topology and controller selection, and finally the obtained solutions are validated through CHIL and experimental testing.

Regarding control implementation, this work does not aim to compare control strategies. A meaningful comparison of controllers would require dedicated design, tuning, and optimization efforts for each topology, introducing additional degrees of freedom and potentially biasing the results toward control-specific performance. Such an analysis falls outside

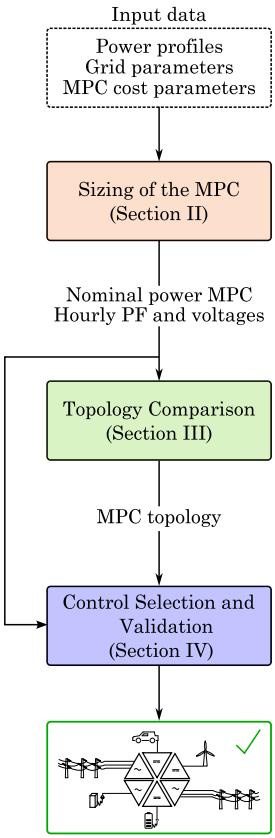

FIGURE 2. Proposed workflow for the design of MPCs in DGs.

the scope of this study. Instead, well-established and validated control solutions are adopted for each topology to ensure proper operation and enable experimental validation under realistic conditions. This choice avoids introducing additional control design variables and allows the study to remain focused on assessing the proposed design methodology and the intrinsic characteristics of the converter topologies, ensuring a fair and consistent basis for comparison.

D. CONTRIBUTIONS

Accordingly, this article presents a comprehensive analysis of MPCs design for LV and MV DNs, covering converter power sizing, converter topology selection, and final experimental validation. The main outcomes of the article are as follows.

1) A complete application-driven MPC design chain that links network-level requirements, converter sizing, topology selection, and experimental validation.
2) Definition of two benchmark models in LV and MV applications for sizing the rated power of MPC terminals.
3) A methodology to qualitatively compare MPCs, which is tested in the defined benchmark models in LV and MV.
4) Implementation and validation of experimental setups for the validation of selected topologies.

Although the optimization methods presented in this article are validated for a specific number of terminals, the underlying approach is equally applicable to an arbitrary number of AC or DC terminals. Each additional port can be incorporated by extending the power balance constraints and including the corresponding decision variables (e.g., rated power and power flow variables) within the same framework. The objective function remains unchanged, while constraints such as voltage limits, current limits, and converter operating limits are applied per port, allowing a straightforward extension to multiport configurations.

TABLE 1. Optimization Runtime According to the Number of Days Considered in LV Use case

Number of representative days	Optimization runtime
1	2.7s
2	6.5s
3	10s
4	17s
5	25s
6	94s
7	61s

E. STRUCTURE

The article is structured as follows: Section II presents the methodology for MPC power sizing and shows two use cases for LV and MV networks based on real systems. Section III reviews the MPC topologies that can be considered for LV and MV applications and presents a comparative evaluation of the isolated MV topologies based on different indicators. Section IV presents the implementation of the converter control for the topologies selected in Section III and shows the experimental setups and results used to validate the converters. Finally, Section V concludes this article.

II. MPC POWER SIZING FOR DISTRIBUTION GRIDS

This section presents two benchmark models in LV and MV applications representing case studies based on real distribution system operator (DSO) information. An optimization-based methodology is applied to these case studies for sizing the rated power of MPC terminals considering AC power flow constraints.

A. SIZING METHODOLOGY

This section presents a methodology for sizing the rated power of MPC ports in DNs. Fig. 3 shows a flowchart of the proposed methodology with physics-based models. The nominal power of the MPC terminals is determined through an optimization that considers the hourly load and generation profiles, as well as grid constraints as AC power flow equations. The optimization can include different elements aside from the MPC: the grid, the loads, and the generator units.

Several representative days are considered, since optimization with complete annual data has high computational requirements. Therefore, the optimization runtime is in the order of seconds to minutes (Table 1 shows an example). To select the representative days, an unsupervised machine

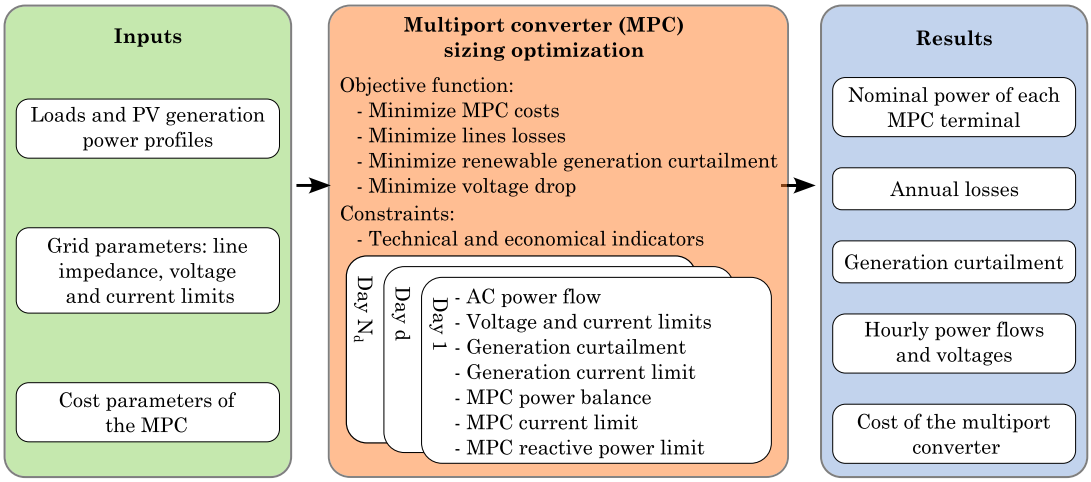

FIGURE 3. Flowchart of the grid-based MPC sizing methodology.

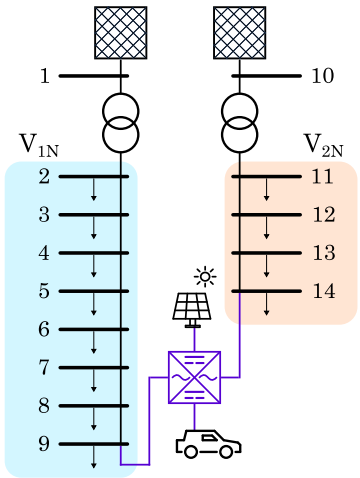

FIGURE 4. LV benchmark model based on simplified Anell LV network with potential MPC location, where V_{1N} is 400 V and V_{2N} is 230 V.

learning clustering methodology for time-series data [23] is applied. However, alternative clustering methodologies can also be considered.

The optimization mainly provides the rated power of the MPC terminals, but also economic and technical indicators for the system performance that can be used to evaluate the advantages of installing an MPC. More details about the optimization formulation are found in [21]. MPC constraints specifically include active power balance between all terminals, as well as current limits and reactive power limits for the AC ports. Current limit of a MPC port is defined as the maximum current that the network to which it is connected can manage, and each MPC terminal should be capable of exchanging reactive power with a minimum capability of ±44 % following IEEE Standard 1547 [24].

The optimization aims to size the MPC and, at the same time, improve network performance. Where network operation optimization can be defined by the following technical indicators.

1) Minimize photovoltaic (PV) curtailment or, equivalently, maximize annual PV generation (E_{ren}).
2) Minimize annual line losses (E_{loss}).
3) Minimize voltage drop (ΔV).

Therefore, the objective function can be expressed as follows.

$$[\min] \sum_{k} S_{n,MPC-k} + \sum_{i} O_i \cdot w_i \tag{1}$$

where $S_{n,\mathrm{MPC}-k}$ is the nominal power of the MPC terminal k, O_i represents the ith optimization objective, and w_i is the weight factor of the ith objective function term.

B. PRESENTATION OF USE CASES

This section presents two use cases for LV and MV networks from Anell, which is a small Spanish DSO located in Catalonia area. These two examples were suggested by Anell as potential use cases were MPCs can improve energy management in the DN. As a result, these use cases have been generalized as benchmark models to analyse these two MPC applications.

1) ANELL LV NETWORK

In this case, the MPC is used to interconnect two LV feeders at voltage levels V_{1N} and V_{2N}, as shown in Fig. 4, where Anell is operating at 400 and 230 V, respectively. Furthermore, the DSO is planning to install up to 100 kW of solar generation and an EV charging station with a maximum power of approximately 9 kW in the same area. These two devices would be connected to a DC terminal of the MPC. Tables 2 and 3 present the line and transformer parameters of the LV network, respectively. Also, the maximum current is supposed 344 A for all lines. The EV profile corresponds to the sum of 4 years of available data and represents a single charging point.

2) ANELL MV NETWORK

This section presents a case where the MPC is used to interconnect two MV feeders at 20 kV that have a significant

TABLE 2. Line Parameters of LV Use Case

From bus	To bus	R [mΩ]	X [mΩ]
2	3	14.94	16.8
3	4	9.5	10.66
4	5	4.6	5.15
5	6	2.78	3.1
6	7	3.94	4.41
7	8	3.18	3.55
8	9	4.73	5.28
11	12	3.95	3.01
12	13	8.91	10
13	14	26.64	29.92

TABLE 3. Transformer Parameters of LV Use Case

V_2 [V]	Z_{tr} to V_2 side [mΩ]	S_{rated} [kVA]
400	8.7+j21.75	250
230	1.64+j5.39	400

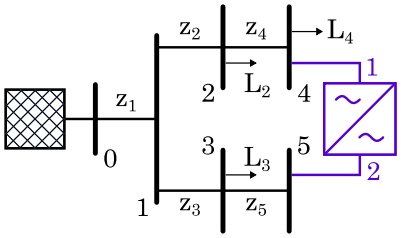

FIGURE 5. MV benchmark model based on simplified Anell MV network with potential MPC location.

TABLE 4. Line Parameters of MV Use Case

From bus	To bus	R [Ω]	X [Ω]
0	1	0.027	0.27
1	2	1.1832	1.3517
1	3	2.4329	2.7595
2	4	2.5865	3.0808
3	5	3.225	3.8381

voltage difference. For example, Anell proposed a use case where one feeder has a voltage drop of 5 % and the other feeder has a voltage drop of 15 %. In this case, the MPC aims to reduce the voltage difference between the last bus of the feeders. Fig. 5 shows the specific use case proposed, Table 4 presents the line parameters, and Fig. 6 shows the load profiles of six representative days with weights on Table 5.

C. SPECIFICATIONS OF MPC POWERS FOR THE USE CASES

1) ANELL LV NETWORK

This section presents the results for the Anell LV network. In addition, the MPC installation is evaluated and compared in several scenarios as follows.

1) *Scenario 1:* Grid without MPC.

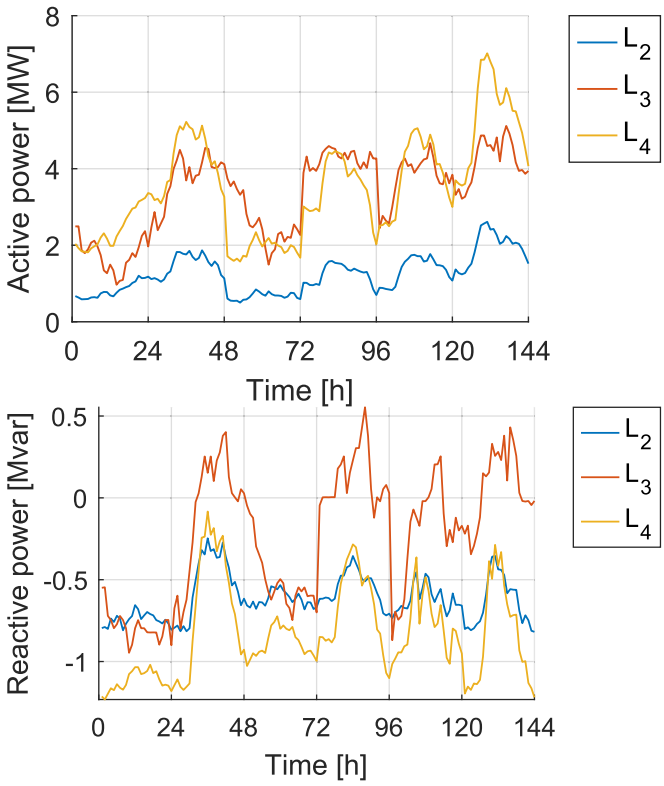

FIGURE 6. Loads profiles for six representative days of MV use case.

TABLE 5. Representative Days of the MV Use Case

Day	Weight
1	25.78 %
2	13.28 %
3	7.42 %
4	11.33 %
5	8.2 %
6	33.98 %

2) *Scenario 2:* Grid with MPC and without integration of PV generation and EV loads.
3) *Scenario 3:* Grid with MPC and integration of PV generation and EV loads.

In this case, the objective of introducing the MPC is to integrate the PV and EV, maximizing PV generation. The objective function is defined as an economic expression that includes MPC capital cost and PV energy revenues. Therefore, the objective function can be expressed as

$$[\min] \sum_k C_{conv-k} \cdot S_{n,MPC-k} + E_{ren} \cdot C_{en} \cdot t_{life} \qquad (2)$$

where C_{conv-k} is the unitary cost of the MPC terminal k, supposed as 150 €/kVA [25], C_{en} is the average annual energy selling price, supposed as 0.05 €/kWh, and t_{life} is a factor to weight CAPEX and OPEX, supposed as 30 years. These weights justify the tradeoff between MPC capital cost and PV

TABLE 6. Specification of Rated Powers and Voltages for the Anell LV Network Use Case

Port	U_n (RMS)	I_n (RMS)	S_n (RMS)	P_n
AC 1	400 V	63.5 A	44 kVA	N/A
AC 2	230 V	50.2 A	20 kVA	N/A
DC 3	N/A	N/A	N/A	65 kW
DC 4	N/A	N/A	N/A	9 kW

curtailment, while annual losses and voltage improvements are just considered as indicators but they are not optimized.

The initial scenario considers only the 400 and 230 V feeders, without interconnection. In this scenario, voltages range between 0.99 and 1 p·u· on both networks, i.e., voltage deviations are not relevant. As expected due to the loads, the first upstream bus on both networks exhibits a significant voltage drop, while the other downstream buses exhibit low voltage drops.

Then, a second scenario considers the introduction of a two-terminal MPC, connecting bus 9 to port 1 and bus 14 to port 2. In this scenario, the MPC operates similarly to a SOP. In this case, without PV, only a small two-terminal MPC of approximately 2.3 kVA is required to provide reactive power and transfer active power between 230 to 400 V feeder. However, in this case, connecting both networks does not provide significant improvements compared to the initial scenario.

Finally, a third scenario is considered introducing the PV generation and the EV charging station. As a result, a four-port MPC is installed, where port 3 is connected to PV generation and port 4 to EV charging stations. The rated powers of the MPC terminals are ranging between 9 and 65 kVA as indicated in Table 6. It can be concluded that the nominal power of the port connected to the EV charging station corresponds to the peak load and the nominal power of the other ports are directly related to the amount of PV generation connected to the MPC. In fact, PV generation curtailment (around 3%) is applied in order to provide the best cost-effective solution of the MPC, which enables to reduce the nominal power of port 3. For the selected days, the maximum PV power available is 80.5 kW, although installed power is 100 kW. Then, port 3 nominal power results in 65 kW, which is around 20% less than the maximum PV available. This practice, known as peak clipping, is common to balance the PV generation and the cost of the associated converter.

Due to the introduction of PV generation, the 400 V feeder exports active power to the main MV network, while the 230 V feeder is importing at the same time. The PV generation is injected to both LV networks through the MPC, for that reason the currents and voltage levels increase significantly in the buses close to the MPC, specially on the 400 V network. The MPC integrates efficiently the PV generation, as shown in Fig. 7, by injecting twice as much power to the 400 V feeder than to the 230 V feeder with the objective of minimizing the losses. The EV charging station is also effectively integrated in the MPC, although it represents only a small load, and most

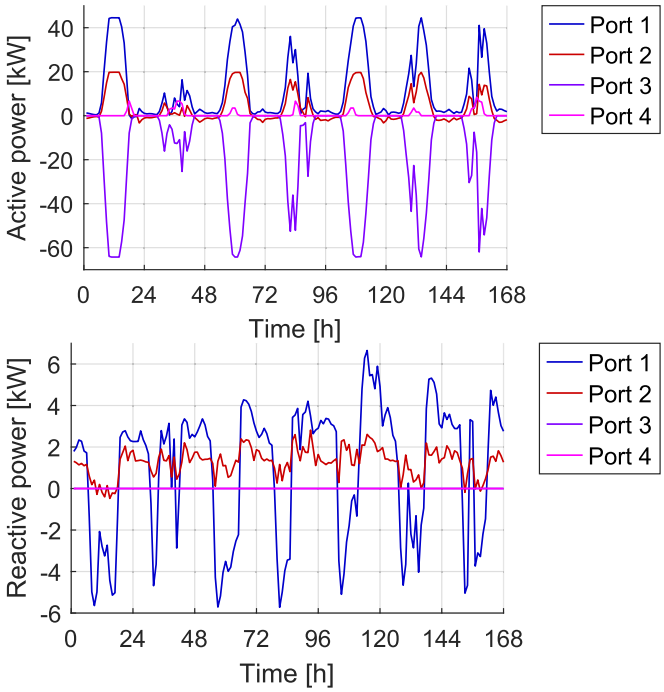

FIGURE 7. Active and reactive power of the MPC terminals for LV use case in the four-terminal MPC scenario.

of the time the EV load is supplied by the PV generation. In this scenario, the MPC also has an important role in reactive power management, as it provides around 1.5 kvar to the 230 V feeder, and can provide or absorb up to 6 kvar to the 400 V feeder. Introducing PV generation and EV loads results in an interesting scenario of MPC application for LV networks.

Regarding the technical indicators, introducing PV generation increases the losses by 34%, compared with scenario 1, due to the export capacity of the system. The increase in losses is related to higher current flows from PV to the external grid than from the external grid to the loads in the initial scenario. On the other hand, integrating PV generation in the MPC, do not lead to significant changes in voltage drop. Although the limited voltage drop improvement and losses increase, MPC installation is justified to efficiently integrate PV and EV, while interconnecting both LV feeders rather than grid operation improvements.

Future work on this use case could include resizing analysis of the lines to efficiently accommodate the PV surpluses. Also, higher EV loads can be considered, such as public or semi-public EV charging stations rather than a single EV, to evaluate the integration of the MPC and PV.

2) ANELL MV NETWORK

The results of MV Anell network are presented in this section. In this case, the objective is to reduce the voltage difference between buses 4 and 5, which can be expressed as

$$[\min] \sum_k S_{n,MPC-k} + V_{4-5} \cdot w \tag{3}$$

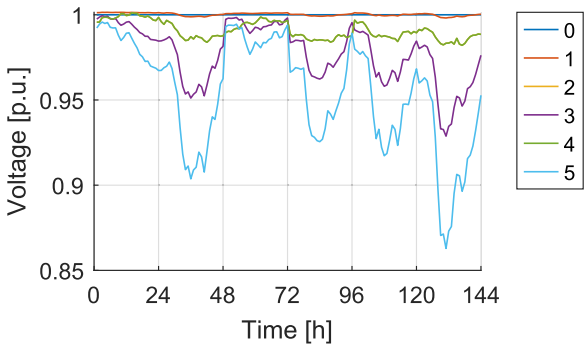

FIGURE 8. Bus voltages for MV use case without MPC.

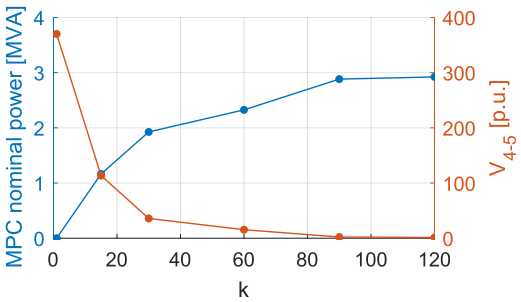

FIGURE 9. MPC nominal power and the objective function term of the voltage difference for different weights on the objective function on MV use case.

TABLE 7. Specification of Rated Powers and Voltages for the Anell MV Network Use Case

Port	U_n (RMS)	I_n (RMS)	S_n (RMS)
AC 1	20 kV	84.4 A	2.93 MVA
AC 2	20 kV	84.3 A	2.92 MVA

where V_{4-5} represents the equivalent annual sum of the voltage difference between the buses to which the MPC will be connected.

The initial scenario, shown in Fig. 8, without feeders interconnection thorough MPC, shows that bus 5 has an important voltage drop, and the voltage difference between the feeders is significant. These results have been validated with Anell, as the DSO observes voltage drops between 5% and 15% without the MPC interconnection.

In this case, a sensitivity analysis is performed. Fig. 9 demonstrates that MPC size depends on the weighting factor w of the objective function, showing that with lower importance of the MPC cost, the MPC nominal power will increase and the voltage difference between buses 4 and 5 will be reduced. Figs. 10 and 11 show the hourly voltage difference reduction for each hour and how the voltage of bus 5 is increased thanks to a bigger MPC. Taking as an example the scenario where k is 120 and the specifications are the ones shown in Table 7. Fig. 12 shows that the MPC enables active power flow from the high-loaded feeder to the low-loaded feeder. Future work on this use case can include the MPC

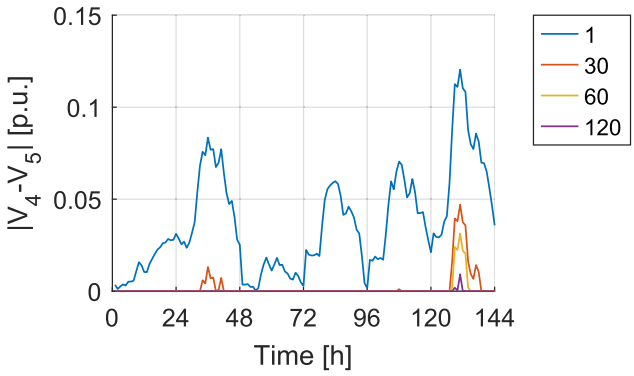

FIGURE 10. Voltage difference between buses 4 and 5 for different weights on the objective function on MV use case.

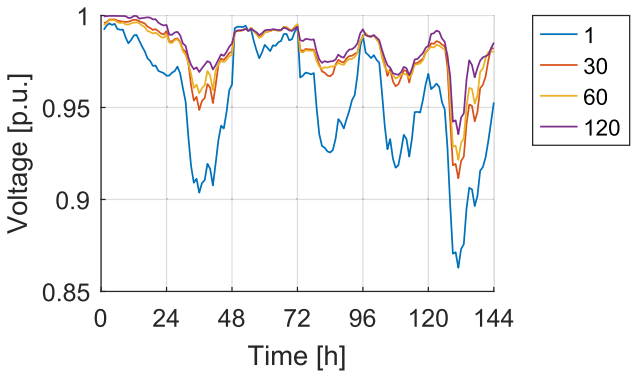

FIGURE 11. Voltage of bus 5 for different weights on the objective function on MV use case.

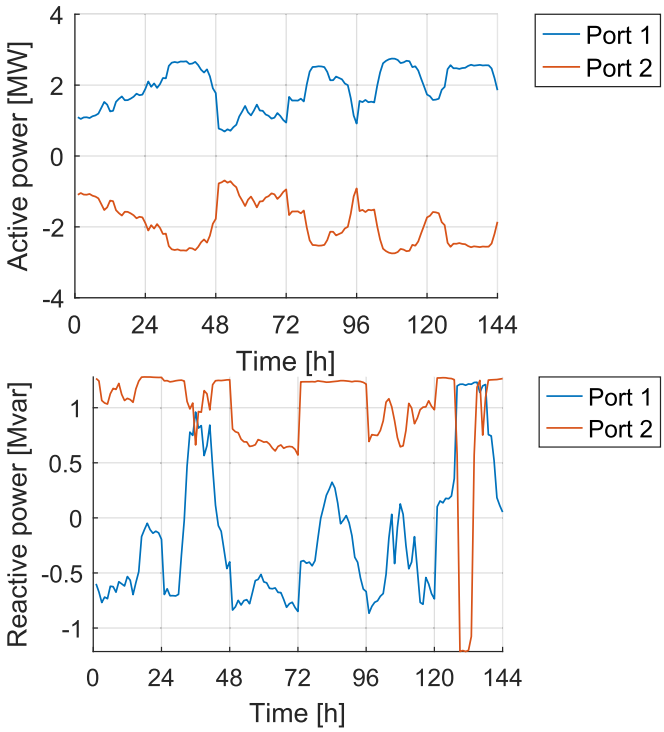

FIGURE 12. Active and reactive power of the MPC terminals with $k = 120$ for MV use case.

sizing based on installation cost, physical size, and practical deployment feasibility.

3) GENERAL REMARKS FROM CASE STUDIES

Although the previous results correspond to Anell network, these case studies were selected as representatives after a preliminary screening of the DSO network. Therefore, general conclusions can be applied to other DSO networks facing similar challenges:

1) When integrating PV and EV through the MPC, the nominal power of the port connected to the EV charging station corresponds to the peak load and EV load can be directly supplied by the PV generation. If PV is much higher than EV, the nominal power of the AC ports is directly related to the amount of PV generation connected to the MPC.
2) The MPC integrates efficiently the PV generation by injecting more power to the feeder with higher voltage level with the objective of minimizing the losses. And if the feeders have significant differences in voltage drop, the MPC enables active power flow from the high-loaded feeder to the low-loaded feeder, reducing the voltage difference between the feeders. The MPC also has an important role in reactive power management.
3) MPC size is highly dependent on the weighting factors of the objective function and they are modified according to the MPC application and scenario.

III. COMPARISON OF MPC TOPOLOGIES FOR DNS

Section II defined the power-sizing requirements for MPCs based on the real use cases in LV and MV DNs. This section shifts the focus to power-electronic aspects and introduces a methodology for selecting suitable MPC topologies based on the application voltage level and the requirement for port isolation. Given that the objective of this section is to present a comparison methodology for MPC topologies, an exhaustive analysis of all possible solutions is beyond its scope. It is worth noting that [8] already provides a comprehensive review of a wide range of converter configurations. Therefore, this work focuses on a subset of topologies that rely on state-of-the-art port converter technologies, thereby ensuring both relevance and practicality.

A. STUDIED TOPOLOGIES FOR LV APPLICATIONS

MPCs for LV DNs cannot be understood without the concept of SOPs, i.e. as an initial two-port option. SOPs emerged as a transformative solution for enhancing flexibility and controllability in LV radial DNs [26]. SOPs are power electronic interfaces that replace passive or normally open points between feeders with actively controllable links [27], [28]. Unlike traditional mechanical switches, SOPs enable dynamic regulation of active and reactive power flows, asynchronous interconnection, feeder decoupling, voltage balancing, and phase coordination. These capabilities are particularly valuable in modern grids with high penetration of DERs, where SOPs can mitigate voltage violations, enhance load sharing, and support ancillary services. Moreover, advanced SOP architectures can perform phase balancing, provide fault isolation, and even contribute to grid-forming functionalities during islanded operation [29].

Although SOPs are primarily designed for AC–AC coupling between feeders, their modular architecture also facilitates the integration of renewable energy sources and energy storage systems, thereby broadening their applicability and enhancing the hosting capacity of DERs in DNs [30]. Configurations with more than two ports more accurately reflect the concept of an MPC and are referred to in the literature as enhanced soft open points (ESOPs).

SOPs are most commonly built using nonisolated back-to-back VSCs. This arrangement is preferred because it offers high efficiency, low capital cost, and relatively simple implementation, making it well-suited for LV DN applications. Consequently, although isolated MPC-based SOPs, also named SSTs, have also been reported in the literature [31], [32], [33], nonisolated topologies remain the most widely adopted in practice. However, it should be noted that isolated configurations may be necessary in LV cases, particularly in instances where, due to safety or standards compliance requirements, galvanic isolation is required.

1) NONISOLATED CONFIGURATIONS

Nonisolated MPCs with multiple AC ports are typically based on AC–DC VSCs connected to a common DC bus. Therefore, the choice of AC–DC VSC plays a critical role in determining the overall performance of the SOP or MPC. The most relevant topologies include the two-level (2 L), three-level (3 L), and four-wire (4 W) VSCs, as illustrated in Fig. 13.

The two-level VSC (2L-VSC), shown in Fig. 13(a), remains the most established and widely adopted option for power conversion in LV DNs, including SOP implementations [27], [28]. Its simple architecture, consisting of three half-bridge (HB) legs and three boost inductors, enables a compact, cost-effective, and mature solution for bidirectional power flow control. In SOPs, it is often used in back-to-back configurations. However, its inherent two-level voltage waveform results in higher switching ripple and harmonic distortion unless high switching frequencies or advanced modulation techniques are applied. Moreover, commutation at the full DC-link voltage increases switching losses, creating a trade-off between simplicity and efficiency.

To improve performance, three-level VSCs (3L-VSCs), such as the T-type configuration in Fig. 13(b), introduce an intermediate voltage level [34]. By adding a bidirectional switch in each leg, the T-type reduces voltage stress across devices and improves the quality of the output voltage waveform. This allows smaller AC-side filters, leading to a more compact design [35]. In SOP applications, 3L-VSCs enable more precise power flow control with reduced current distortion. Although they introduce additional complexity in terms of hardware and control, they strike a better balance between efficiency, waveform quality, and compactness [36].

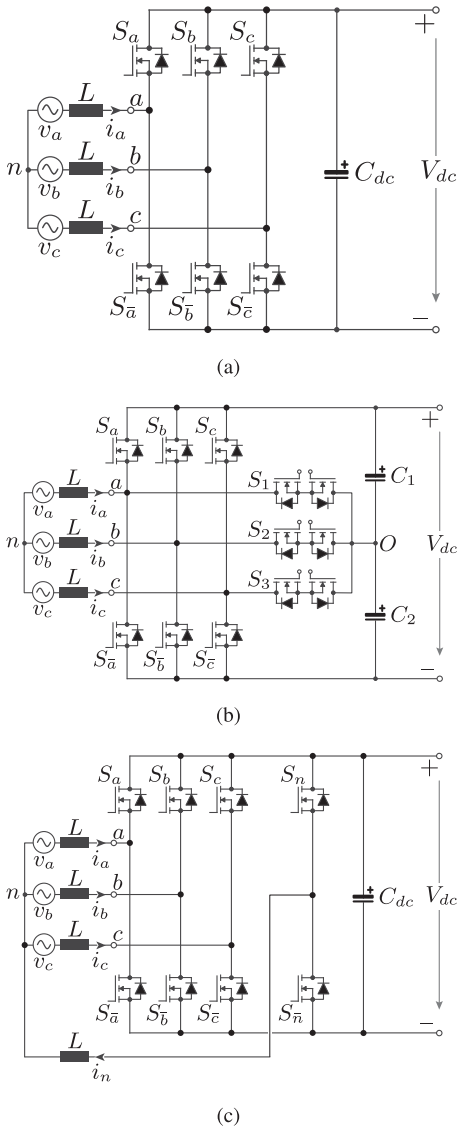

FIGURE 13. Schematics of common VSC topologies adopted in SOPs: (a) 2L-VSC; (b) T-type 3L-VSC; (c) 4w-VSC.

For applications requiring neutral current regulation and unbalance compensation, the 4W-VSC, depicted in Fig. 13(c), provides an extended capability by including an additional leg for neutral control. This enables effective support for single-phase and nonlinear loads and allows phase-balancing functionalities in radial LV networks where neutral shifts and imbalances are common [37], [38], [39]. Despite the added cost, higher switch count, and more sophisticated control requirements, the 4W-VSC offers superior performance in terms of power quality and reliability, making it an attractive choice for SOP applications in unbalanced distribution grids [40].

2) PARTIALLY ISOLATED AND ISOLATED CONFIGURATIONS

In fully isolated configurations, SSTs are commonly implemented using double active bridge (DAB) topologies [31], while MPCs with three or more ports typically rely on triple active bridge (TAB) topologies, as shown in Fig. 19 [14], or multiple active bridge (MAB) [9]. In addition, the DC ports of these active bridge converters are usually interconnected with the AC grid via the AC–DC converter structures described in Section III-A.1. In the case of partially isolated configurations, no solutions have been found in the literature for LV DN applications.

B. STUDIED TOPOLOGIES FOR MV APPLICATIONS

MV SOP applications have similar objectives as those outlined for LV SOPs. Of these objectives, some important features outlined for sub-transmission cases are the rebalancing of feeder loads and the mitigation of voltage differences to improve network utilisation and efficiency. MPCs can be particularly desirable for these applications due to their ability to integrate additional DERs that can increase local network utilization and provide capacity for network support.

Despite the similar objectives, the higher voltage level can increase the cost and complexity of the MPC. Scalability becomes increasingly important to integrate MV ports, while voltage gain becomes critical when integrating the MV ports with LV ports. Although high voltage gain nonisolated solutions are being explored for ultra-LV to LV applications [41], galvanic isolation may be required for the safe integration of MV to LV ports [42], [43]. Similarly, fault tolerance is important for the robust operation of an MPC with MV and LV ports. These characteristics closely align with those of SST topologies, which employ isolated power electronic configurations to achieve robust voltage gain and power-flow management [44].

1) NONISOLATED CONFIGURATIONS

Nonisolated solutions for the MV application generally resemble collocated groups of independent nonisolated converters. Their scalability offers the effective integration of MV ports. Nonisolated MPCs based on 2L-VSCs or 3L-VSCs, suffer from significant limitations, including high switching losses, the requirement of larger AC filters to reduce total harmonic distortion (THD), and limited fault tolerance capabilities [15]. The most suitable solution proposed in the literature is then using a MMC-based nonisolated MPC [45]. However, due to the lack of isolation, all ports are coupled on the DC bus, which could lead to several issues, especially under fault conditions. However, MMCs can mitigate the coupling with an adequate control [46]. In addition, it should be noted that the multiple independent conversion stages are associated with a large number of components [8].

2) ISOLATED CONFIGURATIONS

Fully isolated solutions use a transformer to achieve galvanic isolation between ports. The intermediate transformer stage provides a method to step the voltage up/down between ports, an effective means for fault limitation [47], and limits the harmonic transfer between the LV and MV ports [27]. However, ports are coupled with each other, which drives increased

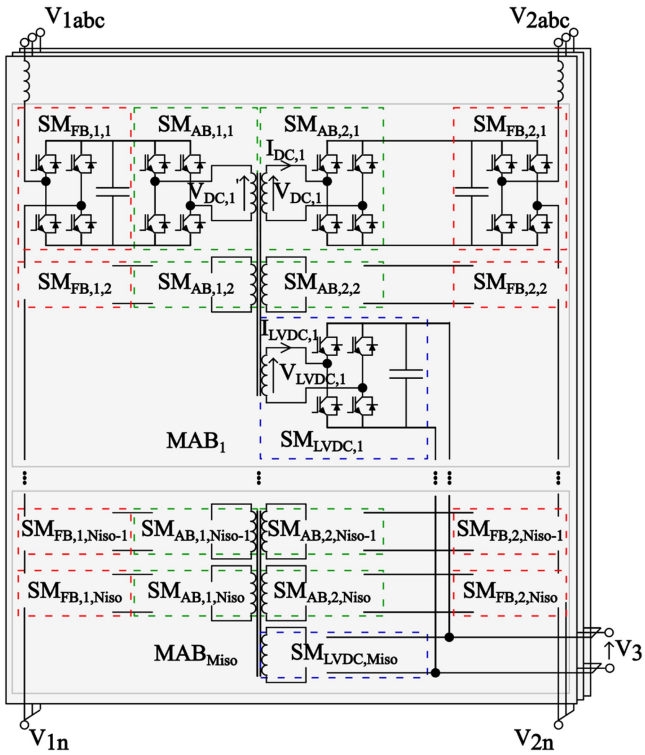

FIGURE 14. Isolated multi-MAB configuration derived from [48].

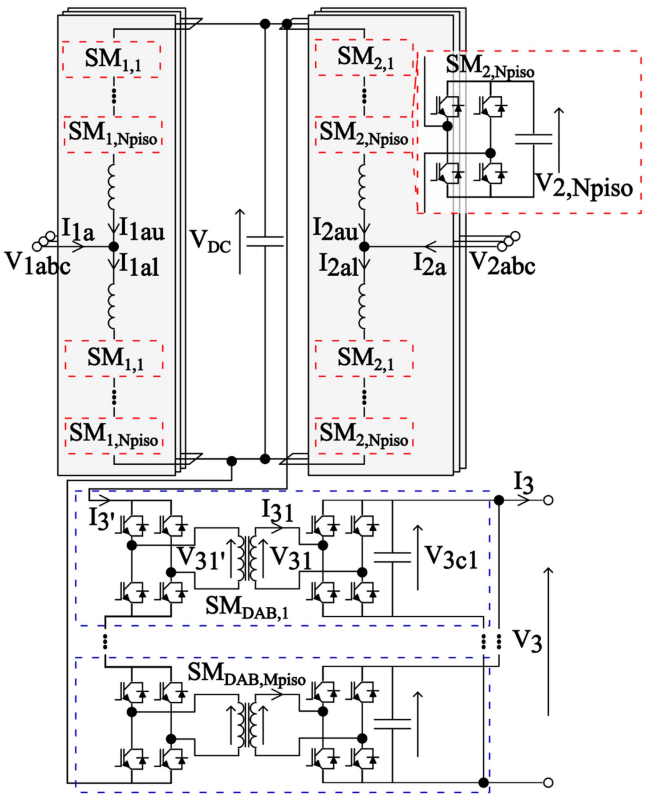

FIGURE 15. Partially isolated back-to-back FB MMC with ISOP DAB stage.

operational complexity with the number of ports [13]. In addition, the number of components is expected to increase significantly as higher voltage ports are integrated.

Triple- or multi-active-bridge (MAB) modules are required to be stacked to scale a fully isolated topology to fit the MV ESOP application as exhibited in Fig. 14 (derived from [48]). The configuration offers flexibility to accommodate different port voltage and current characteristics, benefits from galvanic isolation between all ports, and provides decoupled LV DC voltages at the output. The output LV DC voltages can be converted to a MV AC voltage using a simple and low component (relative to other multilevel solutions) Cascaded H-bridge (CHB) converter [49], [50]. While alternate configurations can be derived from [48], the solution pictured in Fig. 14 is deemed to be most suitable due to its relative low number of components.

3) PARTIALLY ISOLATED CONFIGURATIONS

Partially isolated solutions may offer a mixture of the benefits of non- or fully isolated MPCs. Highly scalable, controllable, and potentially fault-tolerant nonisolated stages can be used for the AC/DC conversion while effective voltage gain isolated stages can be used to integrate ports with widely different voltages without compromising too significantly in terms of cost and size. It is expected that a partially isolated topology will establish an intermediate DC voltage between the non- and fully isolated stages.

The requirement for partially isolated topologies to establish an intermediate DC voltage requires the use of a MMC instead of a CHB for the AC/DC stage. The MMC will increase the number of associated components. A choice must also be made between half- or full-bridge (FB) submodules (SMs) for the MMC. Although FB SMs further increase the number of components for the AC/DC stage, they offer high fault tolerance, the ability to operate in AC voltage gain mode, and increased redundancy [44], [51]. The AC voltage gain mode increases the topology's flexibility to operate with different AC port voltages and a lower intermediate DC voltage, which could reduce the number of components required for the isolated DC/DC stage [52].

The isolated DC/DC stage could use an inverted back-to-back MMC configuration (transforming MV DC to LV DC via an intermediate isolated AC transformer), known as the isolated modular-multilevel-DC-converter. This configuration possesses similar fault tolerance as a conventional MMC [53] but may be associated with a large number of components. Alternatively, an input-series output-parallel DAB (ISOP DAB) configuration may offer an efficient and controllable solution that is more suited to the voltage and current characteristics of the ESOP application [47], [54]. An example of the resulting partially isolated topology using back-to-back FB MMC AC/DC stages and an ISOP DAB DC/DC stage is pictured in Fig. 15.

C. METHODOLOGY TO COMPARE TOPOLOGIES

The high-level discussion of suitable topologies for DN applications in Section III-A and III-B identifies the most feasible

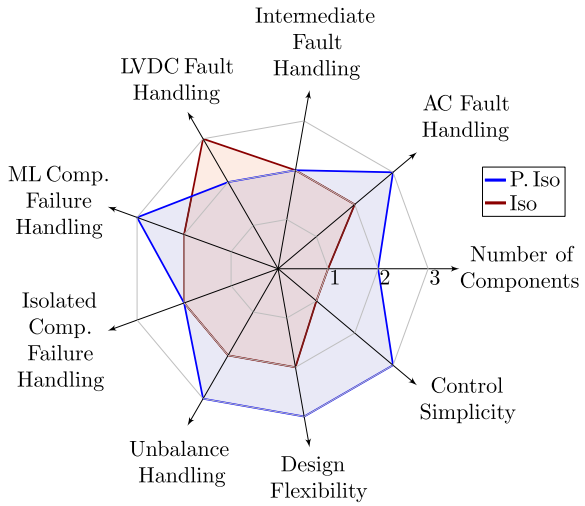

FIGURE 16. Qualitative scoring of MV topologies.

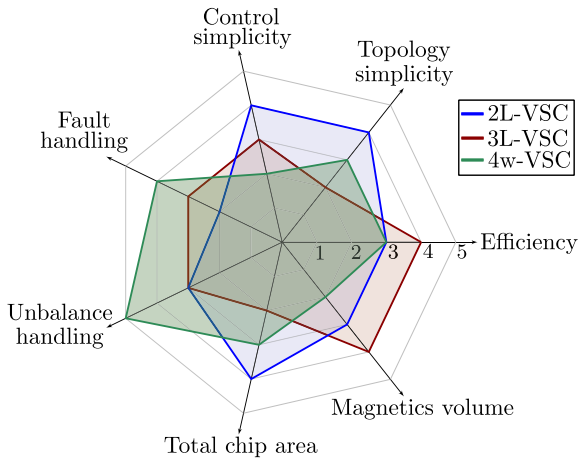

FIGURE 17. Comparative evaluation of the three candidate VSC topologies using a radar diagram where the larger covered area corresponds to superior performance.

topologies for LV and MV conditions. Depending on whether isolation is required, different topologies can be selected. In order to enable a consistent and time-efficient screening at an early design stage, the comparison is primarily based on qualitative criteria. It should be noted that detailed analyses of losses, efficiency, and reliability are not included at this stage, as they require defining specific devices, operating conditions, and control strategies for each topology. Such analyses are instead intended for a subsequent design phase, once a candidate topology has been selected. The proposed methodology is initially presented in the MV case, considering that at least one port needs isolation.

1) COMPARATIVE EVALUATION OF ISOLATED MV TOPOLOGIES

When isolation is required, partially isolated and isolated configurations must be compared in more detail to decide which solution should be applied. In this section, a qualitative comparison is done using a combination of a component count and a qualitative key feature comparison. The component count serves as a proxy to quantify the size and cost of the devices, whereas, the qualitative key features discussion quantifies the operational characteristics.

The number of components of each topology are derived algebraically in terms of port specifications before being analyzed for the subtransmission network ESOP case detailed in Section II-B. The results can be used as a proxy to quantify the topologies' size and cost.

The number of FB SMs required per MMC arm by the partially isolated topology to integrate a peak line-line AC voltage $\hat{V}_{\mathrm{AC}}$ with an intermediate DC voltage V_{MVDC} is defined by $N_{P.\mathrm{Iso}}$

$$N_{P.\mathrm{Iso}} = 2 * \mathrm{ceil}\left(\frac{\hat{V}_{\mathrm{AC}}}{V_{\mathrm{SM,FB}}}\right) + \mathrm{ceil}\left(\frac{V_{\mathrm{MVDC}}}{V_{\mathrm{SM,FB}}}\right). \quad (4)$$

$V_{\mathrm{SM,FB}}$ is the voltage blocking capability (considering switch utilisation) of the FB switches. Each FB SM will include four two quadrant low-frequency (LF) switches S_{FB} and one SM capacitor C_{FB}. Each MMC leg will require one filter inductor L_f (aggregated representation of upper and lower inductance). In addition, one intermediate DC capacitance C_{MVDC} is required to interface the back-to-back MMCs to the ISOP stage. The number of components required for the back-to-back MMC stage of the partially isolated topology is defined as $N\underline{o}C_{\mathrm{MMC}}$

$$N\underline{o}C_{MMC} = 6[N_{P.Iso} * (4S_{FB} + C_{FB}) + L_f] + C_{MVDC}. \quad (5)$$

$M_{P.\mathrm{Iso}}$ DAB modules are required to interface the intermediate DC bus of the partially isolated topology to the LV DC port

$$M_{P.Iso} = ceil\left(\frac{V_{MVDC}}{V_{SM,AB}}\right). \quad (6)$$

$V_{\mathrm{SM,AB}}$ is the voltage blocking ability of the active bridge switches. Each DAB module includes two active bridge SMs, which are composed of four active bridge switches S_{AB} and one transformer winding $T.W.$ each. Each DAB also includes one transformer core $T.C.$ and one LV output capacitor C_{LVDC}. The number of components that the ISOP DC/DC conversion stage requires is defined as $N\underline{o}C_{\mathrm{ISOP}}$

$$N\underline{o}C_{ISOP} = M_{P.Iso}[2(4S_{AB} + T.W.) + T.C. + C_{LVDC}]. \quad (7)$$

The number of FB SMs required per CHB leg to integrate an AC voltage is defined as N_{Iso}

$$N_{Iso} = \frac{\hat{V}_{AC}}{V_{SM,AB}} \quad (8)$$

The CHB's SMs are directly connected with the active bridge SMs of the MAB modules, whose switches have to be operated at higher frequency and will therefore be rated to a lower voltage blocking ability. Each CHB leg uses a filter inductor, which is assumed to be equal to the aggregated filter inductor for each leg of the MMC. The number of components

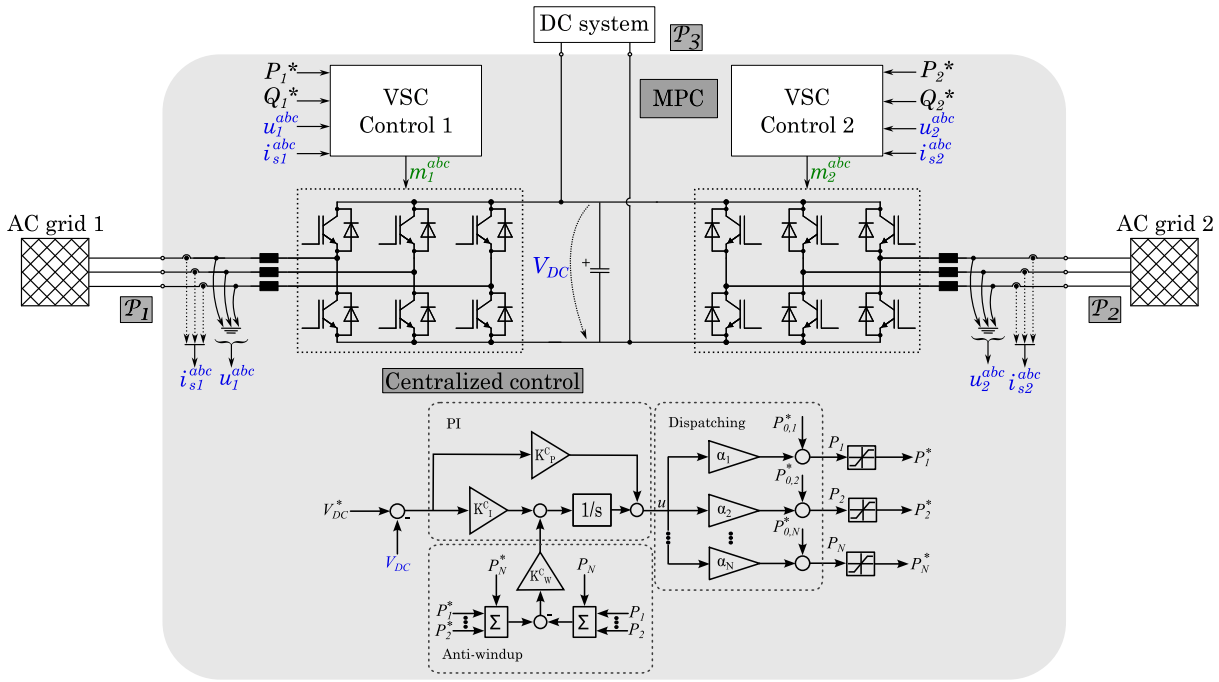

FIGURE 18. Studied non-isolated LV MPC structure.

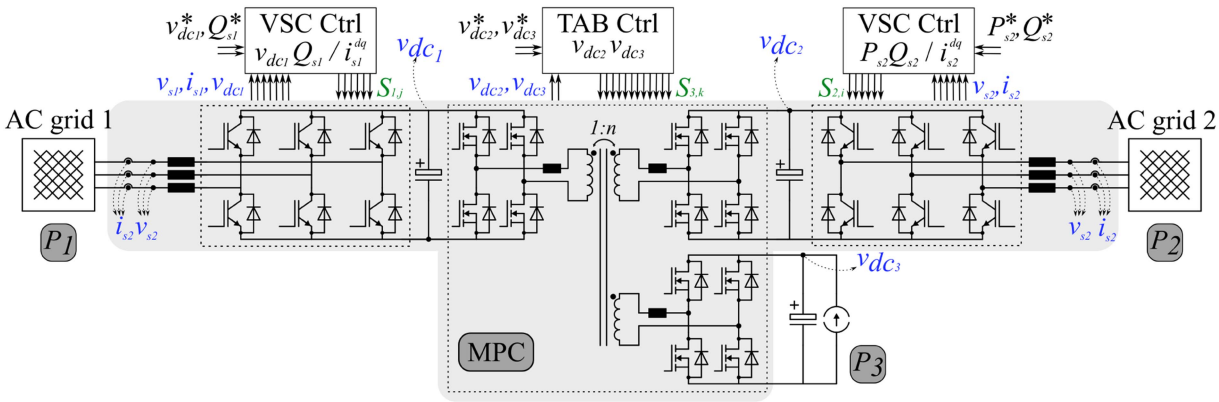

FIGURE 19. Studied isolated LV MPC structure.

required for the two three phase CHBs is defined as $N\underline{o}C_{\text{CHB}}$

$$N\underline{o}C_{CHB} = 6[N_{Iso}(4S_{FB} + C_{FB}) + L_f]. \tag{9}$$

Three sets of MAB modules (M_{Iso}) are required to interface the CHB SMs to each other and the LVDC port. M_{Iso} is defined to ensure that the number of CHB SM pairs (connecting the two AC ports) are grouped with one LV DC assigned active bridge around a transformer core proportionally to the power rating of the AC and DC ports

$$M_{Iso} = ceil\left(\frac{N_{Iso}}{P_{AC}/P_{LVDC}}\right). \tag{10}$$

Each active bridge SM is assumed to be identical to those in the ISOP converter, including four active bridge switches and one transformer winding. The LV DC active bridges also require an output capacitor C_{LVDC}. The number of components required for the multi-MAB isolated DC/DC stage is defined as $N\underline{o}C_{\text{MMAB}}$

$$N\underline{o}C_{\text{MMAB}} = 3\,[2N_{\text{Iso}}(4S_{AB} + T.W.) + M_{\text{Iso}}(T.C. + 4S_{\text{LVDC}} + T.W. + C_{\text{LVDC}})]\,. \tag{11}$$

Fixed switch voltage blocking abilities are defined for LF FB switches and high-frequency active bridge switches, whose values are informed by the optimization in [44], to be used in both topologies. The results highlight the impact of the intermediate DC voltage on the number of components in the partially isolated topology and the impact of the number of multi-active bridge modules on the isolated topology's components. The partially isolated topology is capable of using a high modulation ratio to support a lower intermediate

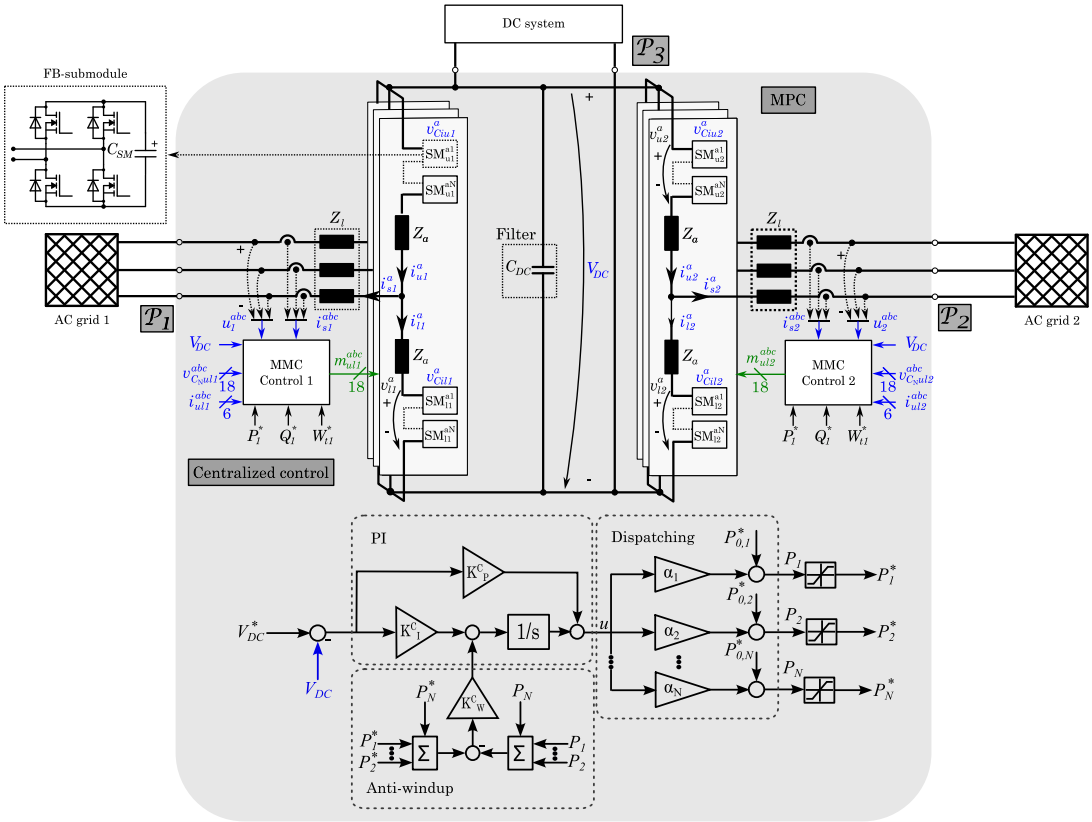

FIGURE 20. Non-isolated MV MPC structure.

DC voltage and therefore lower numbers of MMC and ISOP components, but is associated with an increase in circulating energy and reduced efficiency. The isolated topology can use a lower number of MAB modules to reduce the number of expensive transformers (and LV DC) components, but this increases the topology's operational complexity. All of the partially isolated topology configurations have a lower number of transformer windings and active bridge switches than all of the tested isolated configurations, irrespective of the intermediate DC voltage. A significant modulation ratio tipping point is identified where the partially isolated topology has fewer of all of the component types other than FB switches and capacitors compared to the lowest component (most operationally complex) isolated configuration. The exact modulation ratio m where the tipping point occurs increases with the AC port voltage (from $m = 2.3$ for $V_{\mathrm{AC}} = 5$ kV to $m = 2.5$ for $V_{\mathrm{AC}} = 20$ kV), however, it remains within feasible values considering the literature [44], [52]. Overall, the analysis suggests that the partially isolated topology will require fewer expensive and voluminous components due to its ability to operate with a lower intermediate DC voltage, particularly when the isolated topology's operational complexity is taken into account.

The port fault tolerance of a back-to-back MMC with DC load port was explored in [45] and informs about the partially isolated topology's characteristics. The FB MMC is capable of riding through faults at the AC port without passing critical fault dynamics to the intermediate DC bus, however, the exact behavior depends on the MMC control. The FB MMC is also capable of blocking DC faults, which allows the continued AC operation as STATCOM but without the ability to pass energy between ports. In the case of a LV DC port fault, the ISOP DC/DC converter is expected to be required to be shutdown following fault identification to reduce the transformer voltage to zero and to de-energise the LV side [47].

The performance of the isolated multi-MAB topology during faults is critical. AC port faults impact the fundamental power flow through the linked CHB and active bridge SMs and therefore the transformer. Fault identification and a control mode shift are required to maintain partial operation. LV DC port faults, however, are simply viewed as a DC load changes. Although an intermediate transformer fault is unlikely, it would result in the shutdown of the entire MPC.

The partially isolated topology is resilient to MMC component failure due to the redundancy associated with the FB SMs. In addition, the parallel components of the ISOP stage offer redundancy but this converter is highly sensitive to active bridge failure on the series side. The isolated topology is highly sensitive to CHB component failure due to their direct link with the MAB SMs and therefore on the MPC's power flow and SM balancing. However, the isolated topology possesses many redundant power flow paths when operating below rated conditions.

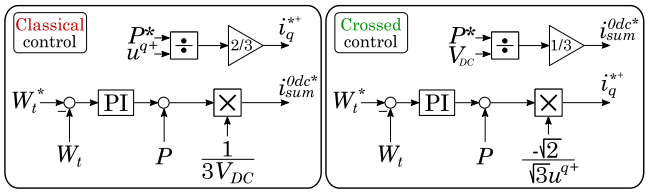

FIGURE 21. Classical and crossed energy based control architectures for an MMC.

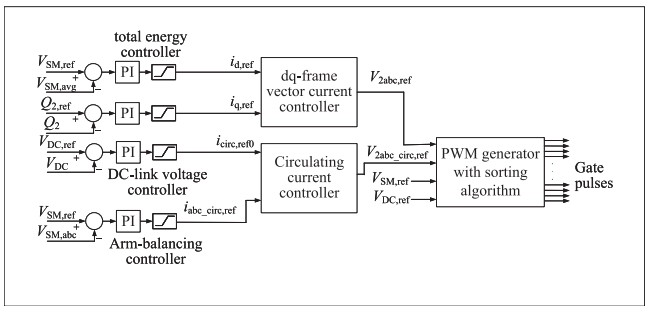

FIGURE 22. Control architecture of the MMC controlling the common DC-link voltage.

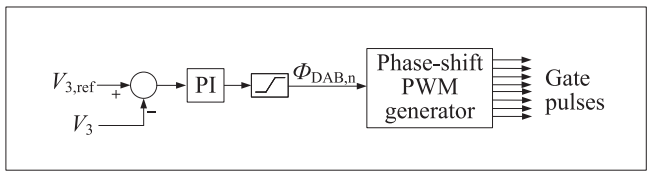

FIGURE 23. Control architecture of the DAB-unit controlling the DC-port voltage.

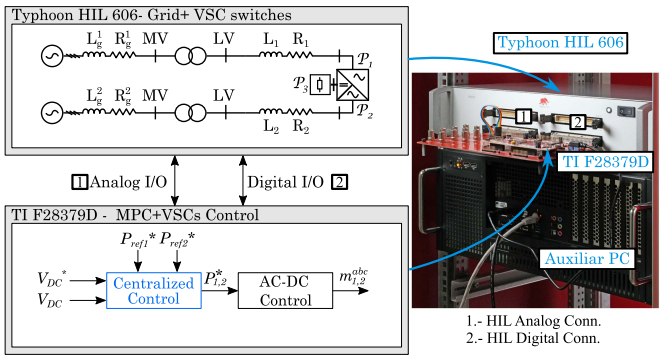

FIGURE 24. CHIL setup for the nonisolated MPC validation.

The partially isolated FB MMC has several control options available to use to suppress the harmonic currents that result from unbalanced operating conditions (e.g., circulating current, energy balancing, and negative sequence [55]). The isolated topology also has the option to use negative sequence controllers to mitigate issues associated with unbalanced conditions, however, the coupling of all of the ports through the transformer may increase difficulty to suppress power oscillations.

The partially isolated topology's FB MMC is highly flexible to support different medium AC voltages by varying either the number of SMs or using a fixed configuration but varying the insertion of SMs. This is particularly relevant in the case of different AC voltage levels, which can be resolved either using asymmetrical back-to-back MMCs or symmetrical MMCs with different modulation ratios. The ISOP converter will need to be reconfigured if the intermediate DC voltage changes. The entire isolated topology is modular but requires similar reconfiguration as the power specification varies.

The partially isolated topology's ports are decoupled due to the FB MMCs and the intermediate DC bus. In addition, the distinct DAB modules of the ISOP converter do not interact with one another on the AC side, meaning that there are no unwanted transformer core couplings and offering relatively simple controllability. In contrast, the isolated topology's MAB modules experience significant core couplings, which increases with the number of active bridges around a single transformer core. This coupling can result in high control complexity.

The qualitative discussion is transformed to a score for each of the key features and is pictured in Fig. 16. The partially isolated topology is only outperformed by the isolated topology in the ability to handle a LV DC port fault.

2) COMPARATIVE EVALUATION OF NON-ISOLATED MV TOPOLOGIES

MMCs, as presented in Section III-B.3, can have HB or FB SM. HB solutions have half the number of components, however, they cannot operate under DC faults, which excludes them from being used with nonisolated MPCs [45]. Consequently, in this case, it is not necessary to perform an extensive comparison, as MPCs based on FB-MMCs are the best possible topology for MV applications where isolation is not required.

3) COMPARATIVE EVALUATION OF LV TOPOLOGIES

This section presents a comparative assessment of the three candidate VSC topologies for LV MPCs.

In this section, only nonisolated and isolated topologies are discussed, since LV partially isolated MPCs solutions have not been found in the literature. For isolated topologies, if a solution with 2 AC ports and at least 1 DC port is required, the most feasible solution is a TAB-based MPC [33]. To determine the topology of the converters connected to the TAB to interconnect it with the AC grids, the comparative evaluation of nonisolated LV topologies presented in this section can be extended.

In the case of nonisolated LV configurations, the component count presented in Section III-C.1 is simplified, as it is clear that 3L-VSCs require three additional bidirectional switches compared to 2L-VSC solutions, and 4w-VSCs require two additional switches, and one additional inductor. Fig. 17 presents a summary of the evaluation, where each topology is assessed across seven key performance metrics: efficiency, structural complexity, control complexity, fault-handling capability, neutral current management, chip area,

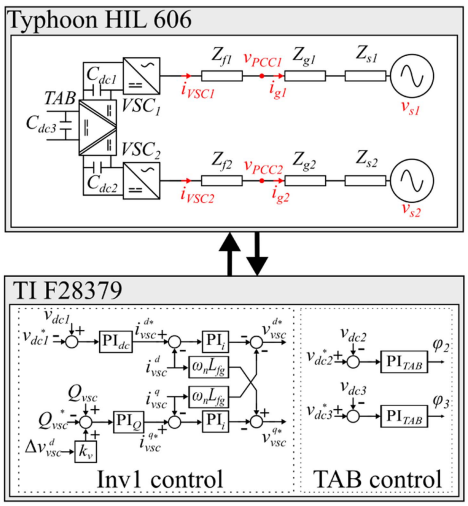

FIGURE 25. CHIL setup for the Isolated MPC validation.

and magnetic component volume. A higher score in each category corresponds to superior performance.

The two-level VSC offers a well-balanced trade-off between implementation simplicity and functional performance. It scores highly in structural and control simplicity due to its minimal switch count and straightforward modulation schemes. Moreover, it features relatively compact chip and magnetic footprints. However, its inability to regulate neutral currents and moderate fault-handling and efficiency ratings limit its suitability for applications requiring high reliability or advanced power quality support.

The three-level VSC, represented by the T-type topology, demonstrates improved efficiency and enhanced harmonic performance, attributed to reduced voltage stress, and finer voltage steps. These characteristics lead to higher scores in efficiency and magnetic volume. However, the increased number of switches and the need for more advanced modulation strategies result in greater structural and control complexity. Furthermore, the lack of neutral current regulation limits its application in unbalanced grid conditions.

The four-wire VSC provides the most robust solution for handling neutral currents and unbalanced loads, significantly outperforming the other topologies in this area. Its additional leg enables zero-sequence current compensation and supports asymmetric load conditions. It also offers enhanced fault-handling capability. These benefits, however, come with increased hardware complexity, higher control burden, and larger passive component requirements, reducing its relative score in implementation compactness.

Based on the presented evaluations, the selection of the appropriate topology depends on the specific requirements of the MPC and SOP application. For balanced grids with stringent cost and size constraints, the 2L-VSC remains a viable choice. The 3L-VSC offers a compelling middle ground between efficiency and performance for moderate complexity scenarios. Meanwhile, the 4W-VSC is the most suitable option for highly dynamic or unbalanced LV networks, where voltage regulation and load symmetry are critical, despite its higher design and implementation complexity. As the Anell LV grid analyzed in this article is balanced and has low power levels, the best option is to use 2L-VSC-based solutions.

TABLE 8. Topology Selection Based on Voltage Level and Isolation Requirements

Voltage Level	Isolation Required	
	Yes	No
LV	TAB+2L-VSC	2L-VSC
MV	DAB+FB-MMC	FB-MMC

D. SUMMARY OF THE SELECTED TOPOLOGIES

In Section III-C, a methodology to qualitatively compare LV and MV topologies has been presented. In this section, the selected topologies for the Anell grid cases presented in Section II-B are summarized. Table 8 shows the obtained results.

When isolation is not required, 2L-VSCs topologies are selected for the LV Anell network, as they are the most compact in terms of simplicity and provided capabilities. For MPCs that require isolation and operate in LV DNs, 2L-VSCs can be interconnected using a TAB converter ensuring isolation in three ports.

In MV levels, when isolation is not required, the only solution that can ensure fault-handling capabilities and acceptable THD levels is a FB-MMC solution. Therefore, a qualitative comparison has not been required. In case that isolation is required, the proposed methodology demonstrated that partially isolated solutions based on FB-MMCs and DABs are the most complete solution.

Therefore, in Section IV, a control strategy suitable for each of the selected topologies is presented, while in Section V, the LV topologies and the partially isolated MV topology are experimentally tested. The control presented for the nonisolated MV topology is not experimentally tested, as it has already been done in [45].

IV. OPERATION AND CONTROL

This section presents the chosen control structures for the topologies selected in Section III. In addition, experimental validation is carried out to demonstrate the operation of the selected topologies in Section III. Color blue As mentioned in Section I, MPCs rely on a power-sharing control layer to ensure proper operation. For nonisolated MPCs, this layer is added in the AC ports control architectures. In contrast, for isolated or partially isolated configurations, DABs, TABs, or MABs converters directly enable coordinated power-sharing across the different ports.

A. CONTROL STRUCTURES FOR MPC TOPOLOGIES

1) NONISOLATED TOPOLOGY FOR LV APPLICATIONS

This section presents the implemented control framework for a nonisolated MPC operating in an LV DN. As this control structure is tested in the Anell LV grid presented in

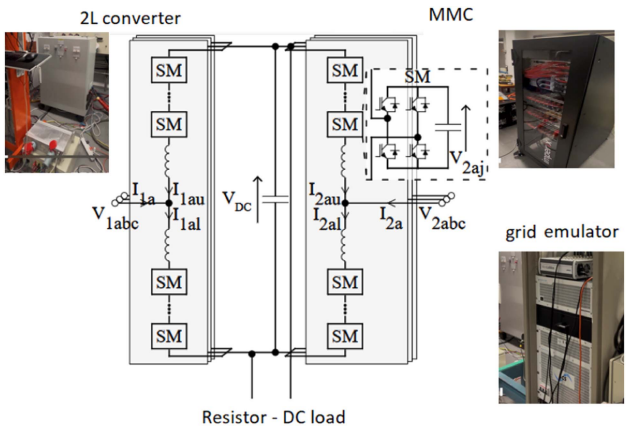

FIGURE 26. Laboratory prototype for a MV 3-port converter consisting of two-level converter at AC-port 1 with an RL-load connected to it, an MMC at AC-port 2 and a grid emulator connected to it, and a DC-load connected at the DC-port.

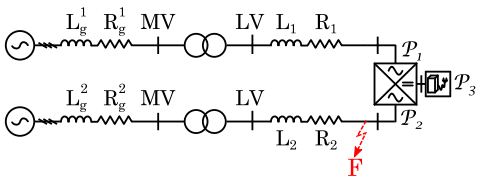

FIGURE 27. Studied system with CHIL setup.

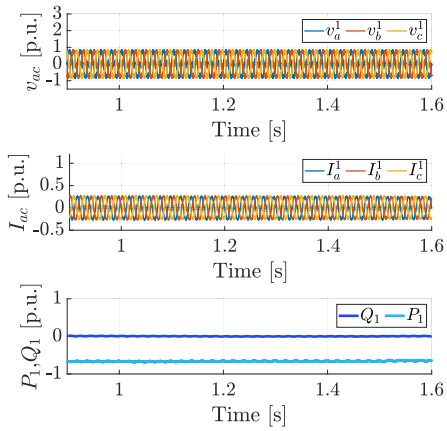

FIGURE 28. AC port 1 results with unbalanced fault.

Section II-B.1, a 2L-VSC topology is used, which, following the methodology presented in Section III-C, is the best possible solution. The aim is to enable reliable power flow management and robust DC voltage regulation across multiple AC and DC ports, especially in scenarios involving balanced and unbalanced AC faults.

Fig. 18 shows an example of the used topology with two AC ports based on 2L-VSCs and one DC port directly connected to the DC bus. As demonstrated in [12], the proposed control can be extended to topologies with N ports, while also adding DC–DC converters. In this article, the studied converter is based on the grid presented in Section II-B.1 and has three ports available to ensure that CHIL tests can be conducted using the available devices. The centralized control architecture presented in [12] and shown in Fig. 18 is used. This centralized approach addresses the limitations of traditional strategies such as droop control and leader-follower control. Droop-based schemes introduce steady-state voltage errors and rely on proportional sharing, whereas leader-follower schemes are vulnerable to faults near the Leader port. In contrast, the proposed control ensures zero steady-state error, fault robustness, and full compatibility with flexible port configurations. In [12], the design of the proposed centralized control is explained in detail.

Each AC and DC port is managed with an individual control loop, forming a cascaded architecture. AC ports are grid-following, syncrhonized via a phase-locked loop (PLL), with outer loops managing active and reactive power, and inner loops controlling current. To enable operation under unbalanced faults, a positive–negative sequence controller is integrated, with sequence decoupling via notch filters [12].

During AC fault conditions, apart from centralized control, several enhancements ensure fault ride-through capability: antiwindup gains, active power management, reactive fault current injection, current references saturation, current prioritization logic, and PLL freezing. In [12], these structures are more detailed.

2) ISOLATED TOPOLOGY FOR LV APPLICATIONS

This section presents an operational description and the control strategy adopted for the selected isolated MPC for LV applications. The topology is based on the TAB, an MPC extension of the popular DAB [14]. The MPC topology uses the TAB to interconnect two AC ports and one DC port. The AC ports are realized by 2-L VSCs, and the DC port is considered a controlled current source. This topology can enhance the interconnection between different sections of the DN and DERs operating at different voltage levels. The topology can be extended to more AC or DC ports by adding active bridges as the MAB used in [9]. Therefore, more AC ports would require adding more inverters.

The control strategy adopted for this topology is based on individual local controllers for each of the subsystems integrated (TAB, VSC1, and VSC2). On one hand, VSC1 controller regulates reactive power injected to AC grid 1, Q_{s1}, and DC-link voltage at port 1, v_{dc_1}, while TAB controller regulates the power flowing from port 1 to ports 2 and 3 by regulating the DC-link voltages at ports 2 and 3, v_{dc_2} and v_{dc_3}. Finally, VSC2 controller regulates active and reactive power flow injected to AC grid 2, P_{s2} and Q_{s2}. The VSC control is performed in the dq synchronous reference frame using a PLL as a synchronization method.

3) NONISOLATED TOPOLOGY FOR MV APPLICATIONS

In this section, a nonisolated MPC for MV DNs is presented. In this case, AC ports are FB-MMCs, as shown in Fig. 20. By using MMCs instead of lower-level topologies, the MPC can

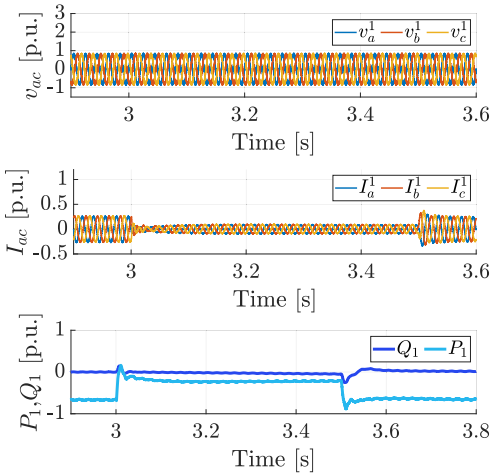

FIGURE 29. AC port 1 results with balanced fault.

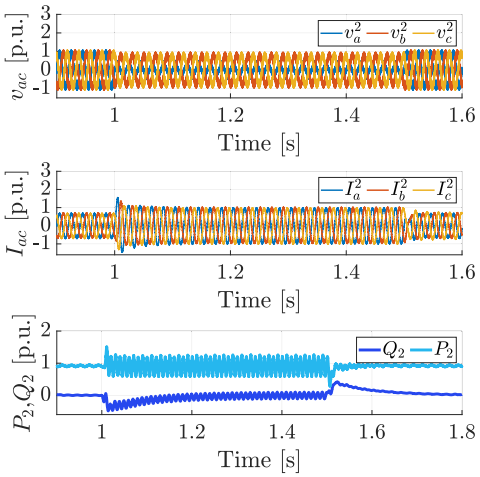

FIGURE 30. AC port 2 results with unbalanced fault.

handle higher AC and DC voltages while avoiding potential undesired harmonic issues.

In the literature, two different control strategies are presented for MMCs: circulating current and energy-based strategies. In this article, an energy-based approach is used, because AC and DC parts of the converter can be managed separately. From the energy-based control architecture, the reference currents related to the active power of the AC and DC grids can be computed using different methods [56]. In the literature, the classical and crossed strategies shown in Fig. 21 are the most commonly employed [56]. It is therefore essential to select an appropriate strategy to achieve a robust MPC operation. In [45], some of the authors of this article compared the classical and crossed control structures using a C-HIL Typhoon setup under AC and DC faults in the nonisolated MPC presented in Fig. 20. The results show that control structures should be chosen depending on whether it is required to prioritise the DC voltage stability or the total energy stability. In addition, all required modifications to ensure FRT operation are documented in [45]. Finally, it should also be noted that

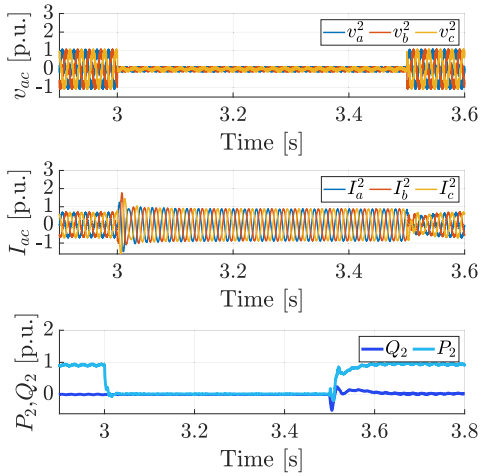

FIGURE 31. AC port 2 results with balanced fault.

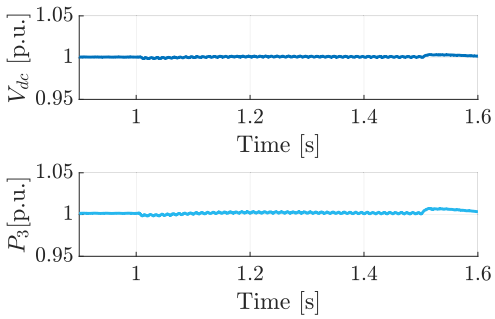

FIGURE 32. DC bus results with unbalanced fault.

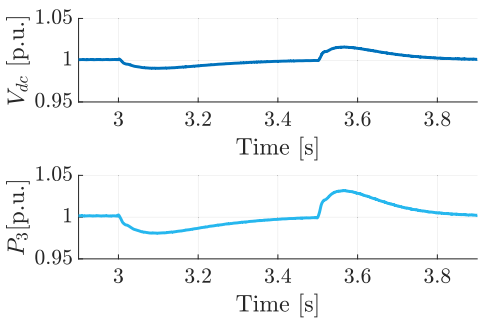

FIGURE 33. DC bus results with balanced fault.

the proposed control architecture can also be used for the nonisolated parts of partially isolated MV MPCs based on MMCs.

4) PARTIALLY-ISOLATED TOPOLOGY FOR MV APPLICATIONS

Based on the evaluation and ranking in Section III-C2, a partially isolated MPC topology is selected as in Fig. 15 for MV grid applications. In the proposed topology, the MMCs can be controlled using the classical approach of grid-following control on the AC-side in a synchronous dq-reference frame, where a PLL is used for synchronization [57]. With reactive-power or AC-voltage control and energy or active-power control generating the reactive- and active-current references,

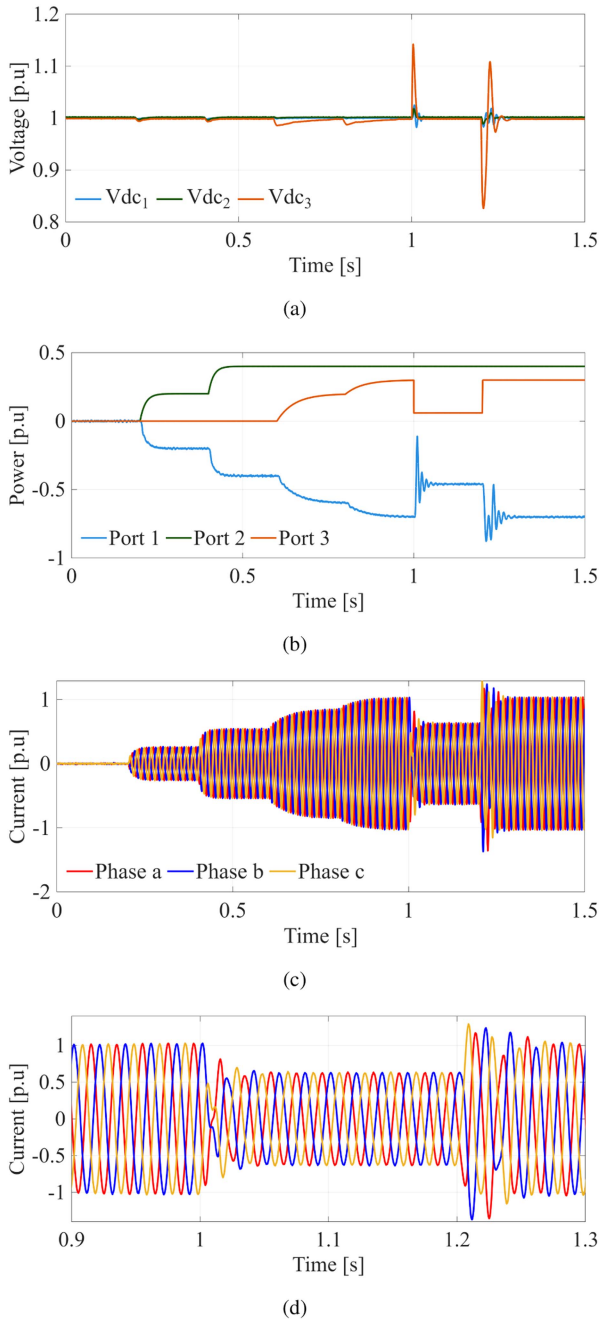

FIGURE 34. TAB-based SOP CHIL results: (a) DC voltage response at ports 1–3, (b) active power response at ports 1–3, (c) AC grid 1 current response, (d) AC grid 1 current response (Zoom).

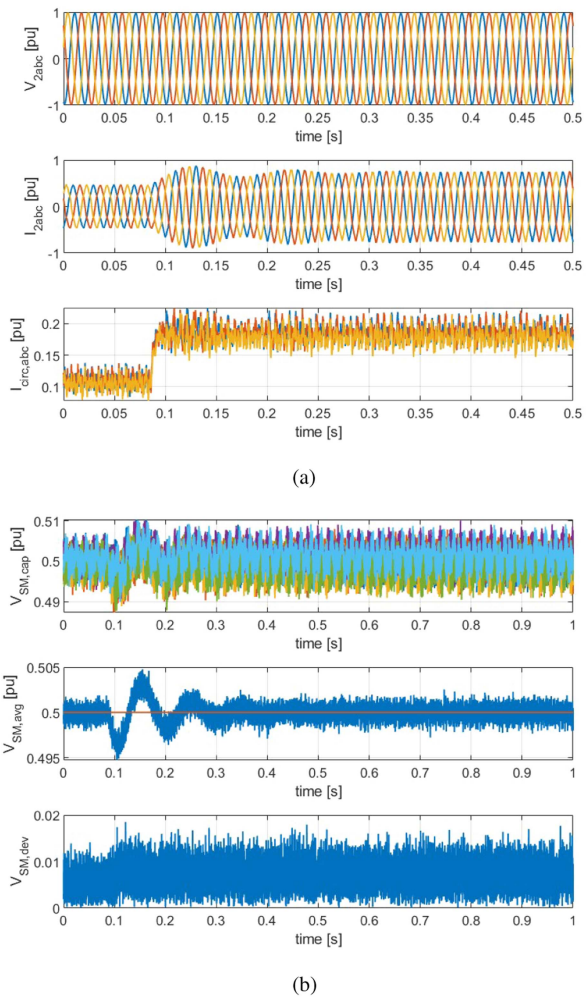

FIGURE 35. Results for a load step-up happening around 0.1 s at the DC-port. (a) Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom). (b) Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage.

respectively, a vector–current controller is employed. In addition, a circulating current controller is used to both attenuate the negative-sequence currents in the MMC phase-legs and to provide a DC-link voltage control as well as energy balancing controller. With the common DC-link voltage controlled from one of the AC-port converters, the other AC-port converter can be operated in active-power control mode with grid-forming control being one option. The DC-port is controlled through the isolation stage to provide a constant voltage, where the phase-shift between the pulsewidth modulation (PWM) carriers for the FB converters on the primary and secondary-side of the transformer are obtained through a PI voltage controller. The control structure of the MMC in DC-link voltage control and one of the DAB-unit in the isolation stage are shown in Figs. 22 and 23.

B. EXPERIMENTAL SETUPS

1) CONTROL HARDWARE-IN-THE-LOOP (CHIL) SETUP

This section presents a CHIL validation of the selected MPCs for LV applications. It should be emphasized that CHIL is not employed here to develop or optimize control strategies, but rather to validate the practical implementation of the proposed design methodology under realistic real-time conditions. In this framework, only the controller hardware is physically implemented, while the converter and grid are emulated in a real-time platform. This approach enables

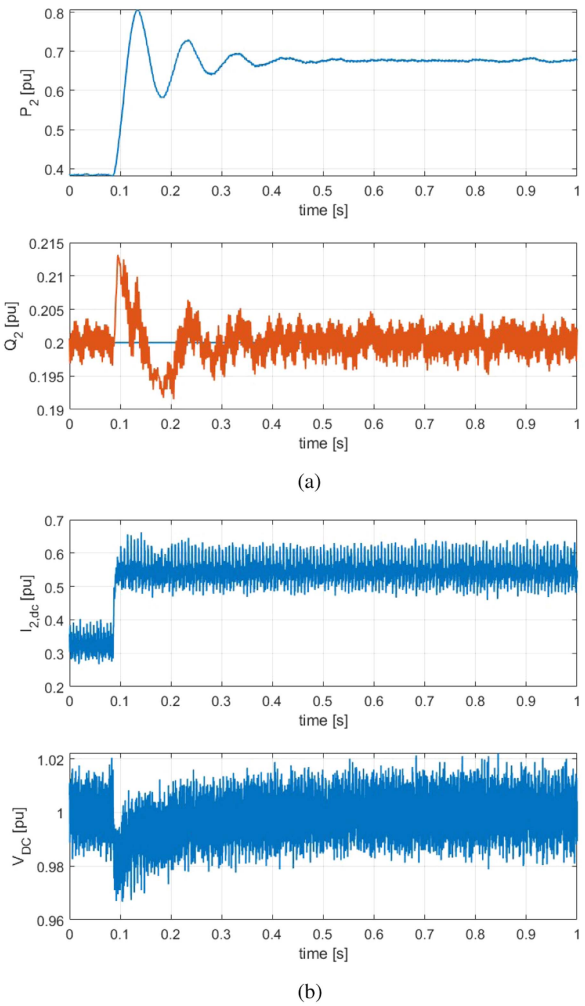

FIGURE 36. Results for a load step-up happening around 0.1 s at the DC-port. (a) Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom). (b) DC current from the MMC to the DC-link (top) and the common DClink voltage (bottom) of the MPC.

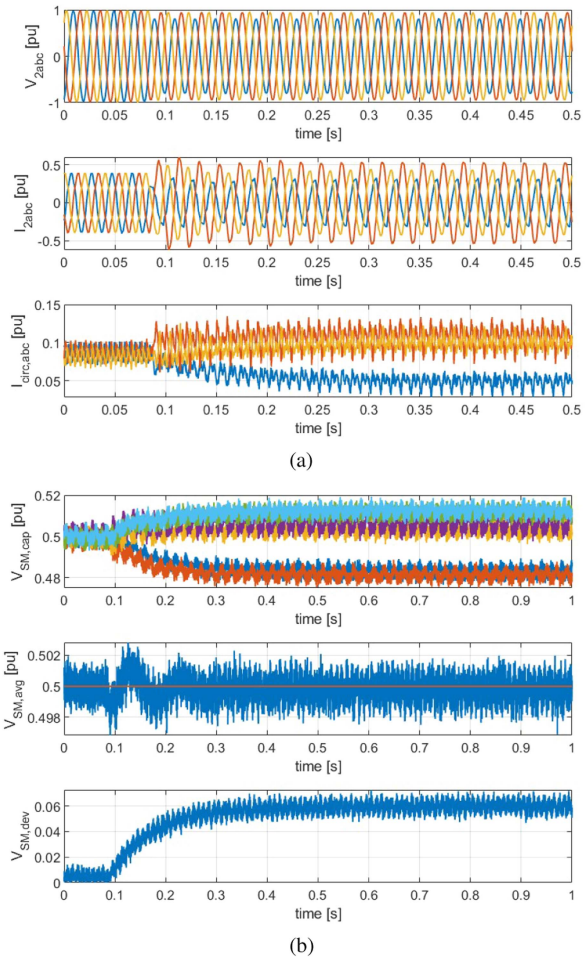

FIGURE 37. Results for an unbalanced voltage dip happening around 0.1 s at AC-port 2 and with no negative-sequence and arm-energy balancing controllers. (a) Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom). (b) Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage.

the assessment of key aspects such as real-time execution, signal interfacing, and control–plant interaction, thereby providing an intermediate validation step between pure simulation and full experimental testing.

To implement the CHIL test, a Texas Instruments F28379D microcontroller is used with the HIL TI LaunchPad Interface. The TI C2000 package from Typhoon is also used for automatically generating control code that can be deployed directly to the microcontroller. Figs. 24 and 25 show the setups used for the nonisolated and isolated LV MPC validation tests, respectively. All the control algorithm is located inside the microcontroller, while the grid and converter switches are maintained within the HIL device.

2) SETUP WITH CONVERTER PROTOTYPES

A laboratory-scale verification for the partially isolated MPC topology, as shown in Fig. 15, was conducted for MV grid applications. The experimental prototype is implemented at reduced voltage levels due to laboratory constraints and hardware availability. The validation therefore focuses on the core control and interaction principles of the MPC. However, owing to the modular nature of the converter structure, these behaviors are preserved when scaling to MV levels, where voltage adaptation is achieved by increasing the number of SM without modifying the control framework. Hence, the laboratory prototype operates at lower voltage levels, with $V_{1\mathrm{LL,rms}} = 50$ V, $V_{2\mathrm{LL,rms}} = 100$ V, and $V_{\mathrm{DC}} = V_3 = 100$ V. Since the entire prototype operates at LV levels, isolation, which is typically used to interface the MV DC-link with the LV load, is not required in this case. Therefore, the DC port in the prototype was implemented with a nonisolated direct connection to the DC-link, with the DC voltage at the interconnection directly controlled to match the required DC-port voltage. The two voltage levels on port 1 and 2 are realized using a two-level converter (using 5 kHz PWM) and

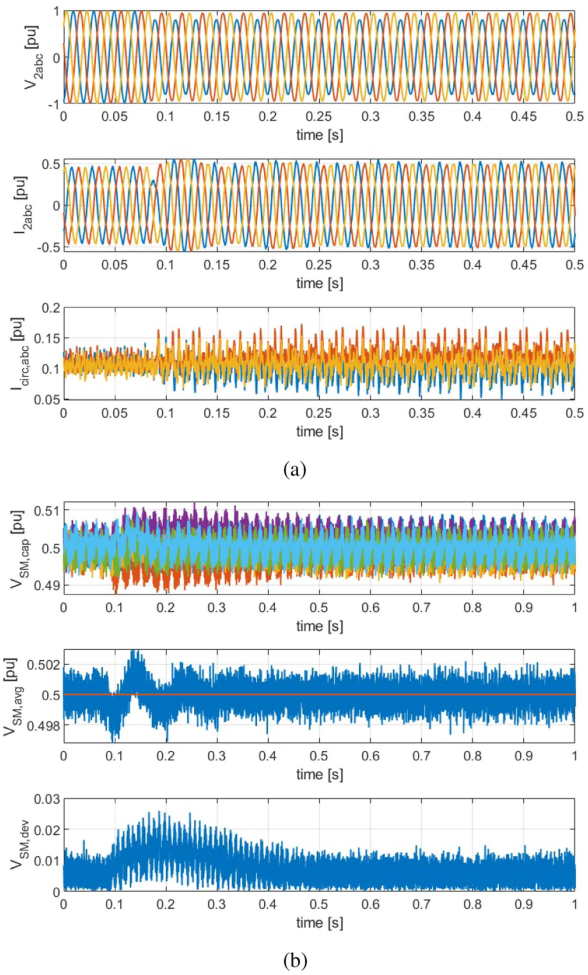

FIGURE 38. Results for an unbalanced voltage dip happening around 0.1 s at AC-port 2 and with negative-sequence and arm-energy balancing controllers. (a) Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom). (b) Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage.

a multilevel converter using FB cells [58], respectively. There are 4 SMs, whose capacitor has capacitance of 0.5 mF and an ESR of 50 mΩ, per arm for each phase and their capacitor voltage is nominally set to 50 V. Each arm of the MMC has a series resistive-inductive filter of 2.3 mH and 60 mΩ. In addition, port 2 is connected to an AC-grid realized through a grid-emulator [59], where as port 1 is connected to a 3-phase passive *RL*-load and the DC-port is connected to a resistive load. The block diagram of the laboratory setup together with the components is shown in Fig. 26.

C. EXPERIMENTAL RESULTS

1) CHIL RESULTS FOR THE NONISOLATED TOPOLOGY IN LV APPLICATIONS

In this section, the LV network presented in Section II-B.1 is validated through the CHIL setup while using the nonisolated MPC based on 2L-VSCs presented in Section IV-A.1. The parameters of the controller and the MPC are defined in Table 9.

TABLE 9. Control Parameters in CHIL Test

Parameter	Value
Switching frequency, F_s	10 kHz
Converter filter impedance, R_l, X_l	0.01 p.u., 0.2 p.u.
DC bus capacitor energy storage time, t_C	40 ms
Inner current control time constant, τ_s	1×10^{-3} s
PLL time constant, τ_{PLL}	0.02 s
PLL damping ratio, ξ_{PLL}	0.707
Reactive power control time constant, τ_Q	0.1 s
Notch filter quality, Q_n	0.5

To evaluate the resiliency of the proposed MPC scheme and its control architecture, a critical operating condition is analyzed. In this scenario, the PV plant is assumed to be unavailable for active power injection, and the DC load is directly connected to the DC bus. Consequently, DC voltage stability must be maintained only through the AC–DC ports. Furthermore, the EV is being charged at its maximum power of 9 kW. Under these conditions, one AC port must inject active power into the DC bus, while the EV charger and the other AC port should absorb it. Fig. 27 shows the system tested with the CHIL setup. It should be noted, that the microcontroller has the centralized control and AC–DC control loops, as shown in Fig. 24.

Both deep balanced and unbalanced AC faults, each lasting 0.5 s, are applied at the port responsible for injecting active power, port 2. This long fault duration is chosen to test a worst-case FRT behavior. The unbalanced fault is a single-phase-to-ground fault (Type B) between phase A and ground, occurring at $t = 1$ s, while the balanced fault begins at $t = 3$ s.

The results obtained from the CHIL simulations are shown in Figs. 28–33. All signals are represented in per-unit (p.u.), with each AC and DC grid normalized based on the nominal values of their respective ports.

Figs. 28 and 29 show that the AC voltages at port 1 remain unaffected by the faults, as these occur in the other AC grid. The converter currents remain constant throughout the simulation, except during the balanced fault. This behavior is due to the active power reference being set to zero during balanced faults in order to prioritize DC voltage stabilization. Since port 1 is not directly affected by the fault, it supplies active power to ensure accurate tracking of the DC voltage reference. The reactive power remains nearly constant throughout the entire test. The oscillations observed in the powers are attributed to signal scaling, offset, and the limited resolution of the analog/digital interfaces. Therefore, this behavior does not indicate an inherent instability of the proposed control strategy.

Figs. 30 and 31 present the results for AC port 2, which is affected by both AC faults. During the unbalanced fault, the phase A voltage decreases, while under the balanced fault, all three phase voltages drop close to zero. In both cases, the current magnitudes increase, operating near the limit of

TABLE 10. TAB-Based SOP System Parameters

Parameter	Value
AC RMS Voltage v_{ac1}, v_{ac2}	230 V, 230 V
AC Frequency f_{ac1}, f_{ac2}	50 Hz, 50 Hz
AC Grid Impedance $R_{grid1,2}, X_{grid1,2}$	0.3 Ω, 0.1 Ω
Inverter Rated Power S_{inv1}, S_{inv2}	50 kVA, 50 kVA
Inverter Inductors L_{inv1}, L_{inv2}	1.2 mH, 1.2 mH
Inverter Resistors R_{inv1}, R_{inv2}	0.1 Ω, 0.1 Ω
DC Voltages $v_{dc1}, v_{dc2}, v_{dc3}$	780 V, 780 V, 400 V
TAB Inductances L_1, L_2, L_3	34.5 μH, 69.9 μH, 69.9 μ H
Port Capacitances C_1, C_2, C_3	3.4 mF, 1.7 mF, N/A
Switching Frequencies (TAB, Inv)	20 kHz, 10 kHz
TAB Port 1 Gains K_{p_1}, K_{i_1}	$0.25\times10^{-3}, 3.7\times10^{-3}$
TAB Port 2 Gains K_{p_2}, K_{i_2}	$0.52\times10^{-3}, 7.8\times10^{-3}$
Inv. 1 Current Gains $K_p^{i_1}, K_i^{i_1}$	9, 1900
Inv. 1 DC Voltage Gains $K_p^{vdc_1}, K_i^{vdc_1}$	1, 372
Inv. 1 Q Control $K_p^{Q_1}, K_i^{Q_1}$	$20\times10^{-6}, 0.12$
Inv. 2 Current Gains $K_p^{i_2}, K_i^{i_2}$	5, 970
Inv. 2 P&Q Gains $K_p^{P_2}, K_i^{P_2}$	$20\times10^{-6}, 0.06$
PLL Gains (Inv. 1, 2) K_p^{PLL}, K_i^{PLL}	0.1, 1

1.05 times the nominal current. In addition, since the negative *qd* current references are set to zero, 100 Hz oscillations appear in both active and reactive power during the unbalanced fault. These oscillations arise from the interaction between the positive-sequence current and the negative-sequence voltage component, which introduces a second-harmonic term in the instantaneous power. Nevertheless, the power values still follow their respective references. During the balanced fault, both active and reactive powers fall to zero due to the AC voltage close to 0.

Figs. 32 and 33 display the DC bus signals during both fault conditions. DC voltage remains stable throughout the tests and successfully tracks its reference after each disturbance. Since the EV charger is considered a load directly connected to the DC bus, its power closely follows the DC voltage. Therefore, it can be concluded that the proposed controller operates consistently in any fault condition.

2) CHIL RESULTS FOR THE ISOLATED TOPOLOGY IN LV APPLICATION

This section presents the CHIL simulation results of a TAB-based SOP. The model derivation, converter operation, and control are presented in detail in [60]. The simulations are based on the converter and controller parameters presented in Table 10.

For the validation of the controller, power disturbances are applied at ports 2 and 3. Also, a voltage disturbance is applied at port 1 v_{dc_1} as follows.

1) $t = 0.2$ s, port 2 active power increases from 0 to 20 kW.
2) $t = 0.4$ s, port 2 active power increases from 20 to 40 kW.
3) $t = 0.6$ s, port 3 active power increases from 0 to 20 kW.
4) $t = 0.8$ s, port 3 active power increases from 20 to 30 kW.
5) $t = 1$ s, port 3 load is partially and suddenly lost (final active power is 6 kW).
6) $t = 1.2$ s, port 3 load is recovered and reaches 30 kW again.

Fig. 34 shows the behavior of the TAB-based SOP under several changes in the operating point. Fig. 34(a) shows that voltages at each port are regulated successfully. The port 1 voltage regulation is faster than ports 2 and 3, which improves the DC voltage response at ports 2 and 3. When $t \sim 1$ s, the AC current at port 1 reaches its nominal values [see Fig. 34(d)], and at $t = 1$ s, the port 3 load is partially lost, decreasing by 26 kW [see Fig. 34(b)]. Fig. 34(a) shows a large voltage peak in v_{dc_3}, while ports 1 and 2 are less affected by this change. After reaching steady state, at $t = 1.2$ s, the load at port 3 is recovered, creating a big voltage dip in v_{dc_3}, following an overshoot and reaching steady state after 0.2 s. This overshoot is also observed in the active power and AC current at port 1, which is supplying the power demanded by ports 2 and 3. It is clear that the dynamic response remains as expected, even when the SOP is subject to faults in one of its ports, like the loss of port 3 simulated at $t = 6$ s. Finally, it is important to note that port 3 is more susceptible to power disturbances due to its lower nominal voltage.

3) PROTOTYPE RESULTS FOR THE PARTIALLY-ISOLATED TOPOLOGY IN MV APPLICATIONS

With the setup as in Fig. 26, the three-phase MMC is controlled using the classical approach of grid-following control on the AC-side. A reactive-power and energy controllers generate the reactive- and active-current references, respectively, for the implemented vector–current controller. In addition, a circulating current controller is used to both attenuate the negative-sequence current in the MMC phae-legs and to provide a DC-link voltage control as well as an energy control. With the number of SMs in the arm being low at 4, PWM with a carrier frequency of 20 kHz is used to bypass or insert the FB SM, applying positive or negative capacitor voltage to generate the converter voltage output. With the DC side of the converter controlled from the MMC converter side, the AC side of the 2L-VSC operates with the nominal voltage in grid-forming control mode to supply a passive load. Similarly, a resistive load is connected directly to the DC-link, representing a constant power DC load. For the tests, the gains of the controllers in Fig. 22 are adjusted to achieve selected bandwidth requirements for the different control loops as indicated in Table 11. Note that the control bandwidths are selected based on a cascaded control structure with clear time-scale separation. The inner current control loops (AC-side and circulating current) are designed with high bandwidth ($\sim$ 500 Hz) to ensure fast dynamic response. The negative-sequence controller is assigned a lower bandwidth to minimize interaction with the main control loops. The outer control loops, including DC-link voltage and reactive power control, are chosen with slower dynamics ($\sim$ 10 Hz) following practical design recommendations. To maintain proper hierarchy, the

TABLE 11. Control Parameters of the MMC in the Prototype

Closed-loop bandwidth	Value, rad/s
Positive-sequence current control	1000π
Negative-sequence current control	200π
Circulating-current control	1000π
PLL	10π
Reactive-power control	20π
Total-energy control	10π
DC-link voltage control	20π
Arm-balancing control	10π

total energy and arm-balancing controllers are set with lower bandwidth ($\sim$ 5 Hz) to avoid interaction with the DC-link control. In addition, the PLL employs a low bandwidth ($\sim$5 Hz) to ensure stable and robust synchronization under grid disturbances.

First, a load step in the active power at the DC-port is applied to test the operation of the converter and results are presented in Figs. 35 and 36 based on base values of 100 V (DC or AC-RMS) and 1000 VA. As the results indicate, all quantities are controlled within allowed limits, with the active power output at the AC port-2, as well as the SM capacitor voltages, being regulated well. A change in active power also affects the DC-link, but it can track its reference value. The slow dynamics associated with the active-power output at AC-port 2 are due to the high capacitance in the SM. The experimental results exhibit high-frequency noise, particularly visible in the circulating currents, which is mainly caused by nonideal effects inherent to the hardware implementation, such as measurement noise. These disturbances are expected in practical setups and do not reflect the fundamental behavior of the proposed control strategy. The results show that the power flow is controlled at all ports, with the capacitor voltage of all SM balanced and within limits, confirming the successful operation of the converter during active-power changes at the ports.

Next, the performance of the converter in case of unbalanced grid operation is tested. In this case, a proper controller of the MMC, including a negative sequence control as well as an arm energy balance controller, is necessary to manage the power exchange at the AC ports properly and maintain balanced capacitor voltages. With only the positive sequence control and no arm energy balance control, the impact of unbalanced grid affects the proper operation of the converter through oscillation of the power exchange as well as oscillations and unbalance in the SM capacitor voltages (due to unbalanced current exchanges in the AC- and DC-side of the MMC) as shown in Fig. 37 when AC-port 2 is connected to an unbalanced grid.

Finally, with a negative-sequence and arm-energy balancing controller implemented, an unbalanced grid voltage dip is applied at AC-port 2. Results in Fig. 38 shows that the converter operates well in this abnormal operating conditions verifying the effectiveness of the control strategy.

V. CONCLUSION

This article presents the various design phases of MPCs, which are proven to be a general power electronics concept that can enhance operation in LV and MV DNs. MPCs are presented as an alternative to reduce traditional network reinforcements or replace conventional network equipment by improving network flexibility.

MPCs must be installed in locations and scenarios where they can solve specific technical issues and result in a cost-effective solution. In that regard, two realistic use cases have been proposed based on challenges identified in DSO networks, in particular considering the example of Anell. LV use case is based on the interconnection of two LV feeders operating at different voltage levels and with PV and EV integration potential, while MV use case is based on the interconnection of two MV feeders at same voltage level but with significant differences in voltage drop. An optimization-based sizing approach is applied to determine the power ratings of each MPC terminal, considering LV and MV network configurations and also PV generation, loads, and electric vehicle (EV) charging profiles. As a result, for LV applications the collocation of different components showed advantages to reduce the power rating of the converters. Also, for MV applications, the MPC was validated as a solution to balance voltage between parallel feeders.

Power electronics topologies, based on both non-isolated and isolated options, were presented, depending on LV and MV applications. Also, a qualitative evaluation of LV and MV applications based on several indicators was presented to compare or select the most convenient topologies. It was clear that component scalability represents an essential feature to consider. Also, when interconnecting LV and MV ports, voltage gain, galvanic isolation and fault tolerance become important characteristics. When only interconnecting MV ports, high scalability, controllability, and potentially fault-tolerant response can be achieved with non-isolated options. If interconnection of LV and MV ports is required, then an effective voltage gain can be mainly achieved with isolated options. A partially-isolated MPC presents a mixture of the benefits from isolated and non-isolated topologies, especially if multiple MV and LV ports are expected.

Control structures were presented for some of the previously analysed topologies. Non-isolated MPCs prioritise the voltage regulation of the common DC bus. In general, they can use a similar control structure for LV and MV applications, but with more complexity for MV applications due to modular multilevel configurations. Isolated topologies require specific control structures for the triple or MAB stages. Partially-isolated topologies combine the control structures from isolated and non-isolated options. Final implementation in CHIL and converter prototypes demonstrates that the selected topologies are operating as expected in a laboratory environment.

Future work could improve the sizing methodology to include a techno-economic analysis, defining precise values for

CAPEX, maintenance cost, lifecycle cost and converter degradation according to the specific topology chosen.

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