

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Dynamic Thermal Response of GaN MMICs

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ABSTRACT

Gallium nitride (GaN) monolithic microwave integrated circuits (MMICs) are a key technology for wireless infrastructure, where channel temperature constrains both output power and lifetime. Predicting this temperature is difficult for two reasons. First, it depends on every layer from the channel to the ambient, many of which are uncertain and require in situ characterisation. Second, the dissipated power varies in time during operation. As heat diffuses, each level of integration contributes on a largely distinct time scale, from nanoseconds near the channel to seconds and longer at the system level. Consequently, the dynamic thermal response both complicates the prediction and enables a solution to resolve individual contributions.

This thesis aims to improve channel-temperature prediction in packaged GaN MMICs by using the dynamic thermal response to separate the relevant thermal contributions. Following the heat path, it combines transient measurements on dedicated test structures with calibrated finite-element simulations. At the integrated-circuit level, the study investigates the dynamics of thermal coupling between heat sources and the role of the through-substrate via in layout consideration. At the package level, a thermal test chip is developed to match the GaN MMIC in material system and layout-level heat-dissipation, enabling in situ characterisation without optical access. At the system level, an experimental setup for additively manufactured, liquid-cooled baseplates is implemented. Collectively, these approaches demonstrate how the device, integrated circuit, and package levels shape the dynamic thermal response and provide methods to separate these contributions in situ.

Keywords: GaN HEMT, MMIC, dynamic thermal response, advanced packaging, electro-thermal device modelling, thermal characterisation, thermal coupling, thermal management, thermal test chip, thermal transient measurement

List of Publications

Appended publications

This thesis is based on the content in the following papers:

- [A] **T. Kristensen**, T. M. J. Nilsson, A. Divinyi, J. Bremer, and M. Thorsell, "Numerical Modeling of Dynamic Thermal Coupling in GaN HEMTs Calibrated by Transient Measurements," *IEEE Transactions on Electron Devices*, vol. 71, no. 12, pp. 7343-7349, Dec. 2024.
- [B] **T. Kristensen**, T. M. J. Nilsson, A. Divinyi, J. Bremer, and M. Thorsell, "Dynamic Thermal Coupling in GaN MMIC Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 1, pp. 38-44, Jan. 2025.
- [C] **T. Kristensen**, T. M. J. Nilsson, D. Kuylenskierna, and M. Thorsell, "Impact of Through-Substrate Vias on the Thermal Resistance of GaN-on-SiC MMICs," submitted to *IEEE Microwave and Wireless Technology Letters*, Sep. 2026.
- [D] **T. Kristensen**, M. Thorsell, R. Lindman, T. M. J. Nilsson, and D. Kuylenskierna, "Thermal Test Chip for In-situ Characterization of GaN-on-SiC MMICs," to be submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Sep. 2026.

Other publications

The following are not included due to an overlap in the content or content that goes beyond the scope of this thesis:

- [a] **T. Kristensen**, A. Divinyi, J. Bremer, T. M. J. Nilsson, and M. Thorsell, "Thermal Transient Measurements of GaN HEMT Structures by Electrical Measurements," *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, Berlin, Germany, 2023.
- [b] A. Divinyi, T. M. J. Nilsson, N. Rorsman, **T. Kristensen**, H. Hultin, S. E. Gunnarsson, and M. Thorsell, "On-Chip Sensors for Temperature Monitoring of Packaged GaN MMICs," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 14, no. 5, pp. 891-896, May 2024.
- [c] **T. Kristensen**, T. M. J. Nilsson, A. Divinyi, J. Bremer, and M. Thorsell, "Characterization and Modeling of Dynamic Thermal Coupling in GaN MMIC Power Amplifiers," *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*, Washington, DC, USA, 2024.
- [d] D. Q. Tran, **T. Kristensen**, R. Soman, M. Malakoutian, P. P. Paskov, N. Rorsman, M. Thorsell, S. Chowdhury, and V. Darakchieva, "Resolving lateral heat transport in GaN-on-SiC HEMT structures via transient thermometry", accepted for publication in *Advanced Materials Technologies*, Sep. 2026.

Summary of appended papers

This section provides a summary of the publications included in the thesis and the contribution of the author.

Paper A

Summary: The dynamic response of thermal coupling is studied in isolation using a dedicated test structure. An FEM model of the effect is developed, including a sensitivity analysis of the model parameters and a calibration method. An example illustrates how the results can be used to optimise a layout.

Contribution: Development of the measurement setup and the FEM model. Performed the measurements and simulations, analysed the results, and wrote the manuscript.

Paper B

Summary: The effect of thermal coupling on a GaN MMIC is investigated using transient measurements, FEM simulations, and an equivalent linear thermal network. The results provide tools and guidelines for considering thermal coupling in MMIC design.

Contribution: Contributed to the design of the test structure. Performed the measurements and simulations, extracted the equivalent thermal network, analysed the results, and wrote the manuscript.

Paper C

Summary: The influence of the through-substrate via on the heat transfer in GaN-on-SiC technology is investigated. Transient measurements on a dedicated test structure are presented, and the implications for the layout of a GaN HEMT are discussed using FEM simulations.

Contribution: Initiated the study and designed the test structure. Performed the measurements and simulations, analysed the results, and wrote the manuscript.

Paper D

Summary: The design and experimental evaluation of a thermal test chip for in situ characterisation of the integration of GaN MMICs are presented. The results show how the integration affects the transient response and how this effect can be modelled in FEM simulations.

Contribution: Initiated the study, designed the thermal test chip and the experimental setup. Performed the measurements and simulations, analysed the results, and wrote the manuscript.

Declaration on the use of generative AI

Generative artificial intelligence tools have been used in the preparation of this thesis. Grammarly has been used to correct grammar, and to improve language and structure. Claude by Anthropic has been used similarly, including to review sections of the text and assist with writing code for plotting data presented in the thesis. The technical content, analysis, and conclusions are the author's own.

Notations and Abbreviations

Notations

A	Scaling factor of the Arrhenius equation
$a(T)$	Temperature-dependent scaling factor of the drain current
C_p	Specific heat capacity
$\mathbf{E}$	Electric field
E_A	Activation energy
f_T	Current gain cut-off frequency
h	Heat transfer coefficient
H_1-H_5	Heat sources of the thermal test chip
i, j	Indices of heat sources in the thermal coupling matrix
I_{DS}	Drain–source current
I_{ds0}	Isothermal drain–source current
$\mathbf{J}$	Current density
k_B	Boltzmann constant
L_{GaN}	GaN layer thickness
L_S	Source inductance
L_{SiC}	SiC substrate thickness
n	Exponent of the temperature dependence, $\kappa \propto T^{-n}$
P_j	Power dissipated in heat source j
q''	Heat flux
Q	Volumetric heat generation rate
$\mathbf{r}$	Position vector
R_{DA}	Thermal resistance of the die-attach interface
R_{i1}	Interface resistance towards the MMIC metallization
R_{i2}	Interface resistance towards the heat spreader
R_{th}	Thermal resistance
S_1-S_6	Temperature sensors of the thermal test chip
S_C	Separation between the hot spots of two channels
t	Time
$t_{failure}$	Time to failure
T	Temperature
T_0	Base temperature (backside of package)
T_A	Ambient reference temperature

T_i	Temperature of heat source i
V_{DS}	Drain–source voltage
V_{GS}	Gate–source voltage
Z_{ij}	Element of the thermal coupling matrix
Z_{th}	Dynamic thermal response (thermal impedance)
α	Thermal diffusivity
ΔT	Temperature rise
ΔT_{∞}	Steady-state temperature rise
κ	Thermal conductivity
κ_{DA}	Thermal conductivity of the die-attach material
ρ	Mass density
ω	Angular frequency

Abbreviations

2DEG	Two-dimensional electron gas
AESA	Active electronically scanned array
AlGaIn	Aluminium gallium nitride
AM	Additive manufacturing
BLT	Bond line thickness
CMOS	Complementary metal–oxide–semiconductor
CPU	Central processing unit
CTE	Coefficient of thermal expansion
DC	Direct current
DSSV	Double-sided source via
DUT	Device under test
FEM	Finite element method
FOWLP	Fan-out wafer-level package
FP	Field plate
GaAs	Gallium arsenide
GaN	Gallium nitride
GRT	Gate-resistance thermometry
HEMT	High-electron-mobility transistor
IC	Integrated circuit
IR	Infrared
ISV	Internal source via
IV	Current–voltage
MC	Monte Carlo
MFP	Mean free path
MMIC	Monolithic microwave integrated circuit
MTTF	Mean time to failure
OSV	Outside source via

PA	Power amplifier
PBF-LB	Powder bed fusion with a laser beam
PCB	Printed circuit board
QFN	Quad-flat no-leads
RDL	Redistribution layer
RF	Radio frequency
RTD	Resistive temperature detector
SFP	Source field plate
Si	Silicon
SiC	Silicon carbide
SiN	Silicon nitride
SiP	System-in-package
SThM	Scanning thermal microscope
SWaP	Size, weight, and power consumption
TBR	Thermal boundary resistance
TIM	Thermal interface material
TLM	Transfer length method
TR	Thermorefectance
TRM	Transmit/receive module
TSEP	Temperature-sensitive electrical parameter
TSV	Through-substrate via
TTC	Thermal test chip

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Chapter 1

Introduction

Wireless communication and remote sensing are critical to modern infrastructure. The most prominent example is mobile communication networks, which connect people and services and are integral to everyday life. The number of users and the data traffic are rapidly increasing in these networks [1]. Satellite communication networks have also developed rapidly, extending connectivity to remote areas and providing a resilient alternative to terrestrial networks. In an emergency, mobile and satellite communications are critical for alerting and coordination. Radar systems are also an important part of wireless infrastructure, integrated into air traffic control, maritime operations, environmental monitoring, and defence. These systems have different purposes but share the requirements for high reliability, large-scale operation, and long range, under strict constraints on size, weight, and power consumption (SWaP). The demands, such as higher data rates and longer range, increase with each generation, requiring innovations in the microwave electronic front-end.

The requirements of the next generation of wireless infrastructure cannot be met with a single semiconductor technology. Higher data rates require digital signal processing, which is most efficiently implemented in silicon CMOS processes. However, for long-range applications, the use of compound semiconductors, such as gallium arsenide (GaAs) and gallium nitride (GaN), is attractive for higher output powers. Therefore, heterogeneous integration of various semiconductor processes into a system-in-package (SiP) is of interest for future systems. This is apparent for active electronically scanned arrays (AESA), used in radar, satellite, and mobile networks. Here, many transmit/receive modules (TRMs) must be integrated in proximity to an antenna array, with half-wavelength spacing between them. As carrier frequencies increase, this is impractical for discrete components and requires SiP solutions.

The transmit power driving the antenna in the TRM is set by the power amplifier (PA). Transmit power sets the system's range, along with the antenna gain and the receiver's noise floor. GaN monolithic microwave integrated circuits (MMICs) have become a leading technology for such PAs, as they reliably operate at the highest power density at microwave frequencies. The wider bandgap of GaN compared to silicon and GaAs allows for a higher breakdown field and operation at elevated temperatures, and the GaN high-electron-mobility transistor (HEMT) provides high sheet carrier density, electron mobility and saturation velocity, resulting in a competitive current density. Combined, this enables higher output power per unit gate width, so that a given output power can be achieved with a smaller device.

The high output power density comes at the cost of managing a high density of dissipated heat. Heat generation is centred in a region approximately 400 nm wide at the drain-side edge

of the gate in the saturation regime, where the electric field peaks [2]. At the typical 5 W/mm output power for commercial technologies, the dissipated power corresponds to a local heat flux above 1 MW/cm². The reliability of the GaN HEMT is largely limited by thermally activated degradation, such as interdiffusion at the gate metal–semiconductor interface, which follows an Arrhenius dependence on temperature. This gives an exponential relationship between the increase in channel temperature and the reduction in mean time to failure (MTTF). The required lifetime sets a maximum channel temperature, and, consequently, the heat transfer from the hot spot constrains the maximum output power that can be sustained. This is quantified by the thermal resistance (R_{th}), defined as the ratio of channel temperature increase above a reference temperature to the dissipated power. The Defense Advanced Research Projects Agency (DARPA) has argued that an eight-fold reduction in R_{th} is needed to reach the intrinsic limit of GaN HEMTs [3]. A considerable effort is directed at this, for example through integration of diamond heat spreaders [4], [5] and micro-channel cooling [6], [7]. This thesis focuses on predicting the temperature of a given assembly, where several effects must be considered.

A central technique for power handling in MMICs is to distribute the power across separate HEMT channels operating in parallel and combine them at the output. This is done both at the device level, in multi-channel transistors, and at the circuit level, where several such transistors are combined. The heat flux generated in a single channel will increase the temperature in neighbouring channels. This thermal interaction is denoted as thermal coupling in this thesis. The thermal coupling between two heat sources decreases with increasing separation, so the channel temperature and its distribution across the MMIC depend on the layout. Consequently, the MMIC layout must be co-designed with thermal performance in mind, alongside electrical performance and manufacturability.

The channel temperature in the GaN HEMT is determined by the heat transfer through each material and interface along the paths from the GaN HEMT channel to the ambient environment. Therefore, R_{th} is determined not only by semiconductor technology, but also by packaging and system integration. Several of the layers in this path, however, are not known beforehand. In the epitaxial layers in the GaN HEMT, the layer thickness is close to the mean free path of phonons in the material, which makes the effective thermal conductivity thickness dependent [8], [9]. As a consequence, very thin layers effectively function like thermal barriers, whose contribution must be determined in situ [10], [11]. Further along the path, heat transfer through the die attach and thermal interface materials depends on the assembly and must also be characterised in situ. The channel temperature of a packaged MMIC is therefore difficult to predict, while knowing it is critical to ensure the safe operating temperature is not exceeded and to design the system.

In a SiP, the path to the ambient is more complex and uncertain than for a conventional package, as shown in Fig. 1.1. These packages help meet SWaP requirements but add heat-transfer paths, material interfaces, and materials. The heat from the MMIC is also distributed across a system with other heat sources, which change the boundary condition seen by the MMIC. As a result, in situ thermal characterisation becomes both essential and more challenging. For instance, flip-chip-mounted MMICs with backside cooling cannot be assessed using optical measurement techniques, necessitating alternative approaches. The characterisation therefore has to be performed in situ in the assembled SiP, without optical

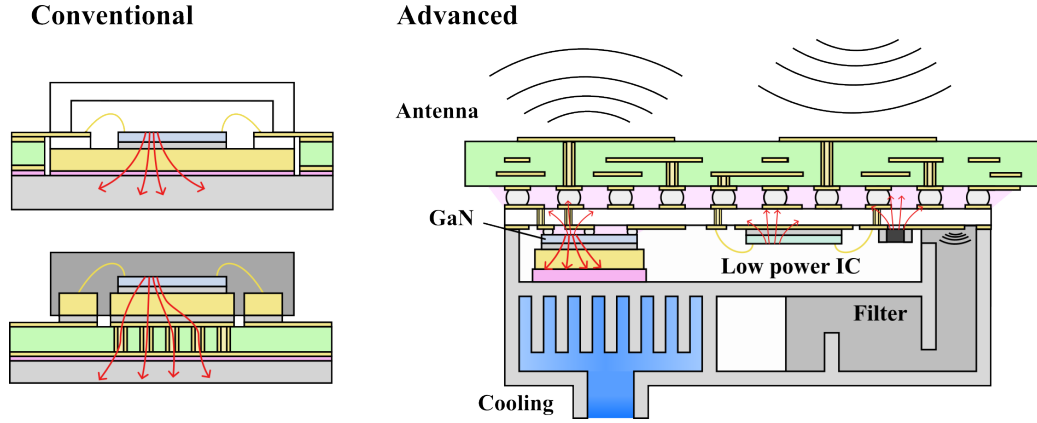


Figure 1.1: Heat paths in conventional packages (left) and in an advanced package (right). In the advanced package, the heat from the GaN MMIC leaves through several paths and interfaces, and the die cannot be accessed. The advanced package illustrates how additive manufacturing can be used to integrate cooling and filters into a package.

access, and it needs to characterise the contribution of the layers along the path.

The power dissipated in a PA varies over time during large-signal operation. Pulsed operation is used to limit average dissipation during inactive periods, while modulated signals introduce envelope variations that alter both power dissipation and temperature. These dynamics have two principal implications. First, the electrical performance of GaN HEMTs is temperature-dependent, and electro-thermal interactions transform the thermal response into a source of distortion and memory effects that affect the linearity of the PA [12], [13], [14]. Second, because the MTTF decreases exponentially with temperature, accurate lifetime prediction requires knowledge of the actual temperature reached for the specific operating waveform. Assuming continuous-wave operation is overly conservative, while relying on the average temperature is too liberal because it neglects critical temperature peaks.

The dynamic response arises because heat requires time to propagate through the system. Rapid variations affect only the material near the source, whereas slower variations allow heat to spread through the MMIC, package, and ultimately into the ambient environment. Heat spreads diffusively, so at time t after a change, the response travels approximately a diffusion length, $\sqrt{\alpha t}$, from the source, where α is the thermal diffusivity of the sample. Therefore, the length and time scales are linked, so the wide span of length scales in packaged GaN MMICs translates to a wide range of time scales. Different parts of the system contribute to distinct segments of the transient response, where the region near the HEMT responds within nanoseconds, heat spreading in the substrate occurs over microseconds, and heat transfer through the package to the system takes place from about ten microseconds to several minutes. Similarly, thermal coupling occurs dynamically, as the heat flux from a neighbouring heat source takes time to reach the device, depending on the layout, and contributes in the 100 ns to millisecond range. Because each hierarchical level of integration responds to a distinct region of the transient response, the transient response can be used to separate the contributions of uncertain layers in the assembly. The dynamic thermal response is therefore both a source of uncertainty in temperature and a mechanism for understanding the system.

Predicting the channel temperature of a GaN MMIC in a SiP requires modelling the whole

thermal environment: uncertain layers along the path, thermal coupling, and the boundary conditions of the MMIC, package, and system. Because the dissipated power varies in time, the dynamic thermal response must also be considered. What is missing is a systematic description of how the hierarchical levels of integration set the dynamic thermal response, together with test structures that make their individual contributions accessible in situ.

1.1 Aim and objectives

This thesis aims to improve channel-temperature prediction in packaged GaN MMICs by developing methods and models that resolve the dynamic thermal response across length and time scales. The dynamic response arises from several effects that are hard to isolate, so they are investigated separately. This thesis work examines thermal coupling, the impact of the through-substrate via, and MMIC packaging, as outlined in the following objectives. The thesis also relates these effects to other factors that shape the dynamic response of GaN MMICs.

- i The layout design of GaN HEMTs and MMICs has mainly been investigated under steady-state conditions, and the dynamic aspects of thermal coupling should be explored further. The objective is to determine the dynamic thermal response of the thermal coupling in a GaN MMIC and its dependence on heat-source separation, substrate material, operating temperature, and packaging.
- ii The through-substrate via connects the HEMT source to the ground plane on the backside of the MMIC. Although it is essential for high-frequency performance, its role in thermal design has not been comprehensively studied. The objective is to quantify the thermal contribution of the via and to establish its implications for the layout design of multi-channel HEMTs.
- iii Characterising uncertain thermal interfaces and evaluating advanced packaging in situ requires a dedicated thermal test chip. The objective is to establish the design of a thermal test chip with a material system and layout-level heat-dissipation that match those of the GaN MMIC, enabling reliable in situ characterisation.
- iv Cooling and multi-module integration set the boundary conditions for the levels discussed above. Additive manufacturing is a disruptive technology for this domain. An objective of the thesis is to establish an experimental setup to evaluate additively manufactured baseplates with integrated liquid cooling.

This thesis primarily focuses on lateral GaN HEMT technologies implemented in MMICs for microwave electronic systems, rather than power devices and discrete transistors. However, the results are also relevant to other GaN processes and thermal management of integrated circuits in general. The central emphasis is on temperature prediction, with reliability and electro-thermal considerations discussed as appropriate. GaN on silicon carbide substrates is generally considered, as this represents a standard process for lateral GaN HEMTs.

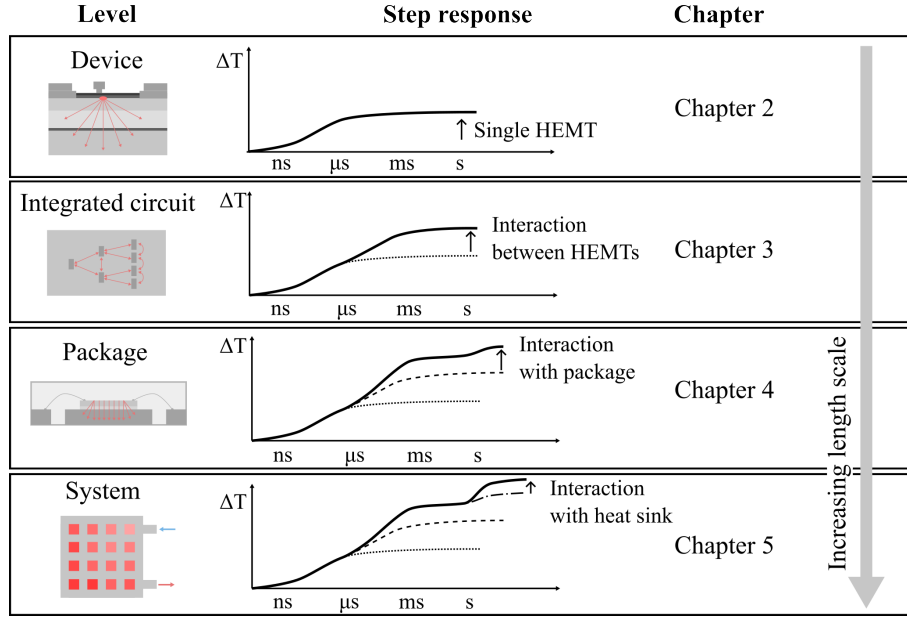


Figure 1.2: Outline of the thesis, showing the four hierarchical levels considered. The graph illustrates how the transient response changes as the hierarchical level's contribution is included.

1.2 Thesis outline

The thesis is organised to describe how each hierarchical level of integration influences the dynamic response of GaN MMICs, as depicted in Figure 1.2. The subsequent chapters are structured as follows:

Chapter 2 begins with an introduction to GaN MMIC technology, introducing the mechanisms of heat generation and transfer within the device. It then discusses the significance of temperature for device reliability and electrical performance. The chapter concludes with an overview of thermal characterisation and modelling methods for GaN MMICs.

Chapter 3 examines how integrating a transistor into a multi-channel device and MMIC circuit alters the dynamic thermal response. The analysis focuses on thermal coupling and through-substrate vias (TSVs). An MMIC example is provided to illustrate these concepts.

Chapter 4 addresses the role of packaging in shaping the dynamic response and emphasises the importance of in situ characterisation methods. The chapter then introduces the design of thermal test chips for this purpose, including a dedicated GaN MMIC thermal test chip.

Chapter 5 explores the impact of system integration on the thermal response and considers the implications for the development of multi-module systems. The chapter also describes an experimental setup developed for evaluating additively manufactured baseplates with integrated liquid cooling.

Chapter 6 concludes the thesis and outlines directions for future research.

Appendix A describes the FEM model used as a reference throughout the thesis.

Chapter 2

Device level

This chapter introduces the GaN HEMT structure and examines the mechanisms of heat generation and transfer within the device. It then discusses the implications for reliability and electrical performance, followed by a review of common thermal characterisation methods. These topics provide background for the following chapters. The finite element method (FEM) simulations presented are detailed in Appendix A.

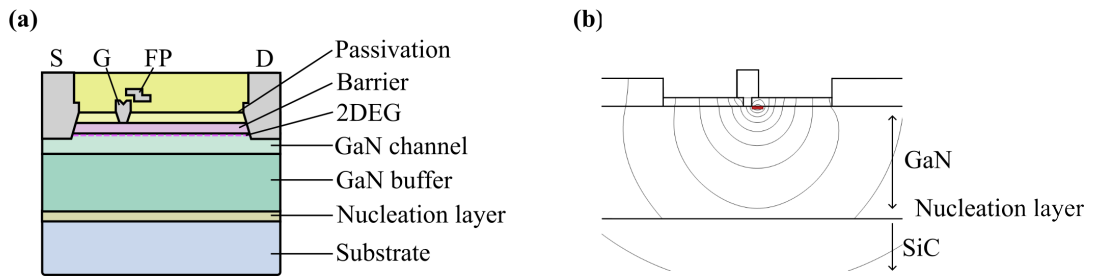


Figure 2.1: Lateral GaN HEMT. (a) Cross-section of a typical device. (b) Contour plot of temperature distribution in the device from FEM simulation (Appendix A).

2.1 Structure and operation of GaN HEMTs

A lateral GaN HEMT commonly resembles the structure shown in Fig. 2.1. It is centred around a heterojunction between the GaN channel and a wider-bandgap barrier, commonly AlGaIn. A two-dimensional electron gas (2DEG) is formed at the interface. The GaN channel layer is commonly thin and grown on a GaN buffer, which can be doped or include a back-barrier to improve performance [15], [16], [17]. A nucleation layer is used between the buffer and the substrate to accommodate lattice mismatches and enable growth. A thicker substrate is used for mechanical support. The choice of materials and their thermal implications are discussed further in section 2.2.

The transistor is formed by ohmic source and drain contacts to the 2DEG, with a gate between them. As in other field-effect transistors, the gate controls the sheet-carrier density in the 2DEG via an electric field. Field plates (FP) are often used to redistribute the electric field and increase the breakdown voltage [18], [19]. The 2DEG is removed outside the active device by implantation or mesa etching of the GaN channel. Several passivation layers protect the heterojunction and support the field-plate.

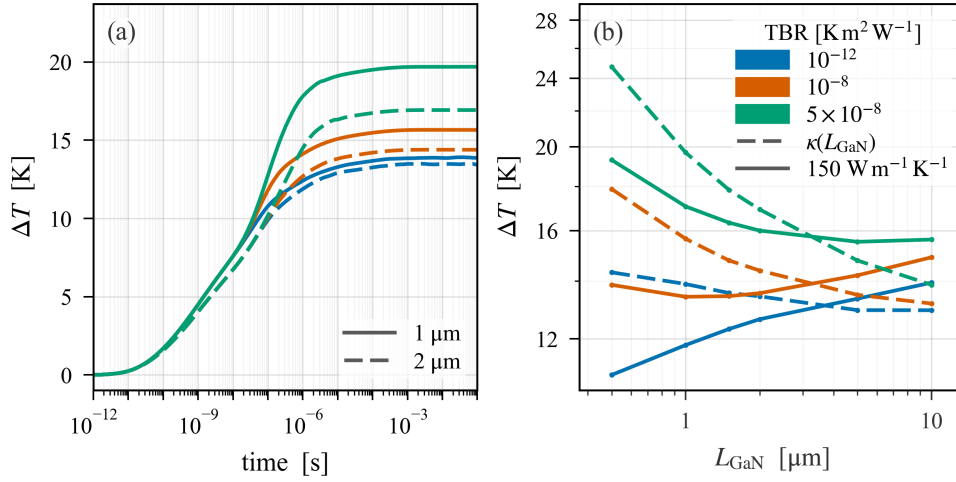


Figure 2.2: Effect of the GaN layer thickness L_{GaN} and the TBR of the nucleation layer on channel temperature. Thickness-dependent thermal conductivity of GaN is used, estimated from [8]. 1 W/mm is dissipated. (a) Transient response for 1 μm and 2 μm GaN layers. (b) Channel temperature versus L_{GaN} with constant (solid) and thickness-dependent (dashed) thermal conductivity of GaN.

2.2 Heat generation and thermal transport

This section describes the heat transfer from the point of generation to the boundary beneath the die.

2.2.1 Heat generation

Heat generation in the device occurs primarily through Joule heating when it is biased at an active operating point. Electrons acquire kinetic energy through acceleration in the applied electric field, subsequently releasing it to the lattice as phonons. The resulting heat dissipation is typically modelled by $Q = \mathbf{J} \cdot \mathbf{E}$, indicating that dissipation follows the spatial distribution of current density, $\mathbf{J}$, and electric field, $\mathbf{E}$. The value of $\mathbf{J} \cdot \mathbf{E}$ is highest at the drain side of the gate under saturation, forming a concentrated hot spot from $< 100 \text{ nm}$ for scaled devices [20] to $\sim 400 \text{ nm}$ wide [2] for larger gate length. This distribution varies with the bias point [21], [22] and the design of the gate and field plate (SFP) [23], [24], [25]. Notably, heat generation occurs on a length scale comparable to the mean free path (MFP) of phonons in GaN, which can vary in magnitude from 100 nm to micrometres [26]. As a result, heat transfer is quasi-ballistic and must be analysed by considering phonon scattering mechanisms rather than assuming purely diffusive heat transfer as in bulk materials [22]. The Joule heating model is only an approximation.

2.2.2 Epitaxial layers and thermal boundary resistance

The epitaxial layers at the device level are also thin relative to the phonon mean free path (MFP). Consequently, boundary effects reduce the effective thermal conductivity of these layers compared to their bulk values as thickness decreases [8], [9]. This effect is particularly significant for the thin nucleation layer between the GaN buffer and the substrate, which

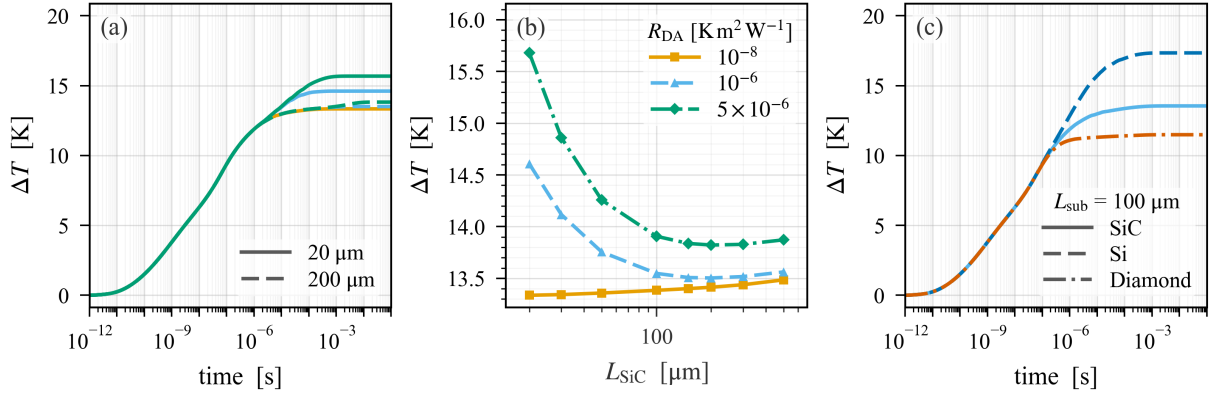


Figure 2.3: FEM simulation of the effect of the substrate for 1 W/mm dissipated power. (a) Transient response for 20 μm and 200 μm L_{SiC} for the die-attach values in (b). (b) Steady-state temperature for a sweep of L_{SiC} for three different R_{DA} values. (c) Transient response for SiC, Si, and diamond substrate.

effectively acts as a thermal boundary resistance (TBR) on the order of $10^{-8} Km^2 W^{-1}$ [10], [11]. Due to its proximity to the hot spot, this TBR contributes substantially to the overall temperature increase. The temperature rise across the TBR depends on the heat flux at the interface. Therefore, the thickness of the GaN layer, L_{GaN} , represents a trade-off between spreading the heat flux before the TBR and minimising the distance to the substrate. Fig. 2.2 illustrates this trade-off for a range of L_{GaN} values and three different TBR magnitudes: $10^{-12} Km^2 W^{-1}$ (negligible TBR), $10^{-8} Km^2 W^{-1}$ (moderate TBR), and $5 \times 10^{-8} Km^2 W^{-1}$ (high TBR). Assuming constant thermal conductivity, an optimal layer thickness can be identified. For $10^{-12} Km^2 W^{-1}$, the thinnest possible layer is optimal. These results highlight the necessity of considering TBR in epitaxial design. When accounting for the thickness dependence of the GaN thermal conductivity, the optimal L_{GaN} shifts to values that are impractical, further emphasising the importance of this dependence. The simulation assumes a 100 nm-wide hot spot, representative of a highly scaled device. Heat dissipation over a broader area would reduce the need for heat spreading and permit a thinner layer. The transient response in Fig. 2.2 shows that the GaN layer changes the transient around the onset of the response. Note that the diffusion length at this time scale is comparable to the phonon MFP, so that FEM predictions might be inaccurate in the ns region, but it is shown for completeness.

Heat is also transferred upward through the barrier to the gate and metallization, influencing the temperature distribution near the hot spot. The thin barrier and passivation layers function as thermal barriers, limiting heat spreading to the metallization layers, which are themselves separated from the hot spot. For substrates with low thermal conductivity and flip-chip mounted MMICs, the top metallization layer may serve as an alternative path for heat removal [27]. Additionally, the use of diamond heat spreaders as passivation layers is being investigated to enhance heat spreading [4]. Nevertheless, heat transfer through the backside is the dominant path and the focus of this thesis.

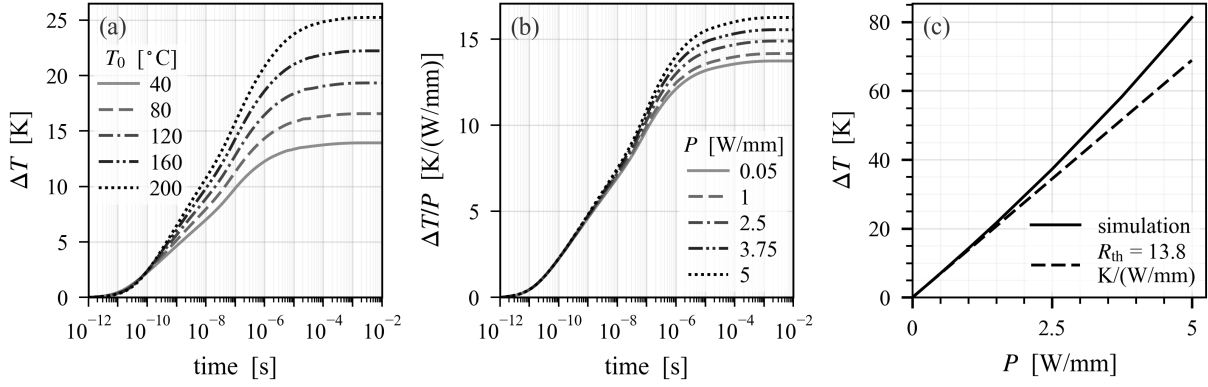


Figure 2.4: Temperature dependence of dynamic response. (a) Transient response for different base temperatures T_0 at 1 W/mm. (b) Transient response, normalised to dissipated power, for different dissipated power levels. (c) Steady-state temperature increase for a sweep of dissipated power. Dashed line shows a linear approximation extracted at low power.

2.2.3 Substrate and die-attach

Silicon carbide is the most commonly used substrate material and provides a high thermal conductivity [28]. The widely used 4H-SiC polytype exhibits an anisotropic crystal structure, resulting in approximately 20% higher thermal conductivity along the lateral direction [28]. This property enables the SiC substrate to function as an effective heat spreader, distributing heat before it reaches the thermal interface at the substrate backside. The impact of substrate thickness, L_{SiC} , is demonstrated in Fig. 2.3 (b). An ideal interface, represented by $R_{DA} = 10^{-8} \text{ Km}^2\text{W}^{-1}$, shows that increasing L_{SiC} leads to a higher channel temperature. In contrast, with a realistic interface of $R_{DA} = 10^{-6} \text{ Km}^2\text{W}^{-1}$, insufficient heat spreading occurs at low L_{SiC} , resulting in an optimal substrate thickness. For higher R_{DA} values, both the steady-state temperature and the optimal thickness increase slightly. Figure 2.3 (a) illustrates how both the magnitude and onset of R_{DA} influence the transient response.

Diamond substrates have very high thermal conductivity and are a leading way to reduce thermal resistance [5]. Fig. 2.3 (c) illustrates the resulting reduction. The change in the response is observed around 200 ns, which is similar to the ~ 70 ns measured with Raman thermography for SiC and sapphire in [29]. However, diamond has been less adopted due to a higher cost. Silicon substrates are commercially available and attractive for compatibility with other silicon processes and for larger wafer sizes, thereby reducing cost. Silicon substrates come at the cost of a lower thermal conductivity, which causes a higher temperature increase in Fig. 2.3 (c). An alternative technique is to grow GaN on a GaN substrate, which has the potential to remove the TBR layer, at the cost of a moderate thermal conductivity in the substrate [30].

2.2.4 Temperature dependency

The thermal conductivity of the considered semiconductor materials decreases with increasing temperature above room temperature [28]. Simultaneously, the specific heat capacity also varies with temperature [31], [32]. These dependencies cause the dynamic thermal response to be temperature-dependent, as illustrated in Fig. 2.4 (a). Additionally, the thermal

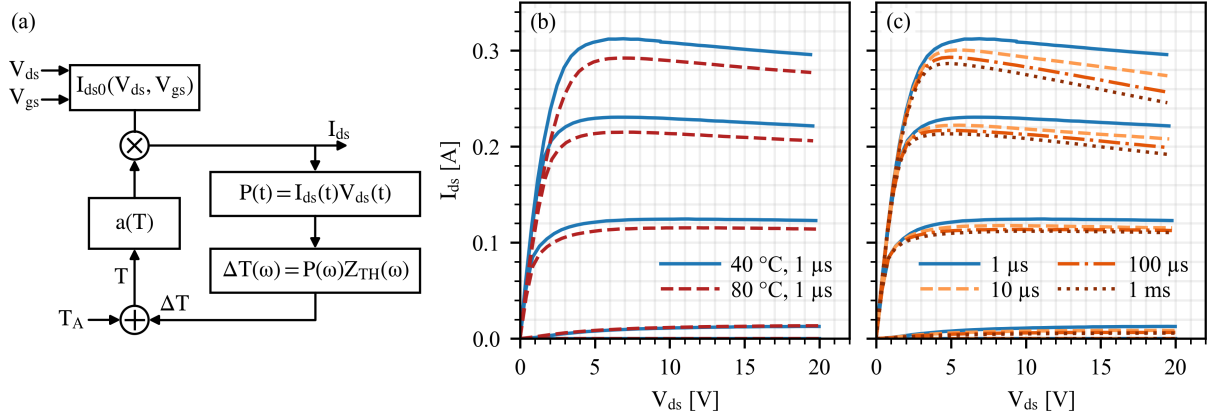


Figure 2.5: (a) Simplified schematic of the electro-thermal feedback loop. (b) Pulsed IV of a $4 \times 75 \mu\text{m}$ GaN HEMT measured on-wafer at 40°C and 80°C set by a thermal chuck with $1 \mu\text{s}$ pulse width. (c) Pulsed IV of the same device at 40°C with different pulse widths.

resistance becomes non-linear, as shown in Fig. 2.4 (b), due to the reduction in thermal conductivity at elevated temperatures resulting from higher dissipated power. In the transient response depicted in Fig. 2.4 (b), the thermal resistance increases during the later stages of the transient as the temperature rises and thermal conductivity decreases. For steady-state temperature versus dissipated power, shown in Fig. 2.4 (c), a linear approximation is reasonable around 1 W/mm , which is used as a reference for simulations in this thesis. For higher power levels, non-linearity must be accounted for.

2.2.5 Separation of layers in time

For the reference case described in Appendix A, the transient thermal response spans from nanoseconds to around 1 millisecond. Each device layer influences the dynamic response differently. Heat remains within a few hundred nm of the hot spot during the first nanoseconds. After approximately 10 ns , the GaN layer begins to affect the temperature, as shown in Fig. 2.2. The substrate's influence becomes apparent after about a hundred nanoseconds, as illustrated in Fig. 2.3. The die-attach boundary impacts the response later, typically between $2 \mu\text{s}$ and 1 ms , depending on the substrate thickness. This dynamic response enables the separation and analysis of effects that would otherwise be combined into a single resistance in a static model. However, overlapping temperature dependencies with other effects necessitate careful consideration.

2.3 Implications of thermal effects

The preceding discussion has addressed the mechanisms of heat generation and transfer at the device level. Temperature is a critical factor, as it degrades both electrical performance and expected device lifetime. To further explain these implications, the following sections discuss electro-thermal effects and reliability considerations.

2.3.1 Electro-thermal effects

The interaction between electrons and phonons, as discussed in section 2.2, leads to heat generation and causes electrical performance to be temperature-dependent. As temperature increases, increased phonon-electron scattering reduces both electron mobility and saturation velocity, thereby decreasing drain current. In amplifiers, this manifests as reduced gain, a lower f_T , and reduced saturation power [33]. The temperature dependence is illustrated in Fig. 2.5 (b), which shows the IV response of a $4 \times 75 \mu\text{m}$ GaN HEMT measured on-wafer at 40°C and 80°C , demonstrating a clear change in the IV characteristics. The measurement was conducted using pulsed operation with microsecond pulses and sufficient cooling time between pulses. The observed decrease in current at high $I_{DS} \cdot V_{DS}$ is attributed to the temperature rise during the pulse, which further reduces the current.

Electro-thermal feedback can be modelled in simplified form as shown in Fig. 2.5 (a). An isothermal current I_{ds0} captures the dependence on V_{DS} and V_{GS} , and the model is scaled by a temperature-dependent factor $a(T)$. The temperature, $T = \Delta T + T_A$, is determined by the dissipated power, with the dynamic response $Z_{th}(\omega)$ completing the feedback loop. The feedback is dynamic, meaning that the temperature increase depends on the waveform applied to the device. This is demonstrated in Fig. 2.5 (c), where measurements at the end of short and long pulses reveal different IV responses mainly due to the higher temperature reached during the longer pulse. This effect is similar to that shown in Fig. 2.5 (b), but the steeper decrease at high $I_{DS} \cdot V_{DS}$ for longer pulses indicates increased thermal resistance. For modulated signals, the RF carrier frequency is higher than the thermal system's cut-off frequency, so the temperature primarily follows the signal envelope, which may fall within the thermal response [34]. The thermal response spans from nanoseconds to several minutes, encompassing a broad range of applied waveforms. The temperature increase exhibits a time delay, causing a phase lag between the thermal response and the applied waveform. This makes thermal feedback a dispersive, memory-dependent effect [12], [13], [14]. Linearization techniques can partially mitigate these effects [35].

Electron trapping is another important source of dispersion and memory effects in GaN HEMTs. The capture and emission rates of traps follow a thermally activated process, so knowledge of the device temperature is important for understanding trapping mechanisms. Further, the trapping effects fall within the microsecond to second range and overlap with the thermal response. This causes a complex interplay between two mechanisms that must be separated, a distinction that can be enabled by accurate knowledge of the dynamic thermal response.

2.3.2 Reliability

Accurately predicting device lifetime is challenging because it depends on numerous statistical processes and varying initial conditions. Device temperature plays a critical role by accelerating failure mechanisms such as diffusion, migration, and chemical reactions, for instance, interdiffusion at the metal-semiconductor interface [36]. The time to failure for these mechanisms follows a statistical distribution, with temperature dependence commonly modelled by the Arrhenius equation in Eq. 2.1, where A is a scaling factor, E_A is the activation energy, k_B is the Boltzmann constant, and T is the temperature. The exponential relationship

between time to failure and temperature imposes a significant penalty for operation at elevated temperatures and increases uncertainty in device reliability.

$$t_{failure} = A \exp\left(\frac{E_A}{k_B T}\right) \quad (2.1)$$

GaN HEMTs are generally expected to operate reliably for years, a condition that cannot be directly validated before deployment. Consequently, reliability assessments rely on accelerated testing, where devices are tested at elevated temperatures and high electric fields. The predicted mean time to failure (MTTF) is then extrapolated from these measurements using statistical distributions and the Arrhenius equation. The measured activation energy typically represents an effective value encompassing multiple failure mechanisms, with reported values for GaN HEMTs ranging from 1.0 to 2.5 eV in [37]. GaN devices also have failure mechanisms that are not thermally activated, such as hot-electron damage [36]. In a comparison of accelerated life testing under RF and DC excitation with the same dissipated power in [38], it was concluded that the consequent temperature was similar for the two methods.

2.3.3 What temperature should be considered

A key consideration in thermal design is determining which temperature metric is most relevant. The temperature influencing the electro-thermal loop represents a weighted average across the device, integrating effects along the gate width and channel length. In contrast, the temperature relevant for reliability assessment should correspond to the specific failure mechanism under investigation. For gate degradation, the peak temperature near the gate, often the highest temperature in the channel, is critical. It is important to use the same temperature definition used in establishing MTTF statistics. Typically, the peak temperature at the hot spot is used for this purpose [39], [40], [41].

2.4 Characterisation and modelling methods

This section presents an overview of principal techniques for characterising and modelling channel temperature. Following the structure in [42], the methods are categorised as optical, electrical, and contact measurements, each of which is discussed in detail in this section. Numerical methods are also addressed. Figure 2.6 illustrates the regions where each method measures temperature.

2.4.1 Optical measurements

Optical thermometry uses the optical properties of semiconductor materials to measure temperature. The three main methods are infrared, thermorefectance and Raman thermometry. They are non-contact and resolve spatial temperature distributions, which suits heat transfer analysis and hot-spot estimation in GaN HEMTs.

Raman thermometry is an active technique in which a laser is directed at the measurement area, and the temperature-dependent Raman shift of the scattered light is analysed [43]. It

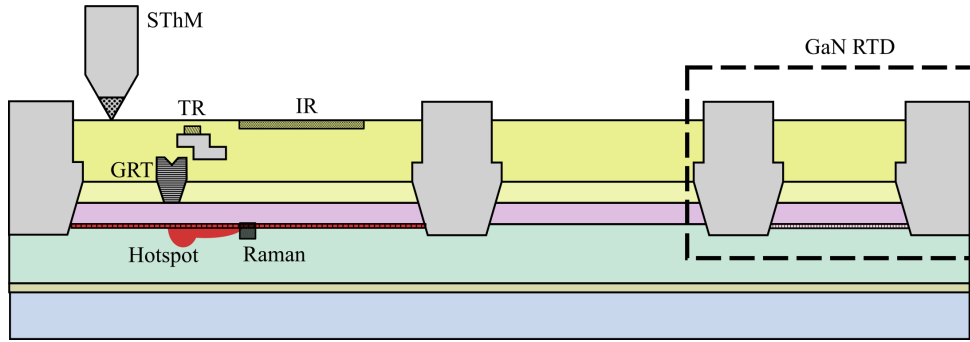


Figure 2.6: Illustration of where the different measurement methods can sense the temperature in a GaN HEMT. Adapted from [39].

offers sub-micrometre spatial resolution and dynamic measurements with nanosecond-scale resolution [29]. Raman thermometry can be configured for depth profiling [44] and can probe through the backside of the substrate to measure hot-spot temperatures [45]. However, it provides an average temperature over a finite volume, which must be taken into account when comparing results with other methods or simulations [43].

Thermoreflectance is another established active technique that measures temperature based on the temperature dependence of the reflectance of incident light. This method achieves sub-micrometre spatial resolution and high temporal resolution [46], [47]. Thermoreflectance is also employed for material characterisation [48].

Infrared thermometry is a passive technique that detects infrared radiation emitted from the device and is suitable for quick measurements of large structures. Its spatial resolution is limited, and it is reported to underestimate the peak temperature [49]. The low emissivity and IR transparency of GaN can be addressed with a coating [49].

2.4.2 Electrical device measurements

Temperature-sensitive electrical parameters (TSEPs), such as on-resistance or threshold voltage, can be calibrated against known temperatures and subsequently used to probe device temperature [50], [51]. They reflect the temperature that governs electrical performance, which is what electro-thermal models need. However, TSEPs yield an average channel temperature [52] and do not offer a localised estimate of the hot spot. Additionally, the calibration is device-specific, necessitating measurements on multiple devices to predict temperatures for different geometries. Contributions from parasitic impedances, the bias network, and electron trapping in the active device must also be considered. Pulsed IV measurements with short pulses from a quiescent bias point are commonly used as baseline measurements, as short pulses minimise temperature rise during measurement. Nevertheless, delivering sufficiently short pulses for isothermal measurement at nanosecond resolution is often infeasible.

2.4.3 Contacting device measurements

Contact temperature measurements have been conducted using the tip of a scanning thermal microscope (SThM), achieving spatial resolution down to the hundreds-of-nanometers scale

[53]. A primary challenge of this method is its invasiveness, as the probe physically interacts with the sample. Measurements are taken at the top of the passivation layer to avoid disturbing the active device. Alternatively, integrated temperature sensors, such as resistance temperature detectors (RTD) [54], [55], [56], diodes [57], and thermocouples [58], can be placed near the device. These sensors must be designed to minimise invasiveness and are generally positioned at some distance from the hot spot, thereby limiting their sensitivity to the actual peak temperature. Gate-resistance thermometry (GRT) is a notable technique in which the gate itself functions as an RTD, providing a well-defined probe near the hot spot. GRT has been identified as an important method for devices with a source-field plate [59]. GRT has also been employed to study dynamic thermal response [60]. GRT averages over the gate width, and the separation from the hot spot must be considered. Further, it requires a dedicated test structure. In [59], a temperature increase is seen for GRT after < 100 ns. This is a similar time scale to the temperature increase observed on the gate using thermoreflectance in [46], where the gate temperature is delayed relative to the GaN channel temperature.

In this thesis, contacting temperature measurements are conducted using a compact GaN 2DEG resistor as an RTD. This approach was first described in [61] and paper [b]. The 2DEG resistor offers several advantages: it exhibits strong temperature dependence, enabling reliable measurements; it is located at the surface of the GaN layer, eliminating thermal interfaces between the sensor and heat dissipation; it can be integrated into a compact area, facilitating well-defined point measurements; and it utilises the same fabrication process and stack-up as the device, allowing for compatibility with commercial manufacturing processes without modification. The dimensions of the 2DEG resistor represent a trade-off between achieving a compact area for point measurement and meeting manufacturing constraints. The area must also be selected to provide sufficient resistance for accurate measurement and to ensure that the resistor's value remains significantly higher than the metal trace's resistance, thereby minimising the influence of the metal's temperature dependence. The impact of temperature dependence of ohmic contact resistance is minimal [62]. Before use, the 2DEG resistor must be characterised to ensure measurement correctness. This is accomplished by heating the sample on a thermal chuck and measuring its conductance at various temperatures. A polynomial fit is then applied to model temperature as a function of measured conductance. Because the 2DEG resistor exhibits non-linear behaviour [61], characterisation must be performed near the intended bias point. The bias point should be selected to balance the need for sufficient current for reliable measurement, minimal power dissipation, and reduced trapping effects [61]. Variations in resistance among small 2DEG resistors have been observed; therefore, individual calibration is necessary before measurements.

2.4.4 Numerical methods

Numerical methods are important for technology development and device design. They are also required to interpret experimental measurements, assess measurement validity, and estimate hot-spot temperatures that are not directly accessible. The three principal numerical approaches are summarised below.

Monte Carlo

Monte Carlo (MC) simulations capture the statistical physics of phonon transport and are thus a suitable method for analysing ballistic heat transport near the hot spot [22]. However, these simulations require extensive computational resources to achieve convergence, limiting the feasible size of the computational domain. As a result, MC methods are primarily applied to materials studies and simplified structures. Additionally, they depend on complex physical models and specialised simulation tools.

Finite-element method

Finite-element method (FEM) simulations of the Fourier heat equation, as presented in Eq. 2.2, are more computationally efficient for complex three-dimensional geometries. FEM solvers numerically discretise the domain into finite elements connected by a mesh, enabling the solution of the differential equation. Simulations require the material density (ρ), specific heat capacity (C_p), and thermal conductivity (κ). The heat dissipation term (Q) must be specified to represent the volumetric heat generation described in section 2.2. Appropriate boundary conditions are necessary to ensure that the system is solvable. The mesh must be sufficiently refined near the hot spot to capture steep temperature gradients accurately. Mesh density can be reduced in regions farther from the hot spot to improve computational efficiency.

$$\rho(\mathbf{r})C_p(\mathbf{r}, T) \frac{\partial}{\partial t} T(\mathbf{r}, t) - \nabla \cdot (\kappa(\mathbf{r}, T) \nabla T(\mathbf{r}, t)) = Q(\mathbf{r}, t) \quad (2.2)$$

Eq. 2.2 only holds for diffusive heat transfer, i.e. when the length scale is large compared with the phonon MFP. However, this is not the case for the geometries around the gate, and the hot spots are smaller than the MFP, leading to underestimation of the peak temperature [22], [63]. Further, this is not the case for the thin epitaxial layers in the device, so effective material values for these layers must be considered. Still, FEM is used for peak temperature estimation [39], [40], [41]. Further, it works well to predict the implications of the layout and package, for which it is used in this thesis. Finally, FEM is a valuable tool for multi-physics simulations, in which thermo-mechanical and electro-thermal simulations can be performed.

Analytical models

Analytical models are the most efficient way to approximate the temperature distribution, but they rely on simplifying assumptions and often do not capture the full physics of the system. They are useful for fast geometry optimisation, and for approximating the dominant thermal time constants [64]. A common compact model is the use of equivalent thermal networks, which approximate the heat transfer by thermal resistances and capacitances. Such networks can be solved effectively using electrical circuit solvers, where voltage models temperature and current models dissipated power. Foster networks are often used because they are easy to fit to measured responses, as in paper [B]. However, translations to Cauer form are truer to the physical system.

2.5 Chapter summary

Heat is generated in a hot spot on the drain side of the gate, approximately 100-400 nm wide under typical operating conditions. It spreads through layers whose thickness is comparable to the mean free path of phonons in the material. Heat transfer is therefore quasi-ballistic, and the heat transfer at thin layers will differ from that predicted for bulk materials. Further, heat transfer is temperature-dependent, making it a non-linear problem. In time, the device level occupies nanoseconds in the GaN layer and reaches microseconds to milliseconds as heat spreads in the substrate.

The chapter established two things that the following chapters use. The choice of layer thickness is a trade-off between spreading the concentrated heat flux from the hot spot before the thermal interface materials and maintaining a short distance to the heat sink. Which temperature matters depends on its purpose; electrical performance is governed by the average temperature in the active region, and the peak temperature near the gate typically governs reliability. The reviewed methods complement each other.

Chapter 3

Integrated circuit level

This chapter examines the changes that arise when a single-channel device (Chapter 2) is integrated into a multi-channel device and an integrated circuit. At this hierarchical level, both device layout and integrated circuit configuration influence channel temperature. Thermal coupling between heat sources and the impact of boundary conditions, including the MMIC boundary, MMIC backside, and through-substrate via, collectively determine the temperature distribution. Understanding these effects is essential for designing circuits that balance electrical and thermal performance.

3.1 Thermal coupling

Distributing power across parallel HEMT channels is advantageous from a thermal perspective at a fixed total power dissipation, as it spreads dissipated power over a larger area and reduces heat flux. However, when heat sources are positioned in proximity, the heat flux from one source elevates the temperature at adjacent locations. This thermal interaction, referred to as thermal coupling, increases channel temperature and results in a non-uniform temperature distribution across the MMIC. To understand this effect, this section first analyses a two-channel example before extending the discussion to multi-channel devices and an MMIC configuration.

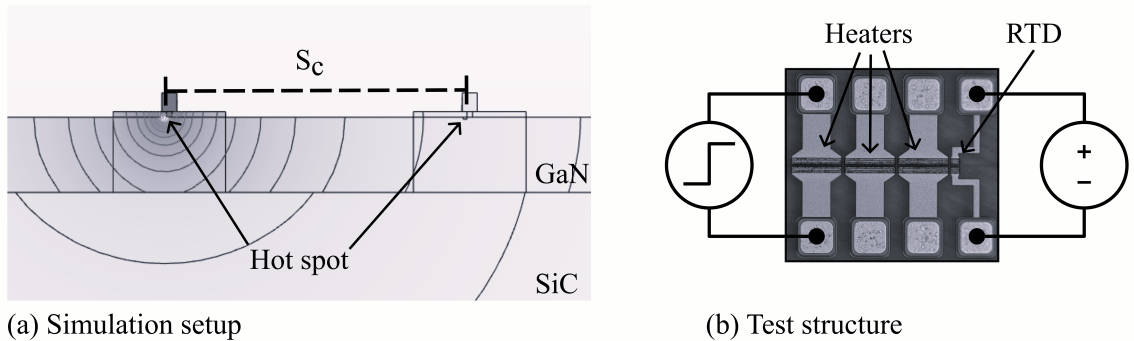


Figure 3.1: (a) Simulation setup with two GaN HEMT channels separated by a spacing S_C between the hot spots. The contour shows the temperature distribution when heat is dissipated only in the left channel. (b) Test structure from paper [A].

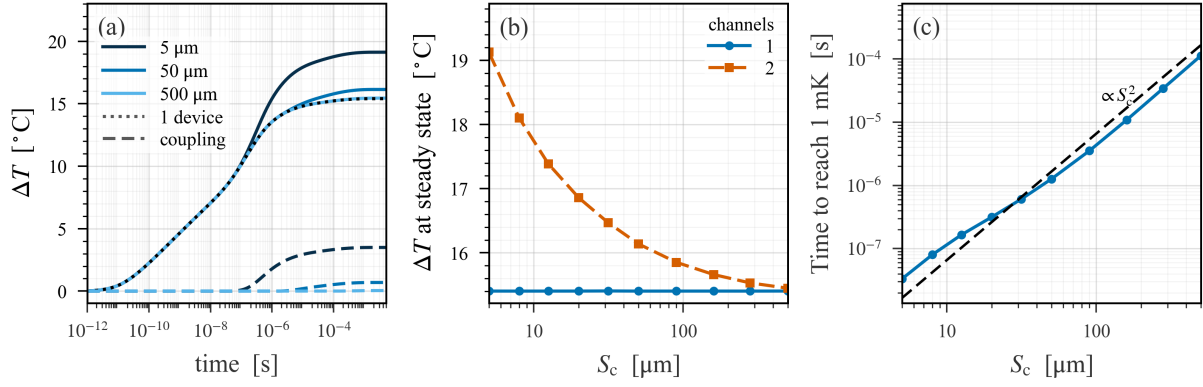


Figure 3.2: Simulated transient response for two channels for 1 W/mm. (a) Transient response with 5, 50, and 500 μm separation, and with single-device result plotted with dotted lines. The coupling term shows the temperature added to the second channel when only the left channel dissipates heat. (b) Steady-state temperature increase as a function of S_C for a single channel and two channels. (c) Time before the coupling reaches 1 mK for a sweep of S_C .

3.1.1 Two-channel device example

Thermal coupling is initially examined using a two-channel transistor, as shown in Fig. 3.1 (a). In this configuration, two transistors are separated by a distance S_C between their respective hot spots. Fig. 3.2 (a) illustrates how the transient response deviates from that of a single device when an additional channel dissipates heat at separations of 5, 50, and 500 μm . A pronounced temperature increase is observed for a 5 μm separation after about 100 ns. A similar difference after 500 ns due to thermal coupling was measured with Raman thermometry in [65] for S_C of 30 μm . The effect is less pronounced for 50 μm and low for 500 μm . A separate way to investigate thermal coupling is to dissipate heat just in the left channel, as shown in Fig. 3.1 (a), and monitor the resulting temperature rise in the adjacent channel. This response is represented by the dashed "coupling" lines in Fig. 3.2 (a). For a separation of 5 μm , thermal coupling becomes significant after approximately 100 ns, while the response at 50 μm is delayed and lower. This is the same way as thermal coupling was investigated in paper [A], described further in section 3.1.5. The factors influencing this coupling response are discussed in more detail in the following paragraphs, using FEM simulations with parameters calibrated to the measurements in the appended papers. In Figs. 3.3 - 3.7, one parameter is varied about a common reference case drawn in black, further described in Appendix A, designed to resemble a typical device. In these plots, S_C values of 20 μm , 50 μm , and 160 μm are compared, where 20 μm resembles the spacing between two neighbouring channels. The values 50 μm and 160 μm correspond to coupling to channels farther away in a multi-channel device.

Separation

Increasing the separation between two heat sources reduces the heat flux arriving from the neighbour, and with it the thermal coupling in Fig. 3.2. As found in paper [B], thermal coupling can be interpreted as a low-pass-filtered response to transient heat dissipation, with both the magnitude and cut-off frequency of the response decreasing as the separation

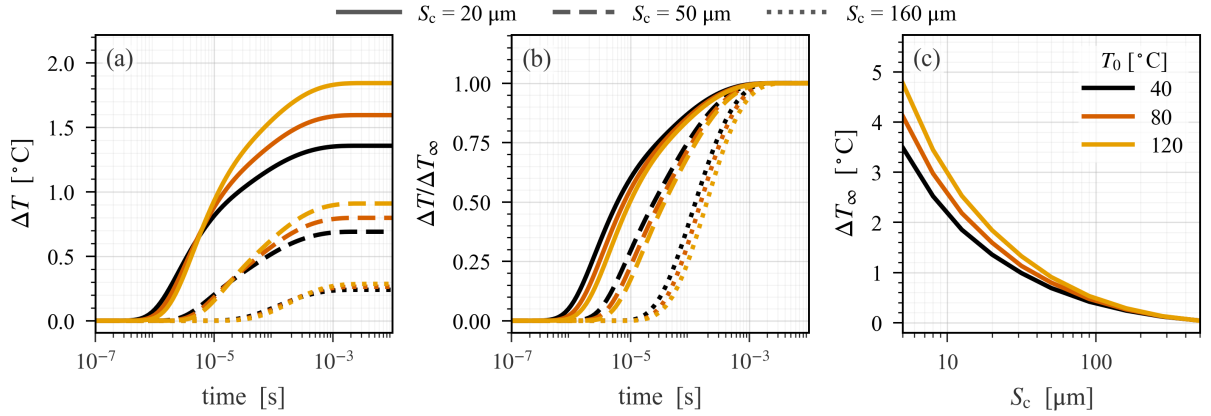


Figure 3.3: Thermal coupling for 40°C, 80°C, and 120°C base temperature for 1 W/mm. (a) Transient response. (b) Transient response normalised by its steady state value. (c) Steady state value, ΔT_∞ .

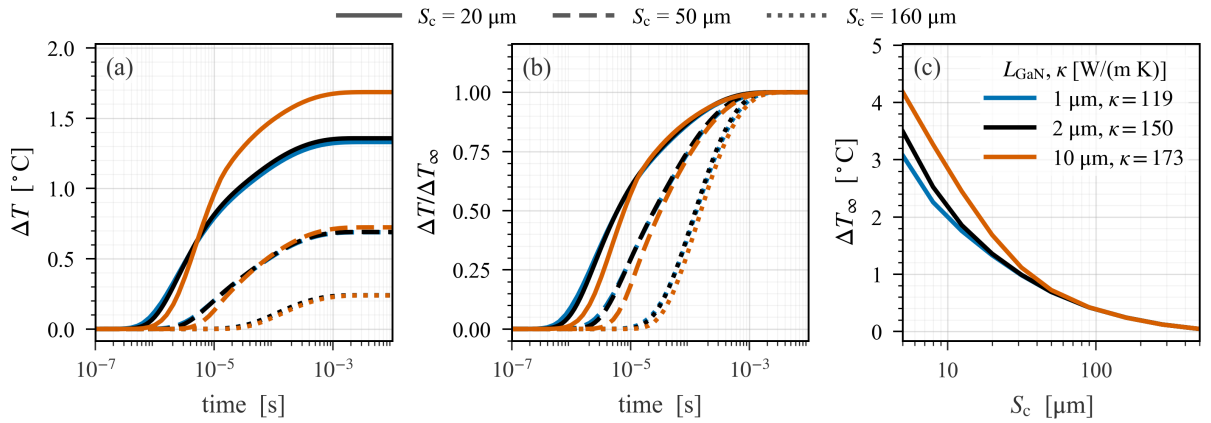


Figure 3.4: Thermal coupling for 1 μm , 2 μm , and 10 μm GaN layer thickness for 1 W/mm. Panels as in Fig. 3.3.

increases. The steep rise at small S_C in Fig. 3.2 (b) is the penalty for short channel separations. As the cut-off frequency shifts, the onset of the transient response is increasingly delayed with greater separation. In Fig. 3.2 (c), this delay approximately follows an S_C^2 dependence, consistent with the diffusive scaling $t \propto S_C^2/\alpha$ of transient heat conduction [66]. Deviations from the S_C^2 trend arise from the more complex structure, including three-dimensional heat spreading across multiple layers, interactions with the boundary beneath the MMIC, and variations in thermal conductivity, which are discussed in the following paragraph. Additionally, using a 1 mK temperature increase as the extraction point introduces artefacts, since it corresponds to a different fraction of the final increase for each separation. While using a fraction of the total temperature increase would be more physically accurate, a fixed 1 mK threshold is more practical for defining when coupling starts to change the response.

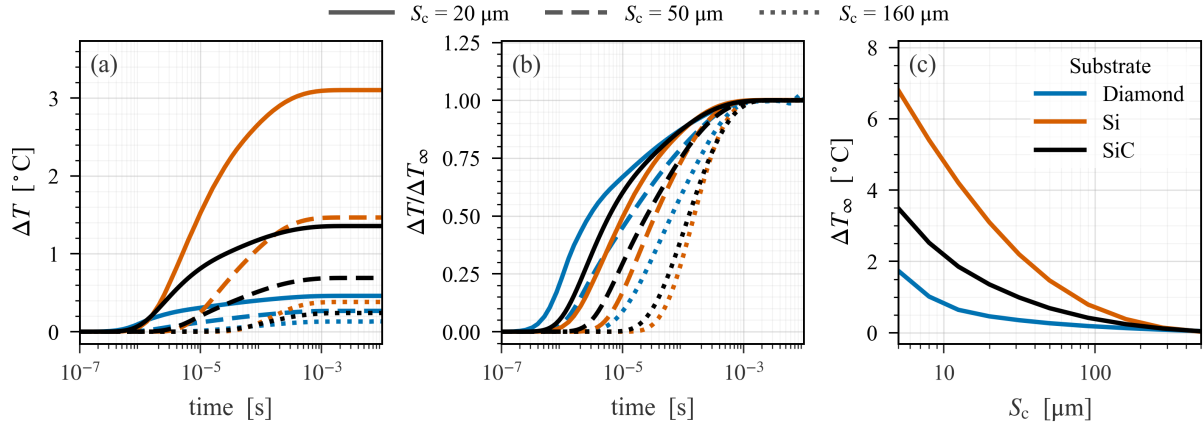


Figure 3.5: Thermal coupling for SiC, Si, and diamond substrates for 1 W/mm. Panels as in Fig. 3.3.

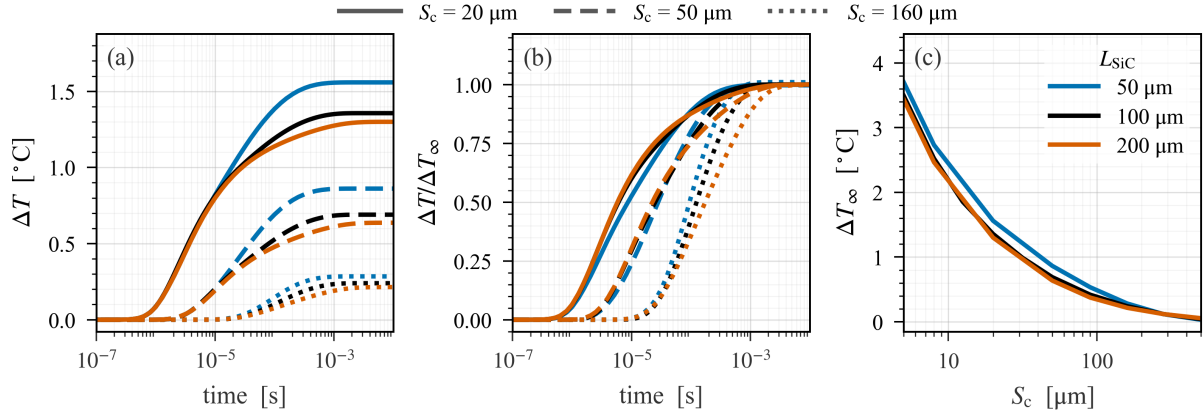


Figure 3.6: Thermal coupling for three different substrate thicknesses L_{SiC} for 1 W/mm. Panels as in Fig. 3.3.

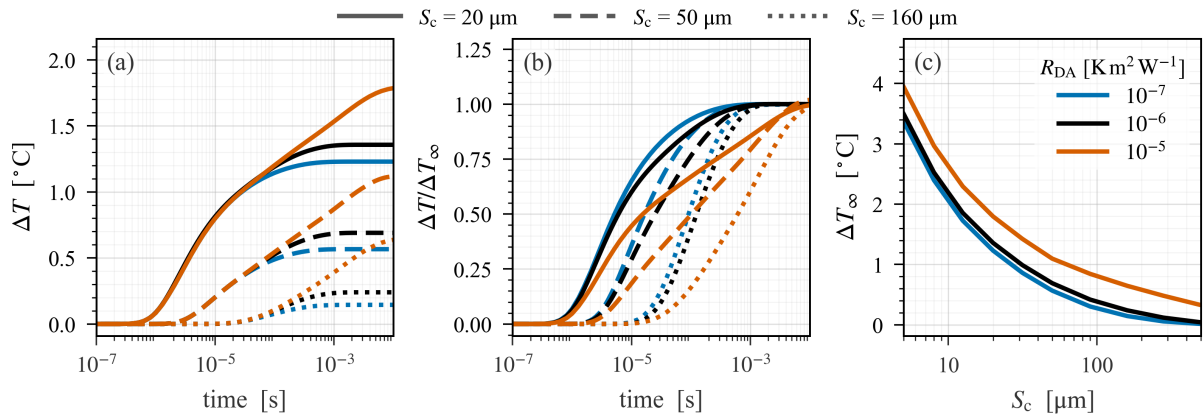


Figure 3.7: Thermal coupling for three different die-attach resistances R_{DA} for 1 W/mm. Panels as in Fig. 3.3.

Temperature

An increase in temperature reduces the thermal conductivity of the substrate, as discussed in Chapter 2, so that the heat flux from a neighbouring heat source results in a higher temperature increase, as shown in Fig. 3.3. The reduced thermal diffusivity also delays the onset of the thermal coupling response, as observed in Fig. 3.3 (b), which aligns with measurements reported in paper [A]. The layout should therefore be evaluated at the intended operating temperature, since a room-temperature assessment underestimates both the coupling and its onset time at elevated temperatures.

GaN layer

The GaN layer is important to consider since it is where the heat is generated. However, the GaN buffer is typically 1-2 μm , which is considerably thinner than the relevant separation between the HEMTs. As a consequence, the differences in the GaN layer mainly change the response for low S_C , when the GaN layer thickness is comparable to S_C . This is seen in Fig. 3.4, where a small change is seen comparing a GaN thickness of 1 μm to 2 μm for short S_C , but the change is negligible for large S_C . A GaN thickness of 10 μm is simulated as an extreme, indicating that the sensitivity to the GaN layer increases for a thicker GaN layer, as more of the heat spreading takes place in the GaN layer for this case.

Substrate material

The influence of substrate material is assessed through simulations using SiC, Si, and diamond substrates, as shown in Fig. 3.5. For consistency, the thickness and epitaxial layer are matched to those of the SiC reference, although these parameters may vary in practical devices. Silicon has lower conductivity and thermal diffusivity; therefore, the coupling response has a higher magnitude and occurs later than in the SiC reference. The opposite is observed for the diamond substrate, whose higher thermal conductivity and diffusivity yield a lower magnitude and a slightly earlier response. Fig. 3.5 (c) suggests a larger channel spacing for GaN-on-Si than for GaN-on-SiC, whereas diamond allows more compact devices [67].

Substrate thickness and die attach interface

Both substrate thickness and the resistance of the die-attach interface (R_{DA}) influence the die-attach contribution (Figs. 3.6, 3.7), as detailed in section 2.2.3. Substrate thickness affects the heat flux at the interface, while R_{DA} determines the resulting temperature rise. This behaviour should be interpreted in terms of the ratio between S_C and L_{SiC} . When $S_C \ll L_{SiC}$, the die-attach effect manifests later in the transient response, and when $S_C \sim L_{SiC}$, the impact is evident from the onset. The temperature distribution thus depends on the package as well as on the layout and material system, so layouts should be designed for the intended package, where a lower R_{DA} permits shorter channel separations. Substrate thinning increases sensitivity to R_{DA} , as discussed in section 2.2.3.

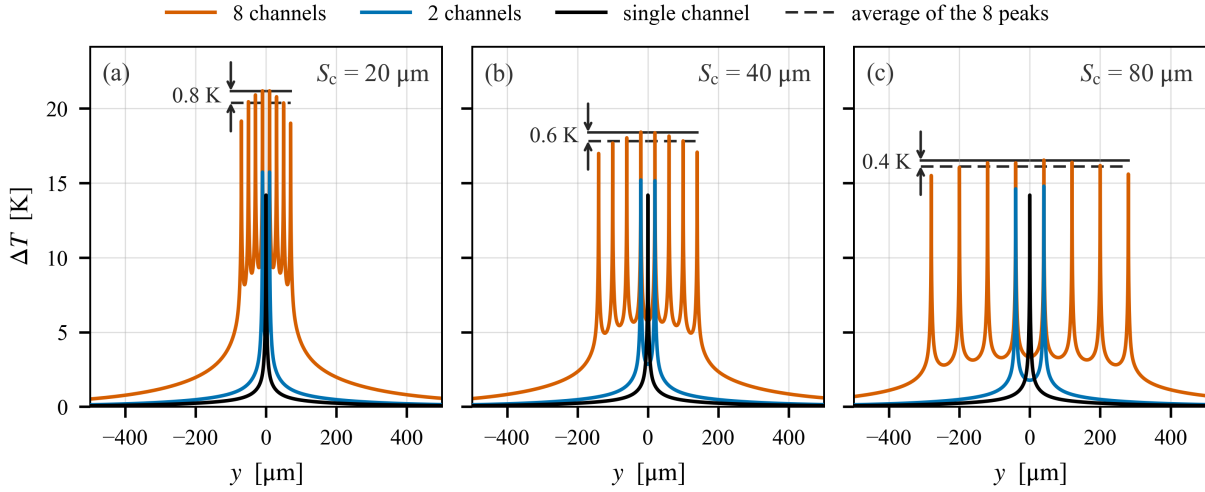


Figure 3.8: Steady state temperature distribution across the channels for a single channel, two channels, and eight channels for 1 W/mm. Three different spacings are considered, with (a) $S_C = 20 \mu\text{m}$, (b) $S_C = 40 \mu\text{m}$, and (c) $S_C = 80 \mu\text{m}$. The difference between the peak channel temperature and the average of the eight peak temperatures is marked for the eight-channel.

3.1.2 Scaling to a multi-channel device

Incorporating additional channels into a device has three primary consequences. First, as illustrated in Fig. 3.8, increasing the number of channels raises the channel temperature. Here, S_C of $20 \mu\text{m}$ is typical for GaN MMIC transistors. With S_C of $20 \mu\text{m}$, the peak temperature increase is 21.2°C for eight channels, compared to 15.7°C for two channels. Increasing S_C to $40 \mu\text{m}$ reduces the peak temperature increase to 18.4°C , and further to 16.5°C at $80 \mu\text{m}$. This trend is attributed to the cumulative heat flux from multiple sources. These simulations assume uniform power density across all channels. If the total dissipated power remains constant, distributing it across more channels reduces the temperature because of the larger area. However, for constant power density, adding channels increases the overall temperature.

A second observation is that integrating more than two channels results in a nonuniform temperature distribution. This occurs because edge channels are, on average, farther from other channels and thus experience less thermal coupling. In Fig. 3.8, the peak channel temperature exceeds the average peak temperature by 0.8°C for S_C of $20 \mu\text{m}$, decreasing to 0.6°C and 0.4°C for S_C of $40 \mu\text{m}$ and $80 \mu\text{m}$, respectively. The consequences of this uneven temperature are twofold. First, the peak temperature constrains the maximum allowable power density, so optimal output power is achieved with a uniform temperature distribution in which every channel sits at the limit. An uneven distribution is therefore a sign of unused potential. Second, an uneven temperature distribution also implies that the channels operate under different conditions, resulting in minor differences in transconductance, threshold voltage, and related parameters. This can introduce amplitude and phase imbalances, particularly since HEMT channels are combined in phase. Literature reports strategies to limit peak temperatures and promote uniformity, such as non-uniform channel separation [68], distributed gate [69], and circular HEMT designs [70]. Because coupling sets in only after 100 ns to 1 microsecond,

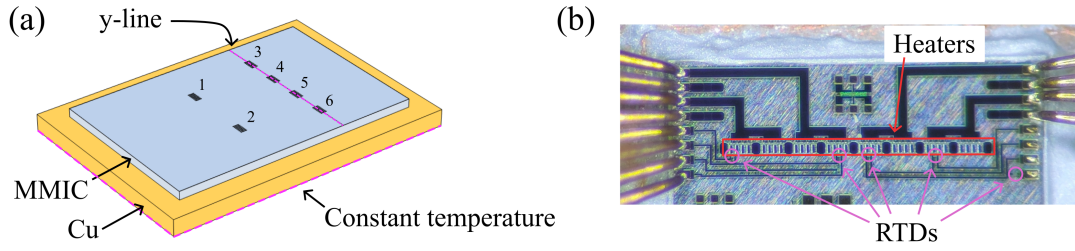


Figure 3.9: (a) FEM implementation of MMIC example with six eight-channel HEMTs with $75\ \mu\text{m}$ gate width and S_C of $20\ \mu\text{m}$. The HEMTs are arranged to resemble a power amplifier with a driver stage (1,2) and an output stage (3-6). (b) shows the test structure investigated in paper [B].

the device temperature stays nearly uniform during short pulses, so layouts should be tailored to the intended waveform.

A third observation is that a multi-channel device has a different sensitivity to the material stack-up compared to single-channel devices. When eight channels operate at the same power density, the total heat flux at the MMIC boundary increases, making the multi-channel device more sensitive to the die-attach interface and the later packaging than a single-channel device would be.

3.1.3 MMIC layout

The weak coupling at large separations in Fig. 3.2 suggests that coupling between multi-channel devices on the same MMIC is small. However, the aggregate heat flux from multiple channels leads to a measurable temperature increase, raising the peak temperature increase by $\sim 10\%$ in the example below. Paper [B] experimentally investigated this phenomenon using the test structure shown in Fig. 3.9 (b), which features eight closely spaced multi-channel heat sources. Transient measurements with integrated RTDs demonstrated that thermal coupling substantially influences both temperature distribution and transient response. To put paper [B] in context, this section simulates the MMIC in Fig. 3.9 (a), which models a GaN MMIC power amplifier with four HEMTs in the output stage and two HEMTs in the driver stage. The complete simulation setup is detailed in Appendix A. This configuration represents a more spacious MMIC layout compared to the more compact output-stage layout examined in [B], which is the worst-case design thermally.

Figure 3.10 illustrates the evolution of the surface temperature distribution in the MMIC example, with the corresponding transient response presented in Fig. 3.11 (a). At $1\ \mu\text{s}$, the temperature remains largely confined within the single-channel cell, and devices display similar temperature profiles along the y-line (see Fig. 3.9 (a)). By $100\ \mu\text{s}$, heat has diffused beyond the single-channel cell, resulting in a non-uniform temperature distribution among the channels, although this distribution remains consistent across devices. After $1\ \text{ms}$, heat dissipation extends across multiple devices, and simulations with all multi-channel HEMTs dissipating heat exhibit higher overall temperature compared to those with a single multi-channel device, as reflected in the transient response of Fig. 3.11 (a). At $10\ \text{ms}$, the transient

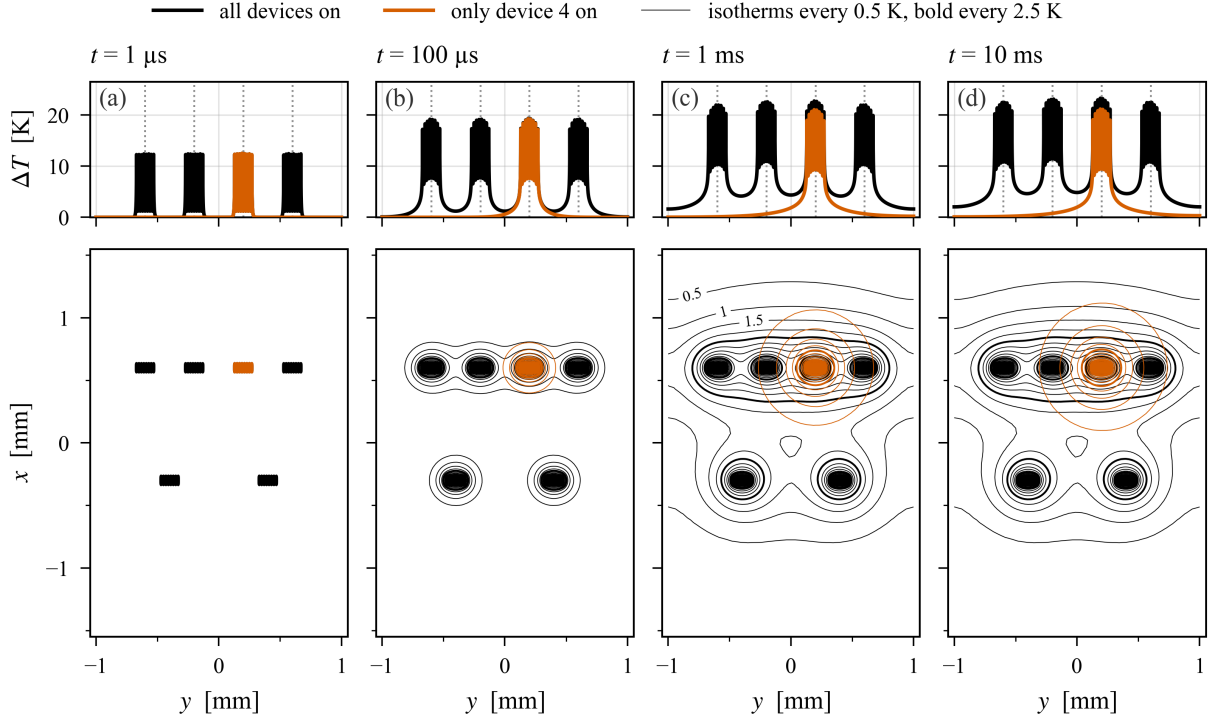


Figure 3.10: Evolution of the surface temperature of the MMIC example at $1 \mu\text{s}$ in (a), $100 \mu\text{s}$ in (b), 1 ms in (c), and 10 ms in (d). The case with all devices dissipating power is shown in black, and only device 4 dissipating power is shown in orange. The top shows the temperature along the y-line in Fig. 3.9 (a). The bottom shows a contour plot of the surface temperature distribution. Each device dissipates 1 W/mm .

response approaches steady-state conditions, as evidenced by the small change from 1 ms to 10 ms . Examination of the temperature profile along the thickness in Fig. 3.11 (b) reveals that the temperature rise over the die-attach increases due to the higher heat flux toward the die-attach boundary. This increases the sensitivity to packaging. These three contributions are separable in time. Heat transfer before 100 ns to $1 \mu\text{s}$ is mainly within the single-channel cell. Thermal coupling between channels occurs until around $100 \mu\text{s}$, and coupling between HEMT cells occurs on the millisecond timescale. These observations are consistent with measurements reported in paper [B].

Thermal coupling between HEMTs therefore matters both for predicting device temperature and understanding the influence of the layout. However, full 3D FEM simulations are too slow for a circuit design flow in which layout, bias and waveforms are varied iteratively. A more practical approach is an equivalent thermal network described by a thermal coupling matrix [71], which was implemented in paper [B]. An example of such a matrix is provided in Eq. 3.1, where T_i denotes the temperature of heat source i , P_j is the power dissipated in source j , and T_A is the ambient reference temperature. The diagonal elements Z_{ii} correspond to self-heating, while the off-diagonal elements represent thermal coupling between sources.

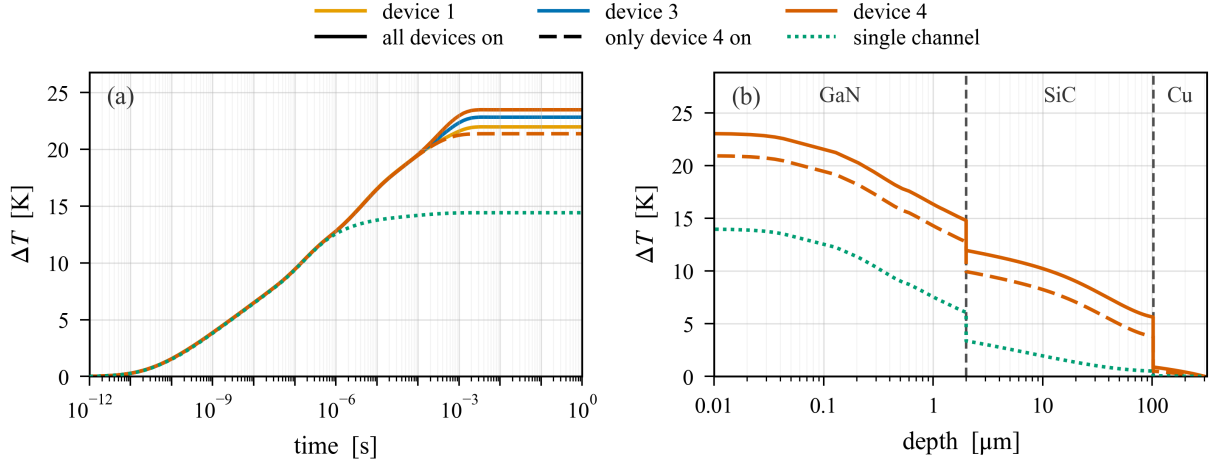


Figure 3.11: (a) Transient response of devices 1, 3, and 4 for the MMIC example, with all devices dissipating (solid) and only device 4 (dashed) compared to a single channel. (b) Temperature against depth for the centre channel in device 4. 1 W/mm dissipated power.

$$\begin{bmatrix} T_1(\omega) \\ T_2(\omega) \\ \vdots \\ T_i(\omega) \end{bmatrix} = \begin{bmatrix} Z_{11}(\omega) & Z_{12}(\omega) & \cdots & Z_{1j}(\omega) \\ Z_{21}(\omega) & Z_{22}(\omega) & \cdots & Z_{2j}(\omega) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{i1}(\omega) & Z_{i2}(\omega) & \cdots & Z_{ij}(\omega) \end{bmatrix} \cdot \begin{bmatrix} P_1(\omega) \\ P_2(\omega) \\ \vdots \\ P_j(\omega) \end{bmatrix} + T_A \quad (3.1)$$

Each term is a thermal impedance that captures the dynamics, realised with equivalent thermal resistances and capacitances so that it can be simulated in an electrical solver. In paper [B], a linear network was employed to characterise the impact of thermal coupling on the dynamic response of the power amplifier. A limitation of the linear network approach is its inability to capture non-linear system behaviour arising from temperature-dependent heat transfer in semiconductor materials. Consequently, the linear model is most appropriate for small-signal evaluations of dissipated power and operating temperature, as conducted in that study. The extraction is similar to the integration of electromagnetic simulations in MMIC design, where FEM simulations are used to derive an equivalent network that more accurately reflects the physical environment than an analytical model.

3.1.4 Boundary condition

The heat flux at the MMIC boundary also affects layout design. In the appended papers, heat transfer from the MMIC sides is typically assumed to be negligible and modelled as an adiabatic boundary condition. This boundary condition reduces the available volume for heat to spread, thereby increasing the device temperature. Paper [a] demonstrated, through transient measurements on devices with varying proximity to the boundary, that close placement to the boundary significantly elevates temperature. An adiabatic boundary can be conceptualised as thermal coupling from a mirror heat source located on the opposite side of the boundary. The coupling matrix in paper [B] reveals that the diagonal elements Z_{ii} vary depending on device separation from the boundary, as a consequence of this.

3.1.5 Characterisation method

A central contribution of this thesis is the direct measurement of thermal coupling using transient measurements on dedicated test structures, building on [61]. The test structure used in paper [A] is shown in Fig. 3.1 (b), and the structure in paper [B] is shown in Fig. 3.9 (b). In these structures, heat dissipation is generated using an ungated GaN 2DEG resistor, and a compact GaN 2DEG resistor is used as an RTD (Section 2.4.3) to measure the thermal coupling at different separations from the heat source. This is a similar structure to that investigated in [61] and in papers [a], [b], and [d]. The same principle is also used in [B] and [c] for the thermal coupling at the MMIC level. In paper [C], it is used to investigate interaction with the TSV.

In the course of this work, it became clear that the same test structures are useful for more than characterising thermal coupling. The measurements in paper [A] showed that the structure can also be valuable for calibrating an FEM model, using the different sensitivities discussed in section 3.1.1. An advantage of calibrating based on such a structure is that it yields a simpler experiment than measurements on a real device, since heat dissipation is easier to resolve in a resistor than in a gated device. A limitation of the measurement technique is that it does not capture the hot-spot temperature and cannot approach the hot spot to within a couple of μm . Therefore, the FEM simulation of heat transfer in the channel cannot be accurately calibrated with this method and must rely on alternative methods or reference values from the literature, as done throughout this thesis (Appendix A). The strength of the method is its ability to isolate other effects that affect the dynamic response outside of the region near the HEMT channel, which the sensor can resolve. The structure could also be used when comparing technologies, to understand thermal contributions of substrate, die-attach and coupling, which affect electrical measurements.

3.2 Influence of the through-substrate via

In an MMIC process, the through-substrate via (TSV) connects the top metallization to the backside ground plane. The term TSV is commonly used in the literature to denote a through-silicon via, but here it refers to a through-substrate via for GaN MMICs on SiC substrates. The TSV is formed in an MMIC process by etching through the substrate and plating a thin metallization layer on the via wall. It is conventionally used in a GaN HEMT to electrically connect the source contact to the ground plane on the backside of the MMIC. For multi-channel devices, this may lead to a lower source inductance, L_S , of the HEMT than routing the ground connection via the top metal layer. This is important, as L_S is known to degrade the high-frequency performance of the HEMT [72]. Increasing the number of vias has been shown to reduce L_S , and is therefore proposed as an attractive solution for high-frequency MMICs [72], [73], [74], [75].

The integration of the source-via generally classifies the layout of a multi-channel GaN HEMT. The internal-source-via (ISV) layout denotes a layout where a TSV is integrated at each source contact, as illustrated in Fig. 3.12 (a). A more compact device can be realised by placing TSVs only at the outermost source contact and connecting the internal source contacts via air bridges, which is denoted as an outside-source-via (OSV) layout. A simplified schematic of the difference in the embedding network is shown in Fig. 3.12 (b), showing that the ISV

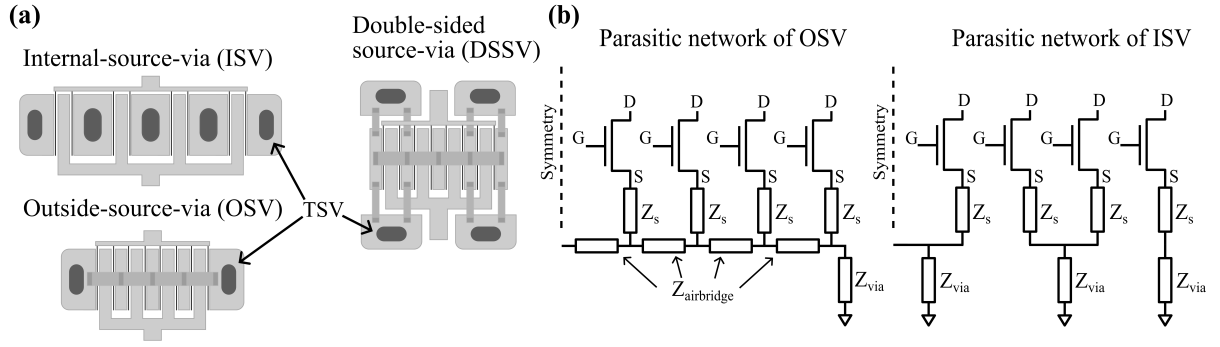


Figure 3.12: (a) Layout of multi-channel HEMT in internal-source via, outside-source via, and double-sided source-via configuration, drawn to scale. (b) Parasitic network of the OSV and ISV layout compared [73].

connects each source contact directly to ground, so the via inductance appears in parallel and L_S is reduced. The OSV, by contrast, has the sources connected in series through the air bridges to the outermost source contacts, resulting in a higher L_S . One should note that variations exist in which, for instance, two four-channel OSVs can be connected with a shared TSV in the centre to form an intermediate solution. An alternative, more complex solution is the double-sided source-via (DSSV) proposed in [76], and illustrated in Fig. 3.12 (a). Moving the TSV to the side enables a more compact transistor cell while maintaining a direct connection from each source contact to the TSV, thereby making the electrical performance comparable to that of the ISV. However, it complicates the matching networks because the input and output manifolds must be routed around the via.

The implications of the TSV for the thermal response have been uncertain. In GaAs, gold has a higher thermal conductivity than the substrate, so it is reported to be beneficial for thermal management in [77]. This has been discussed less for GaN-on-SiC substrates, which is why this is addressed in paper [C]. The experimental results and FEM simulations show that TSVs increase the temperature in GaN-on-SiC MMICs. They also reduce thermal coupling with devices on the other side of the TSV. This is attributed to the void in the centre of the TSV, since its thin gold metallisation conducts less heat than the removed SiC. The boundary in the void limits 3D heat spreading in the SiC substrate from the hot spot in the channel, thereby increasing thermal resistance. An increase in thermal resistance was also reported in [77].

From the discussion in section 3.1, one can expect the ISV layout to have lower thermal resistance than the OSV, as the channel pairs are separated. The contribution of the TSV is to raise the temperature near it in both the ISV and OSV layouts. This leads to a higher peak channel temperature and a more uniform temperature distribution, as the outer TSVs increase the temperature of the edge channels. In paper [C], simulating the ISV layout with its spacing unchanged, but with only the outermost TSVs resembling an OSV, resulted in a lower peak channel temperature than when all TSVs are included. This shows that the internal TSVs increase the thermal resistance. Paper [C] found that the two layouts have different sensitivity to the design parameters. The ISV is more sensitive to the TSV-channel distance, as this distance also affects channel spacing. However, the ISV is less sensitive to TSV size

because the heat flux interacting with the TSV is lower due to larger channel separations. In practice, multiple source TSVs reduce L_S , which sets the achievable gain at high frequencies. However, the TSV reduces heat spreading and increases R_{th} . Moving from OSV to ISV improves both, but at the cost of an increased device footprint. At a constant footprint, a trade-off between L_S and R_{th} must be considered.

The discussion in paper [C] primarily identifies the TSV as a problem in the thermal management of GaN-on-SiC. However, the use of thermal vias has also been proposed in the literature. Metal vias and thick backside metallization have been proposed to improve thermal management for GaN-on-Si in [78], where the substrate was etched under the GaN, and the void was filled with copper. The use of diamond, with its higher thermal conductivity, has also been explored in [79]. A common denominator is that the thermal via only makes sense if the via can transfer heat better than the substrate, while also accounting for the longer path and the resistances involved in getting the heat to the thermal via.

3.3 Chapter summary

This chapter has analysed the dynamic thermal response of GaN MMICs at the integrated-circuit level, focusing on thermal coupling, MMIC boundary interactions, and the role of through-substrate vias. Thermal coupling between channels is driven by heat flux from neighbouring channels, which increases the temperature around the channel. Dynamically, it manifests as a low-pass-filtered response to dissipated power, with both the magnitude and the cut-off frequency decreasing as the separation from the heat source increases. The extent of thermal coupling is influenced by material stack-up, thickness, operating temperature, and package interface. In multi-channel HEMTs, thermal coupling contributes to elevated operating temperatures and non-uniform temperature distributions, a trend also observed across devices within an MMIC. This dynamic phenomenon occurs over timescales ranging from 100 ns to several ms.

The MMIC boundary is an additional layout consideration, as an adiabatic boundary functions as a mirrored heat source, increasing the temperature of nearby devices. The through-substrate via serves as a boundary adjacent to the HEMT channel in GaN-on-SiC, limiting heat spreading from the channel and increasing thermal resistance. This must be considered in the layout design. The ISV layout was found to perform better than the OSV layout, but this is attributed to its larger device footprint rather than the presence of the TSV. For a fixed device footprint, the TSV placement is a trade-off between L_S and R_{th} .

The test structures described in the appended papers are valuable for isolating and analysing these effects. These structures are also effective for calibrating FEM models, which can be used for layout design and for extracting equivalent thermal networks.

Package level

The packaging of an integrated circuit serves an important purpose in connecting the IC mechanically, electrically, and thermally to the surrounding system. Packaging matters here because it defines the boundary for heat transfer from the IC, which is critical for analysing the effects of substrate thickness and thermal coupling. It is also important to understand the system's dynamic response from $\sim 10\ \mu\text{s}$ onward. Packaging also protects the IC from environmental factors, and its reliability directly impacts product lifetime. Typically, the package is significantly larger than the IC, making it a key SWaP-related limiting factor. Therefore, there is a drive for package miniaturisation and the integration of additional functionality within a single package to enhance performance. The packaging level thus involves multiple trade-offs beyond thermal considerations. This chapter provides an overview of the challenges associated with conventional and emerging packaging for GaN MMICs. It discusses the use of thermal test chips to understand the trade-offs governing these packages.

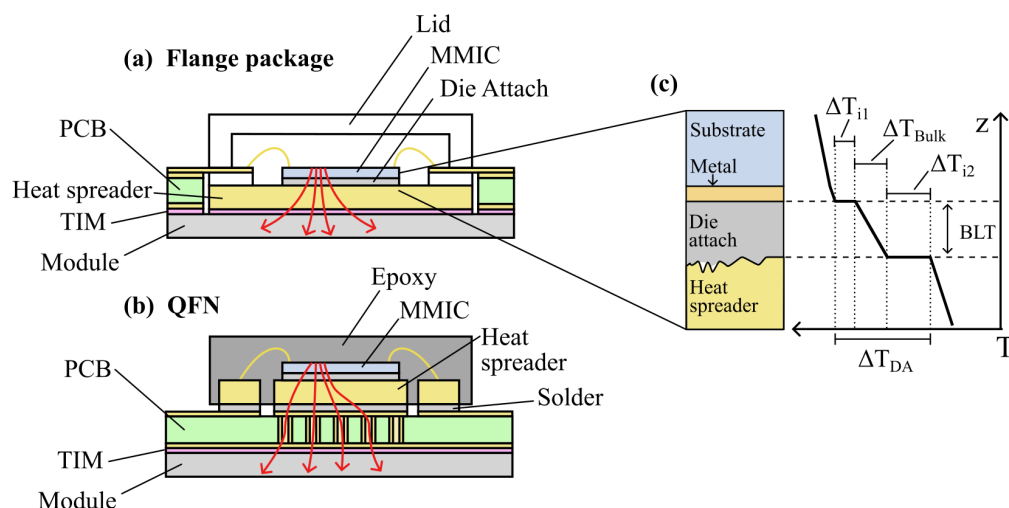


Figure 4.1: Conventional GaN MMIC integration. (a) Flange package. (b) Quad-flat no-leads package. (c) Illustration of temperature distribution over the die-attach interface. Red arrows indicate the dominant path of heat transfer.

4.1 Packaging of GaN MMICs

This section examines the primary layers influencing heat transfer in conventional GaN MMIC packages. Additionally, it addresses the trend toward advanced packaging and its implications for thermal characterisation.

4.1.1 Conventional GaN packaging

Historically, GaN HEMTs have been packaged using a flange assembly, as illustrated in Fig. 4.1 (a). In this configuration, the MMIC is mounted with a die-attach onto a larger heat spreader, with bond wires providing electrical connections to a lead frame, and a ceramic cavity protecting it. The flange is then mounted onto a module with a thermal interface material (TIM) positioned between the flange and the module. This packaging approach, evaluated in paper [D], facilitates heat transfer primarily through the MMIC backside, spreading across the heat spreader before reaching the TIM and the module. This configuration is used for the highest power levels, mainly because the flange can be made thick to enhance heat spreading.

An alternative, more compact package is the quad-flat no-leads (QFN) package, shown in Fig. 4.1 (b). The QFN is designed to be soldered directly onto a printed circuit board (PCB) for both electrical and mechanical connection. However, from a thermal perspective, this introduces higher thermal resistance beneath the package when the heat must be transferred through the PCB to a heat sink. At the same time, it uses a smaller heat spreader, so the heat spreads over a smaller area before reaching the second thermal interface. The QFN is embedded in epoxy, which has a low thermal conductivity compared to the heat spreader.

The thermal management strategies for these two conventional packages are similar. Heat is transferred from the MMIC through the die-attach interface, and the heat spreader distributes the heat over a larger area before it reaches the subsequent thermal interface to the system. The following sections provide a detailed discussion of the die-attach, heat spreader, and secondary TIM.

Die attach interface

The die-attach interface is critical for establishing the mechanical connection between the MMIC and the package, providing electrical contact to the MMIC's backside ground plane, and facilitating thermal transfer to the package. Traditionally, solder has been used to form a metallic bond with the heat spreader, providing reasonable thermal conductivity. Conductive epoxy is also used, though it has a lower thermal conductivity. Paper [D] primarily investigates die-attach interfaces based on the sintering of silver particles, which represents a promising lead-free material and can achieve high thermal conductivities.

Previous sections have modelled the die-attach as an effective resistance R_{DA} . In practice, it is a combination of several resistances, as illustrated in Fig. 4.1 (c). Considering only the bulk thermal conductivity of the die-attach material (κ_{DA}), the expected thermal resistance is approximately BLT/κ_{DA} , where BLT denotes the bond line thickness of the interface. However, there will also be interface resistance (R_{i1}, R_{i2}) between the MMIC metallization and the heat spreader.

$$R_{DA} = R_{i1} + \frac{BLT}{\kappa_{DA}} + R_{i2} \quad (4.1)$$

The interface resistance is influenced by interdiffusion, which forms the metallurgical bond but creates a lower-conductivity interfacial layer. Surface roughness, oxidation, and voids further increase resistance by reducing the true contact area. The interface resistance can be comparable to the bulk resistance, as reported in paper [D], but is difficult to predict because it depends on surface characteristics, material properties, and the attachment process. The value of κ_{DA} is also often uncertain, since it depends on porosity resulting from the attach process. Consequently, in situ characterisation of the die-attach interface is critical, particularly because it is the region of the package with the highest heat flux.

Heat spreader

The heat spreader provides mechanical support for the MMIC and distributes heat flux before the subsequent thermal interface. Selection of the heat spreader material cannot be based solely on high thermal conductivity, since the coefficient of thermal expansion (CTE) must also be considered. Variations in system temperature, such as during power cycling, cause expansion and contraction due to CTE. CTE mismatches between materials introduce stress in interconnects and the die-attach that, over time, leads to interconnect failure. As an example, copper has a CTE of 17.7 ppm/K compared to around 4.7 ppm/K for a SiC substrate [80]. The strain on the bond line scales with the distance from the neutral point on the die [81]. Larger dies or thinner BLT are therefore more prone to failure, which conflicts with what is best from a thermal standpoint. The CTE mismatch further limits the permissible temperature difference across the package. As a result, CTE-matched heat spreaders with lower thermal conductivity must be considered for devices operating at elevated temperatures. Beyond thermal conductivity, the dimensions of the heat spreader are critical, as they determine the area available for heat spreading. The thickness of the heat spreader also determines the volume before the second thermal interface, which depends on thickness in the same way as for the substrate discussed previously. The impact of these dimensions was demonstrated in paper [D]. Notably, the diamond heat spreader investigated in paper [D] showed that diamond is a promising material for enhanced thermal performance, a conclusion also supported by [82], [83], [84].

Thermal interface material

A secondary thermal interface material (TIM) is applied to the backside of the heat spreader to secure the package and minimise thermal interface resistance resulting from imperfect contact due to surface roughness. The MMIC exhibits lower sensitivity to this interface compared to the die attach, since the heat spreader reduces the heat flux. Consequently, the thermal performance requirements for this interface are less strict. However, as shown in paper [D], the importance of the second TIM increases with package miniaturisation and reduced heat spreading before the interface. Additional considerations include accommodating thermal expansion associated with larger package sizes and ensuring that the TIM maintains its properties and does not degrade or dry out over the product's lifetime.

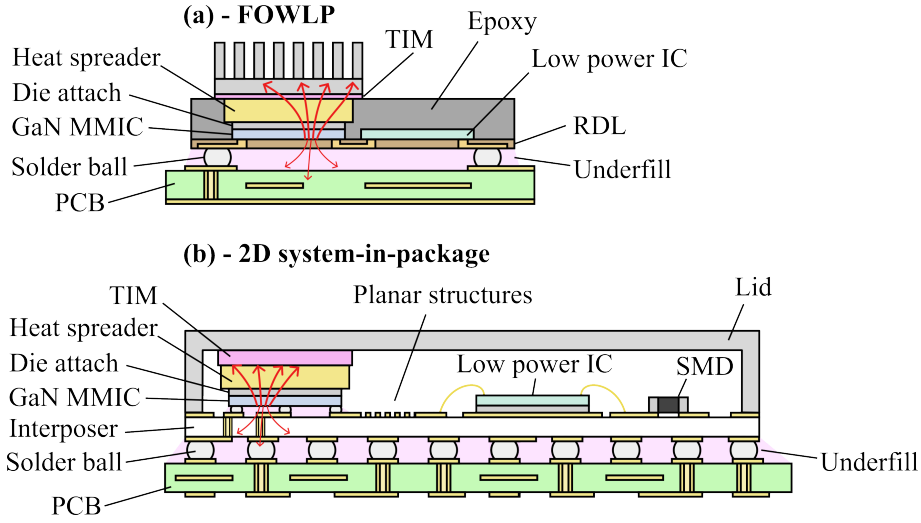


Figure 4.2: Two examples of advanced integration of GaN MMICs. (a) Fan-out wafer-level package, where a redistribution layer connects a GaN MMIC and a low-power IC [85]. (b) Two-dimensional system-in-package, where several integrated circuits and passive components are integrated on a shared interposer. Red arrows indicate the dominant path of heat transfer.

4.1.2 Advanced packaging

A significant trend in the field is the heterogeneous integration of GaN technology into advanced packages, which enables the combination of GaN with other technologies to improve performance, miniaturisation, and functionality. Fig. 4.2 illustrates two examples of advanced packages. In (a), a fan-out wafer-level package (FOWLP) similar to [85] is shown, where a GaN device and a lower-power IC are co-packaged and interconnected via a redistribution layer (RDL). A heat spreader can also be integrated into the high-power device [85], [86] to facilitate backside heat removal, in contrast to the QFN package, which dissipates heat through the PCB. The main advantages of FOWLP are miniaturisation and a reduction in the number of interconnects.

Fig. 4.2 (b) illustrates a two-dimensional system-in-package (SiP), where multiple integrated circuits and passive components are assembled on a shared interposer. The interposer can be fabricated from semiconductor, ceramic, glass, or organic substrates. SiP technology reduces the physical separation between components compared to discrete packages, leading to miniaturisation and improved electrical performance by reducing interconnects. Consequently, SiP is the established approach for advanced systems such as central processing units (CPU) and is a promising solution for future microwave electronics.

The transition from conventional GaN packaging (see Section 4.1.1) to advanced packaging introduces new challenges. Key considerations relevant to this thesis are discussed below.

Multiple heat-transfer paths. The integration of flip-chip packaging or a redistribution layer enables a second heat-transfer path through the upper metallization, which can improve cooling. This should be seen in the context of efforts to integrate diamond heat spreaders on the MMIC topside [4].

Multiple interfaces. An advanced package introduces a more complex system with additional interfaces. The heat transfer through these interfaces will be uncertain and must be characterised in situ. Further, these interfaces must be considered as potential failure points.

Materials with low thermal conductivity. Advanced packages often must be manufactured at low temperatures, for instance, during RDL dielectric formation and when underfill is added to flip-chip-mounted MMICs. The materials used in these processes typically have a low thermal conductivity, which limits heat transfer.

Reduced volume for heat spreading. A miniaturised package reduces the volume for heat spreading. This will reduce thermal performance, so the package must be characterised to confirm a safe operating temperature. Earlier, an uncertain operating temperature could be compensated for with a larger volume margin for heat spreading, but this margin is lost with improved SWaP.

No optical access. A central challenge, as illustrated in Fig. 4.2, is the lack of optical access to the active device. This implies that optical methods cannot be used for thermal characterisation. In conventional packages, optical access could be achieved by removing the lid or measuring without the protective epoxy. However, such approaches are not feasible when these interfaces are required for cooling or electrical connection.

Limited electrical access. Electrical access to devices on an MMIC in advanced packages is only available through the package ports. The transmission line between the package port and the device complicates de-embedding when measuring device intrinsic performance. This makes thermal characterisation using TSEP less attractive.

Thermal coupling. Thermal coupling from other components integrated in the same SiP must be considered. As with thermal coupling at the integrated-circuit level, it will raise the operating temperature, increase the heat flux at later interfaces, and lead to a more uneven temperature distribution.

4.2 Thermal test chips

This section addresses the characterisation of packaged devices. Although the optical, electrical, and contact-based methods discussed in section 2.4 can be applied, simpler test chips are often needed to enable more straightforward and reliable analysis. This applies especially to packages without optical access (Section 4.1.2), which are expected to become more common. A thermal test chip (TTC) is an integrated circuit specifically designed for controlled thermal experiments to evaluate the thermal performance and reliability of IC packages. This section reviews the requirements for TTCs, proposed TTC designs, and the dedicated GaN TTC developed in this thesis.

4.2.1 Requirements of TTCs

A TTC incorporates a heat source with known dissipation and an integrated temperature sensor to measure the resulting temperature rise, in steady state or as a transient. Guidelines for its design are given in the JEDEC standard, JESD51-4A, which establishes a common platform for comparing the performance of semiconductor packages [87]. This section outlines the requirements for such a device based on this approach.

Heater requirement. Heat dissipation in a TTC should be generated using a well-defined heat flux, typically achieved with resistive heaters based on thin-film resistors. Accurate measurement of power dissipation requires a 4-wire connection, and the heater should exhibit minimal temperature dependence to facilitate straightforward operation. The heat dissipation should be relevant to the intended application, often designed to dissipate power approximately uniformly across the area and to cover as much of the area as possible [87], [88], thereby emulating a typical CMOS circuit. For more complex systems, such as CPU emulators, arrays of sub-cell TTCs are used [89]. The dissipation in these sub-cells can be adjusted to replicate realistic power maps and simulate CPU operation.

Sensor requirement. The temperature sensor should be easy to measure and have a good temperature sensitivity. Most commonly, the sensor is implemented using a thin-film RTD or a diode [87]. The contact to the sensors should also be made via a 4-wire connection to reduce the influence of the lead resistance. Further, the sensor should have low power dissipation to avoid affecting the measurement. The dimensions of the sensor depend on its purpose. A compact sensor is well-suited for point measurements and can be used to resolve the spatial temperature distribution. A larger sensor is good for capturing the average temperature in an active region, such as an active cluster on a CPU.

Mechanical requirements. The TTC should be designed for its intended attachment process, depending on whether flip-chip or wire bonding is used. Further, it should be manufactured with a material system that matches the intended technology to achieve similar heat transfer, CTE, and surface metallization, ensuring bonding. The IC thickness should also match to get a realistic sensitivity to the package.

Additional test structures. A thermal test chip should also include additional structures to investigate the package and understand potential failure mechanisms. Daisy chains are often used to investigate potential failures in electrical interconnects. The integration of sensors for relative humidity [90] and mechanical stress [91] is also investigated by others.

4.2.2 Dedicated thermal test chip for GaN MMICs

A thermal test chip (TTC) is a suitable method for in situ characterisation of a GaN MMIC integrated into an advanced package, as illustrated in Fig. 4.2. For this application, a TTC with a material system matching that of a GaN MMIC is required, and a comparable heat-dissipation source should be implemented to address the high, concentrated heat flux in GaN MMICs. Previous efforts include TTCs integrated on SiC substrates in [92] and [93], designed to resemble integrated circuits on SiC and operate at elevated temperatures. However, these designs utilise large resistors to dissipate heat. A more realistic heat-dissipation profile was proposed in [94], though within a silicon technology. In [95], a GaN-on-SiC structure was investigated using thin-film resistors dissipating heat in the same area as the transistor mesa, but without integrated temperature sensors. Similarly, [96] describes a TTC with GaN-on-SiC that uses large tantalum nitride thin-film resistors and GaN HEMTs, and also lacks integrated temperature sensors.

Chapter 3 established that the thermal coupling response measured in papers [A] and [B] demonstrated high sensitivity to the die-attach boundary. Building on this, paper [D] proposed a similar approach to realise the thermal test chip shown in Fig. 4.3 (a). The TTC is

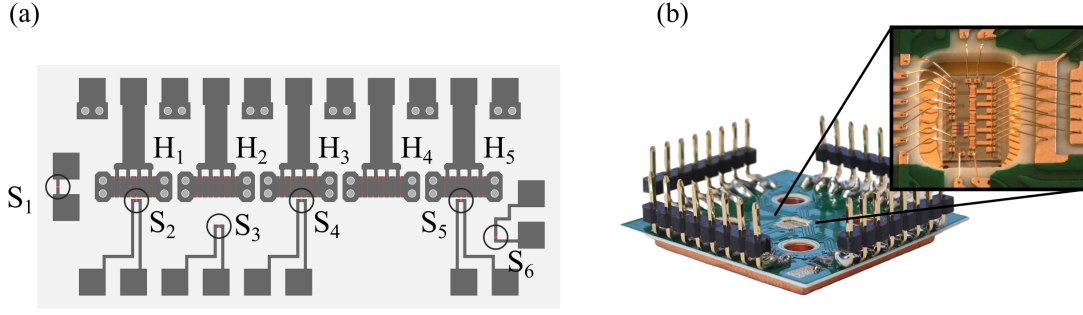


Figure 4.3: TTC design investigated in paper [D]. (a) The TTC layout, with five heat sources $H_1 - H_5$ and six temperature sensors $S_1 - S_6$. (b) TTC mounted on a copper heat spreader and wire-bonded to a PCB.

fabricated using commercial GaN-on-SiC technology to ensure an identical material system. Heat dissipation is achieved through a design that replicates a multi-channel HEMT layout, providing a realistic heat dissipation profile. The device is ungated to simplify heat dissipation, ease implementation of the structure in FEM simulations, and enable more controlled thermal experiments. The power is then distributed as approximately uniform heat over the channel [5], [44]. This is acceptable since the TTC is intended to characterise the package, rather than peak channel temperature.

Temperature sensors are implemented using compact GaN 2DEG resistors, as discussed in Section 2.4.3. Compact temperature sensors are advantageous for evaluating spatial temperature distributions. Three considerations govern sensor placement: (1) three sensors are positioned as close as possible to the heater to monitor the local temperature distribution; (2) additional sensors are placed at increasing distances from the heat source to use varying sensitivities to heat transfer, as demonstrated in papers [A] and [D], thereby improving understanding of the material system; and (3) sensors are arranged symmetrically around the centre to assess the uniformity of heat transfer within the package.

The investigation presented in paper [D] demonstrates the application of the TTC in the demonstrator shown in Fig. 4.3 (b), which resembles the conventional package shown in Fig. 4.1 (a). The results indicate that the TTC exhibits good sensitivity to the die-attach layer, heat spreader, and secondary TIM. An advantage is that this sensitivity is directly linked to an actual MMIC's sensitivity to these layers. Employing transient measurements and sensor measurements at varying separations enables the separation of different layers' contributions. The method does not require optical access and can therefore be used in advanced packages. A limitation of the TTC in paper [D] is the absence of a 4-wire connection to the heat source and temperature sensors on the TTC, which introduces uncertainty in the measurement. This could be addressed in future designs. An advantage of the proposed approach is that GaN technology supports operation at higher temperatures and power densities than many silicon-based processes. In paper [D], power densities exceeding 25 W per mm² of die area were demonstrated for short pulses.

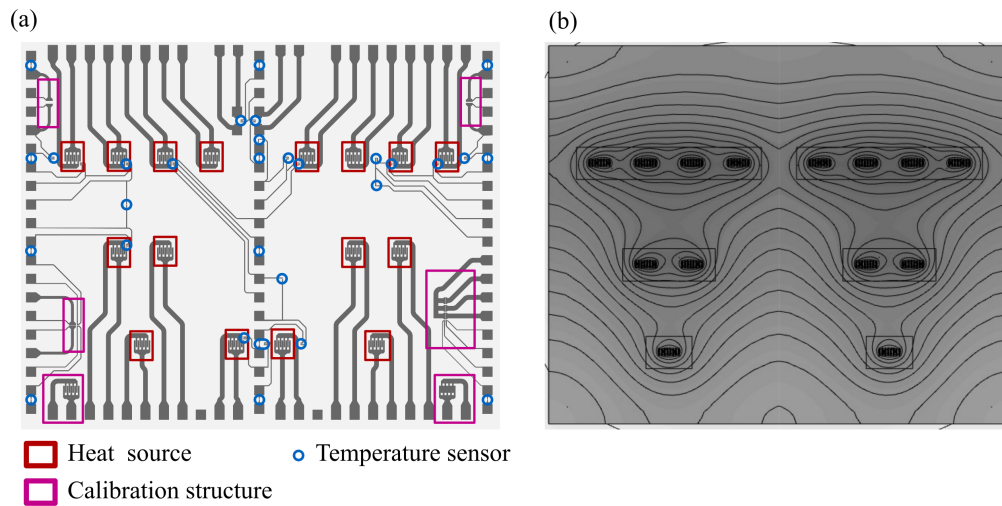


Figure 4.4: Revised TTC design. (a) Layout of the TTC, with the heat sources, temperature sensors, and calibration structures indicated. (b) Simulated temperature distribution for design in (a).

A revised TTC design is presented in Fig. 4.4, intended for integration into an advanced SiP module using flip-chip mounting. This design shows how the approach of paper [D] could be scaled to larger, more realistic circuits. The design incorporates passive short- and open-circuit variants of the heat source to analyse transmission-line effects at the connection to the heat source. Additionally, a transfer length method (TLM) structure is included to measure ohmic contact resistance, and a structure similar to that investigated in paper [A] is implemented for simpler thermal experiments. A key uncertainty for flip-chip-mounted dies is the impact of heat transfer through the solder balls on the temperature distribution. To address this, heat sources and sensors are positioned near the solder balls, similar to the structure used to investigate the TSV in paper [C]. This TTC has not yet been measured.

4.3 Chapter summary

The package is important because it sets the boundary condition for heat transfer from the MMIC to the ambient system and determines the slower parts of the transient response. For a conventional GaN MMIC package, this boundary condition is set by the die-attach, a heat spreader, and a secondary thermal interface. The interface resistance in the die-attach is often uncertain, which is critical because it is located at the point of highest heat flux in the package.

The trend toward advanced packaging makes predicting heat transfer harder and more important, as multiple heat-transfer paths are introduced, additional uncertain thermal interfaces are added, and miniaturisation moves the interfaces closer to the heat generation. Further, materials with lower thermal conductivity are needed to meet mechanical or manufacturing requirements. This will likely cause packaging to play a larger part in the dynamic thermal response in the future. At the same time, advanced packages enable cooling through the topside of the MMIC in addition to heat transfer through the substrate.

Thermal test chips are an important technique for characterisation of future assemblies without optical access. Here, a TTC with a matching material system and layout-level heat-dissipation to a GaN MMIC is proposed. The results in paper [D], obtained in a conventional package, indicate the TTC can also be used for future advanced packages.

Chapter 5

System level

The final stage of the dynamic thermal response involves heat transfer to the ambient environment, which establishes the boundary condition for the previously discussed heat transfer processes. Previously, this boundary was represented by an ideal isothermal surface beneath the package. In this context, the system level denotes the hierarchical level at which heat is transferred to the ambient by convection. Traditionally, heat transfer to the ambient is considered slow and is treated as part of the steady-state regime. However, advancements such as embedded cooling have shifted convection boundaries closer to the heat source, causing the system-level response to enter the transient earlier. Additionally, multi-module systems introduce thermal coupling between modules, further complicating the prediction of boundary conditions. This chapter outlines these challenges and describes the development of an experimental setup designed to address system-level heat transfer.

5.1 Cooling integration

Heat transfer to the ambient environment occurs primarily through convection, facilitated by a circulating fluid, or by radiation. The convection process can be described by the heat transfer coefficient $h = q''/\Delta T$, where q'' represents the heat flux removed through a surface and ΔT denotes the temperature difference between the surface and the fluid. For a given dissipated power, h sets the temperature difference required to drive the heat flux across the surface. h depends on the properties of the convective fluid, flow conditions, and geometry. While the detailed relationships governing h are beyond the scope of this chapter, the discussion will focus on their implications for thermal management requirements and the necessary h for specific package designs.

A primary distinction in cooling strategies is between passive and active cooling. Passive cooling relies on natural convection and radiation, resulting in a low heat transfer coefficient, typically below $25 \text{ Wm}^{-2}\text{K}^{-1}$ for free convection to air [66]. This low h necessitates a reduced heat flux at the boundary to limit temperature increases. In contrast, active cooling employs forced convection by circulating a fluid at the boundary, which can increase h to $25\text{--}250 \text{ Wm}^{-2}\text{K}^{-1}$ for air and $100 - 2 \cdot 10^4 \text{ Wm}^{-2}\text{K}^{-1}$ for liquids [66]. Two-phase cooling, involving phase transitions such as boiling or condensation, can further enhance h to magnitudes approaching $10^5 \text{ Wm}^{-2}\text{K}^{-1}$ [66]. However, two-phase cooling by boiling requires the boundary temperature to exceed the fluid's saturation temperature at the system pressure, thereby raising the temperature above ambient. Additionally, the fluid used in active

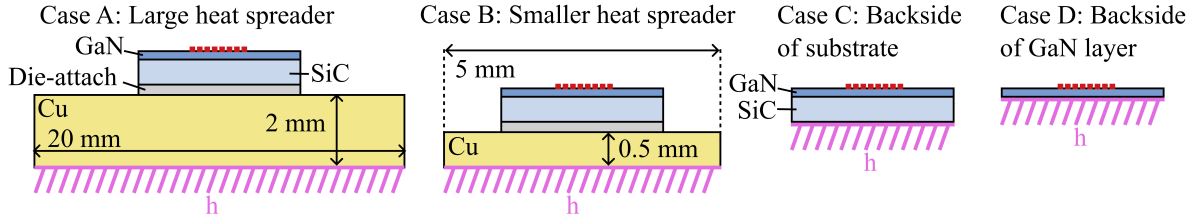


Figure 5.1: Cases investigated in Fig. 5.2.

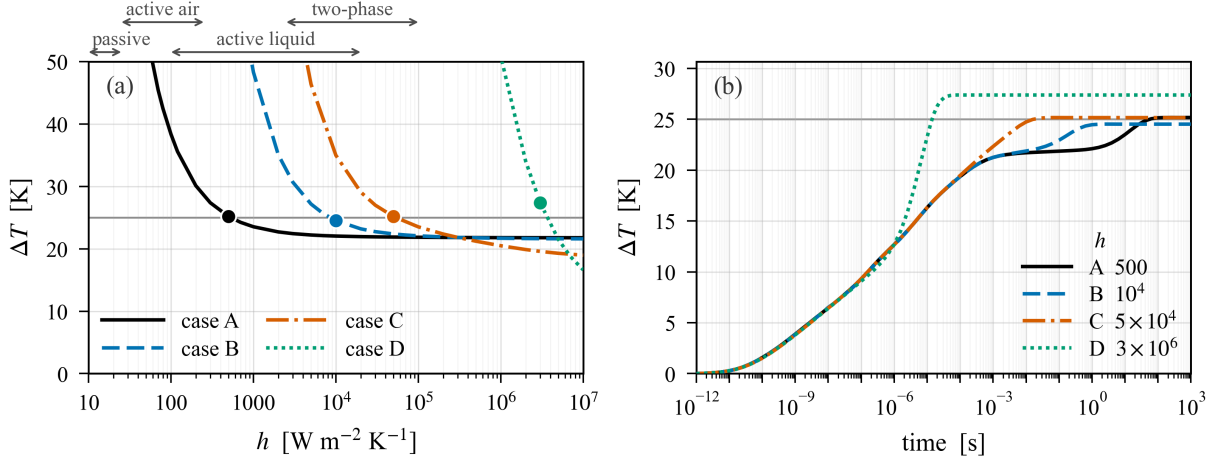


Figure 5.2: Heat transfer coefficient, h , at the cooled boundary for cases A-D from Fig. 5.1 with 1 W/mm power dissipated in an 8-channel device. (a) Steady-state temperature increase versus h . (b) Transient response at simulated point with $\Delta T \sim 25$ K. The corresponding point is marked in (a).

cooling must be maintained above ambient temperature to enable subsequent heat transfer to the environment via a heat exchanger. Achieving higher h values introduces greater complexity in heat sink and cooling system design, can increase energy consumption, and raises sustainability concerns. Active cooling also demands more physical space and may not always be feasible.

A second key consideration is the placement of the cooling boundary. Traditionally, convection is achieved via remote cooling, in which a heat sink is attached to the boundary of the package or module. This approach allows heat to spread over a larger structure before reaching the convective boundary, thereby reducing the required heat transfer coefficient h . However, it also introduces additional thermal interfaces, which can increase the overall temperature rise. In contrast, embedded cooling involves positioning the convective boundary closer to the heat source, as demonstrated by integrating convection within the heat spreader [97], or the substrate [6], [7]. While embedded cooling reduces the number of interfaces between heat generation and convection, it also exposes regions with higher heat flux to convection.

This trade-off is illustrated in Fig. 5.2 (a), where h is varied for the cases depicted in Fig. 5.1. A comparison between case A and case B demonstrates that a larger heat-spreading structure reduces the heat flux at the boundary, thereby relaxing the requirement on h . Consequently, a substantial volume of heat-spreading material is necessary for passive

cooling to be effective. However, the difference between these cases diminishes if h exceeds $10^5 \text{ Wm}^{-2}\text{K}^{-1}$. Case C presents a simulation where h is applied to the backside of the SiC, representing embedded cooling within the substrate. This configuration reduces thermal resistance by eliminating the die-attach interface, but the higher heat flux in this region requires a higher h to ensure effective cooling. Similarly, case D applies a uniform heat transfer coefficient at the boundary of the GaN layer, representing the intrinsic cooling limit for GaN. Due to the elevated heat flux near the channel, this scenario would require an impractically high heat transfer coefficient. It should be noted that applying a uniform heat transfer coefficient at the boundaries in cases C and D underestimates potential improvements, as practical designs typically incorporate pin structures to increase surface area and enable three-dimensional heat spreading, which is not captured in the uniform heat transfer coefficient on a flat surface assumed here. Embedded cooling has demonstrated significant improvements in device performance compared to remote cooling, as shown in [6], and is expected to be particularly effective for Si substrates with lower thermal conductivity, as is the case in [7]. Figure 5.2 (b) demonstrates that the location of the convection boundary influences the transient thermal response; positioning it closer to the heat source causes its effects to manifest earlier in the transient regime. System-level effects therefore matter more for circuit behaviour and design.

5.2 Thermal coupling between modules

The integration of multi-module systems represents a significant trend relevant to this thesis. For example, in active electronically scanned arrays (AESA), transceivers are closely integrated to achieve the required antenna spacing of half a wavelength. When multiple modules share a common cooling system, such as a shared baseplate, thermal coupling between modules must be addressed. As discussed in Chapter 3, heat flux from one module can increase the temperature at neighbouring modules, resulting in uneven temperature distributions and elevated heat flux toward the cooling system. Understanding the implications of such systems is complex, as heat dissipation in the transmitters depends on the applied waveform, the antenna load (which varies with beam steering), and the operating temperature. Fager et al. have investigated this using a behavioural model in [98], employing a thermal coupling matrix to represent these interactions. The thermal coupling matrix must account for both conductive coupling through the antenna and shared baseplates, and coupling via the convective fluid. As the fluid goes through the cooling system, its temperature increases, altering both the heat transfer coefficient h and the fluid's properties. The system's performance thus depends on both fluid temperature and flow rate. The TTC can be used to study these systems in situ, and a next step could be to integrate its temperature sensor into a transmitter circuit.

5.3 Additively manufactured baseplates

Additive manufacturing (AM), commonly called 3D printing, is a disruptive manufacturing technique in which 3D objects are formed layer by layer. In the context of this thesis, it is of interest for realising complex geometries such as integrated cooling channels or microwave filters. At the same time, advances in computational power and artificial intelligence have enabled generative design, in which optimisation algorithms are used to create novel designs.

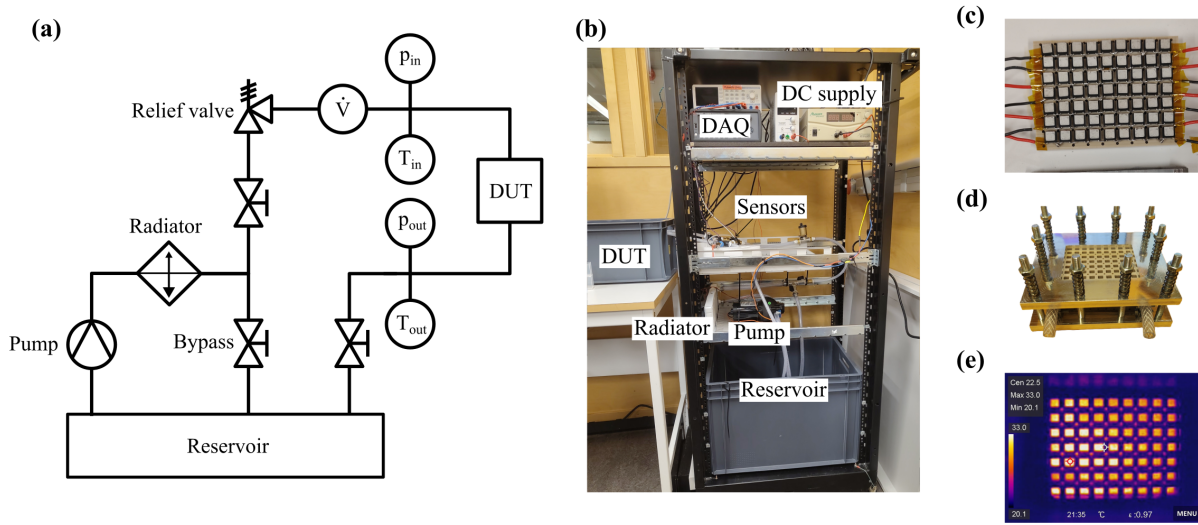


Figure 5.3: Experimental setup for liquid cooling. (a) Flow loop, with pump, reservoir, radiator, bypass, relief valve, and instrumentation for volume flow, pressure, and temperature at the inlet and outlet. (b) Experimental setup. (c) Resistive heater array emulating an active antenna array. (d) Assembled test fixture with resistive heaters pressed down on baseplate. (e) Infrared image of the powered heater array.

When combined with additive manufacturing, this approach enables the production of heat sinks with complex geometries that offer improved thermal performance [99], [100]. It can also be configured to reduce weight or decrease material usage for enhanced sustainability. These designs are inherently complex, as they must address both conductive and convective heat transfer. However, the increased complexity can make interpretation and verification of the designs less intuitive. Consequently, reliable in situ characterisation methods become increasingly important for validating such designs.

AM is also relevant to this thesis, as it reflects a broader shift from bulk materials with established properties to materials whose structure and properties are defined during manufacturing. For example, in powder bed fusion with a laser beam (PBF-LB), the material's microstructure is determined by melt pool dynamics, powder characteristics and manufacturing parameters, such as laser power and scan strategy [101], [102]. As features are miniaturised, such as in small cooling channels, the feature scale may approach the microstructure scale. Post-processing, including heat treatment, further alters the microstructure and, consequently, the structure's properties. Therefore, integrating additive manufacturing techniques into cooling systems increases the importance of in situ characterisation.

To address the outlined requirements, a test setup was developed to evaluate additively manufactured baseplates with integrated liquid cooling. Figure 5.3 presents the measurement setup and the device under test. The system is based on the baseplate shown in Fig. 5.4 (a), which was designed as part of the mucool project.¹ The plate, manufactured by RISE using PBF-LB with an aluminium alloy, is intended to cool an active antenna array comprising 7×9

¹*Multifunctional cooling and electrical interposer for RF wireless systems based on additive manufacturing*, supported by Vinnova, Chalmers, Ericsson, RISE, and Saab. Vinnova reference number: 2021-01328.

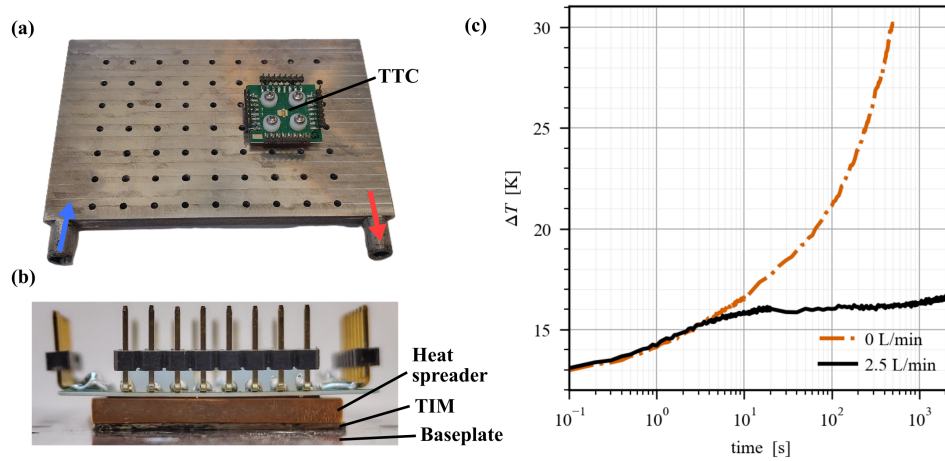


Figure 5.4: TTC from paper [D] mounted on an additively manufactured baseplate with liquid cooling. (a) TTC on the plate. (b) Side view of assembly with heat spreader, a secondary TIM, and the baseplate. (c) Temperature increase measured on S_4 of the TTC, for a 5.6 W step in dissipated power, with 2.5 L/min water flow through the plate and no coolant flow (0 L/min). Same transient measurement setup as in paper [D]. The disturbance in the response from 20 s to 100 s is due to a change in the measurement sampling rate.

transmitters spaced 10 mm apart, with a power density of 10 W/cm^2 . The internal structure of the plate is optimised to achieve uniform temperature distribution by strategically arranging the convective area and routing the liquid within the plate using a proprietary design.

During operation, water is circulated through the baseplate using a pump. A large reservoir, radiator, and bypass loop are incorporated to maintain the inlet temperature near ambient conditions. The system measures both the volumetric flow rate through the plate and the pressure drop across it, analogous to the 4-wire resistance measurement technique used in the appended papers for electrical resistance and thermal impedance. In this context, the pressure drop introduced by the device under test (DUT) at a given flow rate reflects the hydraulic cost of integrating the plate into a cooling loop. Additionally, the temperatures of the liquid at the inlet and outlet are monitored, with the temperature difference corresponding to the heat absorbed by the liquid from the baseplate.

As an initial investigation, an active antenna array was emulated using an array of power resistors, as depicted in Fig. 5.3 (c). The resistor array was pressed onto the baseplate using the fixture shown in Fig. 5.3 (d), which was designed to apply uniform pressure to the resistors, minimise heat conduction through the contact points, and provide optical access to the topside of the resistors for infrared thermometry measurements (Fig. 5.3 (e)). A thin thermal pad was placed between each power resistor and the baseplate. This experimental setup enabled evaluation of the baseplate's performance and comparison of different internal designs. However, the use of power resistors introduced two primary sources of uncertainty in the thermal analysis. First, steady-state measurements made it challenging to distinguish the thermal resistance in the interface between the power resistor and the baseplate from the baseplate's own contribution. Second, there was uncertainty regarding the correlation between the temperature measured at the top of the power resistor and the temperature at the interface with the baseplate.

For more accurate evaluation, future work should utilise the dynamic response of a thermal test chip (TTC). This approach was demonstrated using the TTC and module from paper [D], which were mounted on the baseplate with a thermal pad in between, as illustrated in Fig. 5.4. Figure 5.4 (c) presents the temperature increase following a step in dissipated power, both with and without liquid circulation in the baseplate, to assess its impact on the dynamic response. The temperature profiles are similar for the first approximately three seconds. After this, the case without fluid circulation exhibits a rapid temperature rise, while the case with circulation stabilises. Since only the coolant flow differs between the two measurements, this separates the contribution of the cooling system from the rest of the assembly. The gradual temperature increase observed over the next 15 minutes is attributed to the fluid's rising temperature. Results from paper [D] indicate that the TTC, in combination with finite element method (FEM) simulations, can be used to estimate the properties of other layers in the assembly, establishing the TTC as a promising tool for further system-level investigations.

5.4 Chapter summary

The system level establishes the boundary condition for heat transfer from the packaged MMIC to the ambient environment. The selected cooling method determines the amount of heat that can be transferred for a given temperature difference. It indicates when, in the transient, the system level begins to influence the response. Remote cooling allows for a lower heat transfer coefficient but necessitates larger system size and additional thermal interfaces. In contrast, embedded cooling positions the fluid closer to the heat source, requiring a higher heat transfer coefficient to accommodate the increased heat flux. The selection of a cooling strategy thus involves balancing system-level complexity, physical size, and energy consumption.

Additive manufacturing and generative design enable better cooling solutions but make material properties, geometries and heat transfer more complex. In multi-module systems, thermal coupling between modules must be addressed within a complex multiphysical environment. In both scenarios, in situ characterisation and system-level demonstrators are essential for performance evaluation. An experimental setup has been established to assess additively manufactured baseplates with integrated liquid cooling by measuring liquid flow, pressure drop, and coolant temperature rise. Initial measurements have been made, and the TTC from paper [D] has been identified as suitable for future investigations.

Chapter 6

Conclusions

The maximum sustainable power density is constrained by self-heating. As GaN MMICs are integrated into advanced packaging, managing this limitation becomes increasingly complex, and predicting channel temperature is further complicated by broad spatial and temporal scales and uncertain material interfaces that require in situ characterisation. This thesis has examined how the device, integrated-circuit, and package levels influence the dynamic thermal response, employing dedicated thermal test structures, transient measurements, and calibrated finite element method (FEM) simulations. The objectives are addressed as follows:

- i The dynamic thermal response of thermal coupling in GaN MMICs was investigated using a dedicated thermal test structure and calibrated FEM simulations. Thermal coupling has a low-pass response whose magnitude and cutoff frequency decrease with separation. The response is also influenced by substrate material, operating temperature, and the boundary to the package. FEM simulations accurately reproduce these results and can be utilised for layout design and for extracting equivalent thermal networks for circuit simulations.
- ii Thermal characterisation of the through-substrate via in GaN-on-SiC MMICs revealed an increase in thermal resistance and a change of the temperature distribution. Consequently, layout design must balance the reduction of source inductance, thermal resistance, and device footprint.
- iii A thermal test chip (TTC) with a material system and layout-level heat dissipation representative of a GaN MMIC was designed and employed for in situ characterisation. The TTC has sensitivity to materials and thermal interfaces in the package similar to that expected for an actual MMIC, demonstrating its utility for calibrating an FEM model of the system.
- iv An experimental setup was established to evaluate additively manufactured baseplates with integrated liquid cooling, enabling system-level assessments.

Together, these findings describe how the dynamic thermal response of a GaN MMIC is influenced at each level of integration, from channel layout and through-substrate via to die attach and packaging. The methods used here become more important as carrier frequencies and integration density rise, bringing heat sources closer together, while the heat path gets more uncertain interfaces. Accurate prediction of channel temperature therefore requires that these contributions are separated, characterised in situ, and resolved over the relevant operational time scales.

6.1 Future work

The following directions are recommended for future research:

- One limitation of the TTC in paper [D] was the uncertainty in the embedding resistances, which led to uncertainty in the dissipated power. The revised TTC in section 4.2.2 introduces de-embedding structures to mitigate this issue, and correct implementation of these structures is essential for future work. Additionally, quantification of extraction uncertainty in the FEM model should be addressed.
- Comparison of measurement techniques is necessary to ensure reliable results, and further investigation in this area is recommended. The FEM model presented was calibrated against measurements of thermal coupling and the TTC. For comprehensive validation, the model must also be calibrated against device temperature using an appropriate method.
- Since many circuit solvers work in the frequency domain, frequency-domain characterisation, e.g. with multi-cosine signals, should be explored in addition to the transient measurements employed here.
- Future research should consider implementing a non-linear model for thermal coupling that accounts for temperature dependence.
- Integration of a sensor into a packaged MMIC is recommended to verify thermal performance before product integration, monitor module health over its operational lifetime, and compensate the bias point or linearisation based on operating temperature. The use of an integrated temperature sensor is also relevant for in situ characterisation of active antenna arrays.
- This thesis motivates additive manufacturing for advanced integration and multi-module systems, but characterisation methods for such structures still need to be developed.

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Tobias Kristensen

Gothenburg, September 2026

Appendix A

Configuration of FEM simulation

Finite element method (FEM) simulations presented in this thesis are conducted using the COMSOL Multiphysics solver for heat transfer in solids. The simulation setup is designed to represent a typical GaN high-electron-mobility transistor (HEMT), rather than replicate a specific device. The geometry is simplified to reduce computation time. Table A.1 provides an overview of the model variations employed in this work. The selected material parameters are primarily based on paper [A].

Table A.1: Simulation model configuration.

	Device	Two-channel	Multi-channel	MMIC
Used in	Chapter 2	Chapter 3	Chapter 3	Chapters 3 and 5
Figures	2.1–2.4	3.1, 3.2–3.7	3.8	3.9–3.11, 5.2
Geometry	Fig. A.1	Fig. A.2	Fig. A.2	Fig. A.3
MMIC (mm)	1×1	1×2.5	1×2.5	3×2
Heat spreader (mm)	$1.2 \times 1.2 \times 0.2$	$1.2 \times 2.7 \times 0.2$	$1.2 \times 2.7 \times 0.2$	$3.5 \times 2.5 \times 0.2$
Channels	1	2	8	6×8
W_g (μm)	75	75	75	75
S_C (μm)	–	5–500	20, 40, 80	20
Heat source $w_h \times h_h$ (nm)	100×50	as device	as device	200×50
Au metallization	gate, S/D	gate	gate	no
SiN passivation	yes	as device	as device	no
Symmetry plane	yes	as device	as device	no

The device-level model depicted in Fig. A.1 serves as the reference model for the other variations. A geometry resembling a device is implemented with drain, gate, and source contacts, along with a thin SiN passivation layer. A $100 \times 50 \text{ nm}^2$ heat source is positioned adjacent to the gate, with a width typical of a scaled device [20]. The device is extruded along a $75 \mu\text{m}$ -wide gate. It is placed in the centre of a $1 \times 1 \text{ mm}^2$ MMIC, mounted on a $1.2 \times 1.2 \times 0.2 \text{ mm}^3$ copper heat spreader. These dimensions and the heat spreader are chosen to give a relevant boundary condition. The design is symmetric about a plane perpendicular to the gate, and a symmetry plane is incorporated to reduce the computational domain.

The material parameters used are listed in Table A.2, and are chosen to be representative of the material. The temperature dependence of thermal conductivity is incorporated according to Eq. A.1. The specific heat capacities of GaN and SiC are modelled as temperature-dependent, as described by Eqs. A.2 and A.3, [31], [32]. Anisotropic properties are accounted for in the SiC substrate [28]. Thermal boundary resistances are included at the GaN-SiC interface to

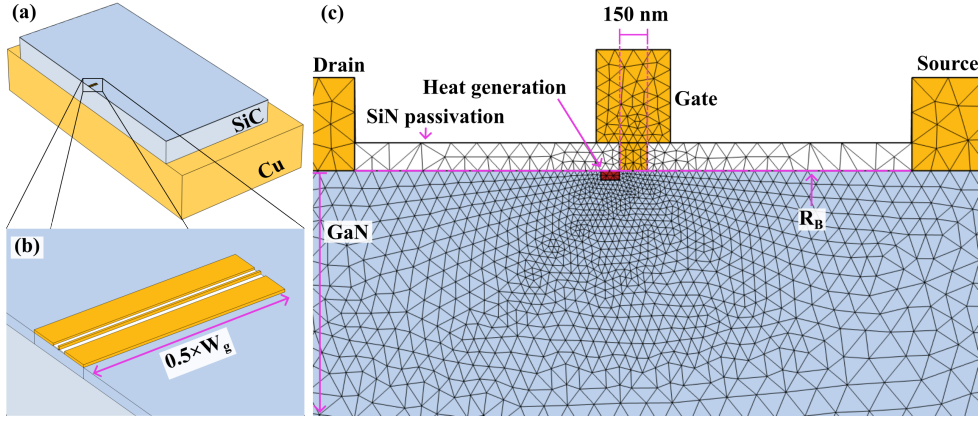


Figure A.1: Device model (a) View of computational domain. (b) Close-up of the device metallization. (c) Cross-section next to the gate, with the meshing indicated.

represent the nucleation layer [10], [11]. Interfaces between GaN and both the passivation and gate metal are included to represent the barrier layer, assuming a similar magnitude to the TBR. The resistance in the die attach is implemented based on the magnitude seen in paper [D]. Values for these interfaces are provided in Table A.3.

$$\kappa(T) = \kappa_{300K} \left(\frac{T}{300K} \right)^{-n} \quad (\text{A.1})$$

Table A.2: Material parameters. κ_{300} and n refer to Eq. (A.1). Materials without n have a constant conductivity. [A], [28], [80], [103]

Layer	Material	Thickness	κ_{300} (W m ⁻¹ K ⁻¹)	n	ρ (kg m ⁻³)	C_p (J kg ⁻¹ K ⁻¹)
Epitaxial layer	GaN	2 μ m	150 (effective)	1.5	6150	Eq. (A.2)
Substrate	SiC	100 μ m	414 (in-plane) 345 (out-of-plane)	1.5	3210	Eq. (A.3)
Substrate	Si	100 μ m	150	1.3	2328	702
Substrate	Diamond	100 μ m	1300	0.9	3510	471.5
Metallization	Au	-	317	-	19320	129
Passivation	SiN	150 nm	2	-	2500	700
Heat spreader	Cu	Table A.1	401	-	8960	385

Table A.3: Thermal contact resistances of the reference model.

Interface	Symbol	R'' (K m ² W ⁻¹)	Represents
GaN / SiC	R_{TBR}	$2 \cdot 10^{-8} (T/300 \text{ K})^{1.2}$	TBR (nucleation layer)
GaN / SiN, GaN / gate metal	R_{B}	$1 \cdot 10^{-8}$	Barrier layer
SiC / Cu	R_{DA}	$1 \cdot 10^{-6}$	Die attach

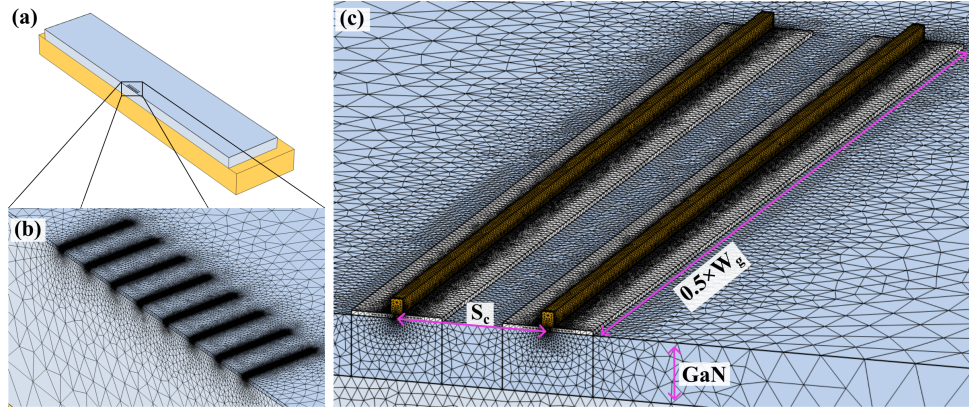


Figure A.2: Multi-channel model (a) View of computational domain. (b) Close-up of eight-channel device with meshing. (c) Close-up of two-channel device with meshing

$$\begin{aligned}
 c_{p,GaN} = & 7.1380 \cdot 10^{-17} T^6 - 2.9836 \cdot 10^{-13} T^5 \\
 & + 4.2185 \cdot 10^{-10} T^4 - 1.5068 \cdot 10^{-7} T^3 \\
 & - 1.6713 \cdot 10^{-4} T^2 + 0.1774 T \\
 & - 1.3545 \text{ Jmol}^{-1} \text{K}^{-1}
 \end{aligned} \tag{A.2}$$

$$\begin{aligned}
 c_{p,SiC} = & 63.38915 - 1.23593 \cdot 10^4 T^{-1} \\
 & + 0.39875 \cdot 10^6 \cdot T^{-2} \text{ Jmol}^{-1} \text{K}^{-1}
 \end{aligned} \tag{A.3}$$

Dissipated power is modelled as uniform heat generation within the volume indicated in Fig. A.1. The power dissipation follows a step function, increasing from 0 W at the initial condition to 1 W/mm with a 1 ps rise time, and is smoothed using two derivatives. This rise time is intentionally set to be faster than the expected heat-transfer response in the solver. The time-dependent solver uses an initial time step of 0.1 ps to resolve the transient, and the step is relaxed during the transient using a logarithmic time step. The solution starts from a uniform temperature of $T_A = 40^\circ\text{C}$. The backside of the copper heat spreader is maintained at $T_A = 40^\circ\text{C}$, except in the simulation shown in Fig. 5.2, where a heat transfer coefficient referenced to $T_A = 40^\circ\text{C}$ is applied. All other ambient boundaries are treated as adiabatic. Device temperature is reported as the peak temperature within the GaN domain, unless specified otherwise. Meshing is performed using a tetrahedral mesh, refined near the heat source to resolve steep temperature gradients, with mesh density reduced in regions farther from the source to optimise computational efficiency. An iterative algebraic multigrid solver is employed to handle the large computational domain.

The single-device model is extended to a multi-channel configuration using the geometry illustrated in Fig. A.2. In this setup, two channels are separated by a distance S_C between their gates, with $S_C = 20\mu\text{m}$ adopted as a typical value for reference simulations. The device is simplified in this geometry by removing the drain and source metallization. A wider

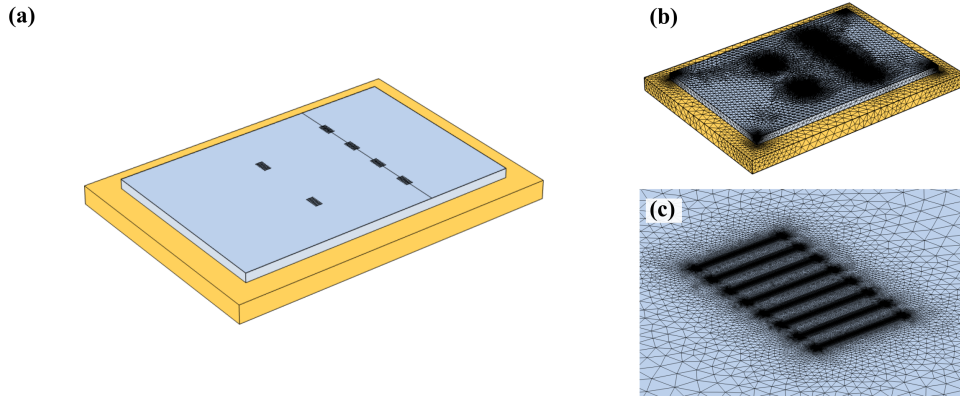


Figure A.3: MMIC example (a) Computational domain. (b) Computational domain with meshing. (c) Close-up of eight-channel device with meshing.

simulation domain, as shown in Fig. A.2 (a), is employed to ensure consistent boundary conditions during the sweep of S_C .

For the larger MMIC example analysed in section 3.1.3, the symmetry plane is omitted. To further reduce the computational domain, the heat-source width is increased to 200 nm, and both the gate and passivation layers are excluded. The device temperature is determined as the peak value within the device. The heat transfer coefficient sweep depicted in Fig. 5.2 is conducted within this simulation, with only device 4 from Fig. 3.9 included. In this scenario, the fixed-temperature boundary on the backside of the heat spreader is replaced with a convective heat-transfer boundary at the surface. The heat spreader dimensions are modified, and the convective boundary is relocated to the backside of the substrate and the backside of the GaN layer, as detailed in section 5.1.

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