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PAPER

Distributed charge-trap dynamics in graphene transistors revealed by RF impedance dispersion

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Abstract

Charge trapping at the graphene/dielectric interface is a major source of instability in graphene transistors, yet its signature in the radio-frequency electrical response remains poorly understood and characterized. This work reports that trap-related charge exchange along the graphene channel produces a distinct, frequency-dependent dispersion in the transistor output impedance, observable from standard microwave measurements without dedicated stress or pulsed-bias protocols. This dispersion primarily affects the reactive part of the output impedance, particularly at low frequencies, and gradually diminishes toward the GHz range, consistent with a distribution of trap relaxation times along the channel. To capture this behavior, a non-uniform transmission-line model is developed that treats channel trapping as a spatially distributed process. An equivalent lumped circuit, consisting of a single *RC* branch in parallel with the channel resistance, reproduces the distributed response accurately, and explicit analytic relationships between both representations enable extraction of local distributed-model parameters from the lumped circuit. The equivalent capacitance converges to a stable value as the number of distributed trapping sections increases, whereas the effective time constant remains dependent on trap position, preserving information about the distributed nature of the phenomenon. Using the converged values, the extracted interfacial trap density is consistent with reported values for graphene/AlOx interfaces, and the extracted trap dynamics depend systematically on channel aspect ratio, identifying device geometry as a means of tuning the frequency range over which trap-induced dispersion is observable. Excellent agreement between model and experimental data is demonstrated across the full characterization frequency range, and the resulting trap-aware description further improves prediction of the device input reflection coefficient. This work establishes high-frequency electrical characterization, interpreted through a distributed-to-lumped framework, as a non-destructive, quantitative route to probe the density, spatial distribution, and dynamics of traps in graphene channels, with direct relevance to interface engineering and defect characterization of graphene devices.

1. Introduction

Graphene field-effect transistors (GFETs) have attracted significant interest due to their outstanding electronic properties, such as high carrier mobility, ambipolar conduction, and excellent electrostatic control [1]. These features make GFETs a widely studied platform, both as a testbed for probing charge transport and defect physics in two-dimensional systems [2, 3], and as a candidate technology for

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high-frequency (HF) electronics [4], biosensing [5, 6], low-noise amplifiers [7], and flexible electronics [8, 9]. Across these applications, device performance and stability remain strongly limited by non-idealities intrinsic to graphene/contacts and graphene/dielectric interfaces, notably contact resistance [10] and charge trapping at border trap sites [11, 12]. These trap states (commonly associated with adsorbates, dangling bonds, or defects introduced during the fabrication process) are known to produce hysteresis, bias-dependent phase shifts, and degradation of the static and dynamic GFET performance [13–16]. Hence, understanding and characterizing charge trapping at graphene interfaces is not only a reliability concern for graphene transistors, but also a broader materials-science question relevant to interface engineering, dielectric integration, and defect control in two-dimensional systems [3, 17].

Charge trap dynamics in graphene devices span a broad range of time scales, from sub-nanosecond to millisecond regimes, depending on trap energy depth, spatial location, and temperature [18, 19]. This broad distribution challenges the common assumption, inherited from conventional semiconductor technologies, that trapping is inherently 'slow' and therefore negligible at microwave frequencies. Faster trap states, particularly those near the graphene/oxide interface, may therefore respond within the period of a GHz signal, perturbing the HF electrical response of the device. This observation motivates HF electrical measurement not merely as a circuit-characterization exercise, but as a potential spectroscopic probe of trap dynamics that are otherwise difficult to resolve with conventional DC or low-frequency techniques. Distributed *RC* network descriptions to capture spatially non-uniform trap activity from HF measurements have proven valuable in incumbent device technologies [20–22], suggesting that an analogous framework could offer new physical insight when applied to graphene channels.

For GFETs, physics-based compact models accounting for mechanisms such as mobility degradation and trap-assisted tunneling within the static channel potential definition have been proposed [14, 23], establishing a foundation for reliability-aware device modeling. However, a framework capable of resolving how distributed trap dynamics manifest in the small-signal HF impedance of GFETs from routine microwave measurements has not yet been reported. Addressing this gap is relevant both to the reliability of RF circuits employing GFETs, where trap-induced impedance mismatch can degrade load matching, power transfer, and stability in microwave applications [24, 25], and, more fundamentally, to the broader effort of characterizing charge-trap populations in graphene and other two-dimensional channel materials using accessible, non-destructive electrical techniques [26, 27].

In this work, a measurable, frequency-dependent dispersion of the GFET output impedance is shown to be produced by dynamic charge trapping along the graphene channel. Furthermore, a modeling framework is developed which is capable of extracting the spatial and dynamic characteristics of this trapping activity directly from standard *S*-parameter measurements. A small-signal GFET model is extended here by describing the impact of traps in two manners towards describing the distributed nature of trap dynamics in these devices [16]: a single lumped *RC* branch, offering a compact and experimentally accessible representation, and a distributed *RC* network, offering a physically grounded picture of trap activity distributed along the channel. An explicit correspondence is established between the two descriptions, showing that they converge under well-defined conditions, and use this correspondence to extract trap parameters. Experimental validation using HF measurements up to 20 GHz demonstrates excellent agreement between the proposed framework and measured output impedance. Beyond providing a compact and reliability-oriented RF modeling tool, to the best of the authors' knowledge this represents the first framework to link trap-induced dynamics in the small-signal HF response of GFETs to a physically interpretable, spatially resolved picture of channel trap distribution, establishing HF electrical characterization as a practical, non-destructive route to probe charge-trap physics in graphene and related two-dimensional channel materials.

2. Description of devices and experiments

The top-gate GFET technology used in this work has been fabricated using standard e-beam lithography on monolayer graphene grown by chemical vapor deposition (CVD) and transferred onto a high-resistivity Si substrate with a 1 μm-thick SiO_2 layer. The graphene channels were patterned by O_2 reactive-ion etching to define stripes with widths of 5 μm and 10 μm, which correspond to channel widths of $W = 10$ μm and 20 μm, respectively, while the gate lengths were $L = 1$ μm and 2 μm. Three devices from this technology have been used in this work. The two gate fingers consisted of evaporated Al (200 nm in an e-beam evaporator at $\sim 10^{-6}$ mbar), which naturally formed a ~4 nm-thick AlO_x layer acting as the gate insulator when exposed to ambient air [28]. Source and drain contacts were defined by Au evaporation without adhesion layers to minimize contact resistance [29]. A scanning electron microscope image (SEM) of one of the devices is shown in figure 1(a).

The native AlO_x/graphene interface formed by this process can introduce interface trap states in graphene devices, associated with non-ideal Al–O

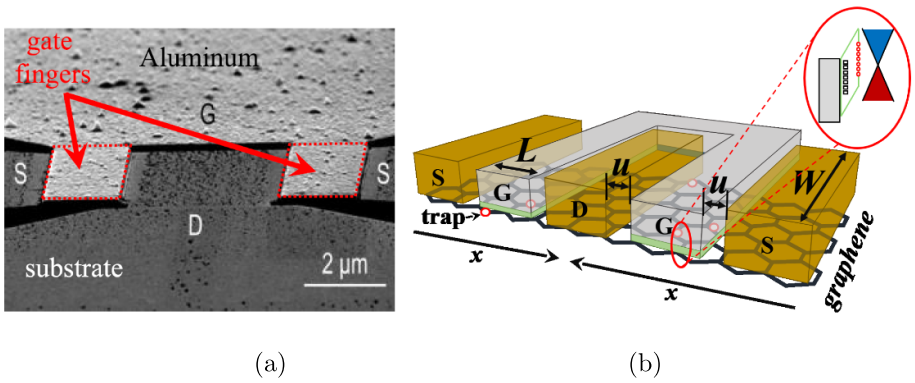


Figure 1. (a) SEM image of a GFET used in this work. (b) Simplified sketch (not to scale) of the GFET structure, where channel length is L, channel width is W, and the length of the access region is $u = 20$ nm. Inset: schematic band diagram of the gate-dielectric-graphene stack where circles (squares) represent the interface (deep) traps.

bonds, residual moisture, and structural disorder introduced during oxide nucleation on the graphene surface [3, 30, 31]. This trap-prone interface makes this GFET technology a suitable and representative platform for investigating the electrical signatures of charge trapping addressed in this work.

The resulting device structure is comparable to other wideband GFETs reported in the literature, making it suitable for RF characterization and modeling purposes. This GFET technology has been used previously for other parameter extraction studies where DC device characteristics are shown [32, 33]. The gate oxide capacitance per-unit-area and the low-field mobility for this GFET technology are estimated as 13.4 mF m^{-2} and 4133 cm^2 V^{-1} s^{-1}, respectively, as obtained elsewhere from microwave measurements [33]. A simplified sketch of the device geometry is presented in figure 1(b), illustrating L, W, and the access regions with length u. Charge traps are assumed to be predominantly located at the interface between the gate oxide and the graphene channel, distributed along both the channel width and length, and are expected to influence charge transport from drain to source through dynamic capture and emission processes. This schematic is not to scale and conceptually highlights the one-dimensional spatial coordinate, x, employed in the subsequent modeling of trap dynamics.

2.1. HF measurements

The devices were characterized in a common-source configuration using ground-signal-ground pads and RF probes connected to a vector network analyzer, enabling S-parameter measurements up to 20 GHz. Bias conditions were set to $V_{DS} = 0$ V in order to include the zero transconductance (cold-FET) condition, with gate–source voltage (V_{GS}) swept from −0.5 V to 1.5 V in 0.25 V steps. A wideband off-wafer calibration method was performed, which allows establishing a 50 Ω-reference. Furthermore, a two-step de-embedding procedure with on-wafer *open* and *short* dummy structures was applied to remove pad and interconnection parasitics [34]. Self-heating effects are not considered in this study as the cold-FET condition ($V_{DS} = 0$ V) makes the intrinsic power dissipation negligible [35, 36].

The Dirac point bias condition was selected for the trap-dispersion analysis reported in this work, since at $V_{GS} = V_{Dirac}$ the channel conductivity is minimized and the device impedance becomes most sensitive to slow charge dynamics at the graphene/oxide interface, maximizing the visibility of trap-induced dispersion in the measured output impedance. This condition thus provides a favorable operating point for isolating and characterizing the trapping response directly from standard S-parameter measurements, without requiring dedicated electrical stress or pulsed-bias protocols. Hence, the analysis focuses on the Dirac point bias ($V_{GS} = V_{Dirac} \approx -0.25$ V) at $V_{DS} = 0$ V for the GFET with $L = 2\,\mu$m and $W = 10\,\mu$m, unless stated otherwise. The Dirac point voltage differs for the other devices: $V_{Dirac}|_{L=2\,\mu m, W=20\,\mu m} \approx 0$ V, and $V_{Dirac}|_{L=1\,\mu m, W=20\,\mu m} \approx -0.4$ V.

3. Enhanced equivalent circuit modeling

When a GFET operates under alternating current excitation, a physical mechanism leads to energy dissipation within the graphene channel. This mechanism arises from the periodic charging and discharging of traps distributed along the channel: as carriers are captured and emitted at trap sites associated with the graphene/oxide interface and gate dielectric, they introduce both a delay in the channel current and an additional lossy component to the impedance, effectively turning the channel into a frequency-dependent RC network [37]. This behavior reflects a general feature of charge-trap dynamics at two-dimensional-material interfaces, where structural and chemical disorder at the dielectric interface

can generate a broad energetic and spatial distribution of trap states [3, 30].

At low frequencies, deep traps can follow the excitation and contribute strongly to energy loss, while at high frequencies only the fastest traps remain active. The former type are mainly buried within the gate oxide whereas the latter are distributed along the graphene-oxide interface (see inset of figure 1(b)) [18, 19]. This behavior explains the dispersion observed in the small-signal output impedance reported elsewhere [20]. To account for trap-related energy-dissipation effects, the zero-transconductance small-signal GFET model, whose elements are explained in detail in [32], is progressively extended: first by introducing a lumped single-pole trap branch, then by generalizing to a distributed trap network through the formulation of a non-uniform transmission line representation that captures the full multi-exponential nature of trap dynamics. As shown for MOSFETs in [38], a lumped model is useful for a first approximation but does not capture the real distributed nature of the device. In the same way, the single-pole trap branch in GFETs is a simplification, since traps are physically distributed along the graphene channel with position-dependent response times, reflecting the spatial heterogeneity of the underlying interface rather than a single, well-defined defect population. This motivates a distributed trap modeling approach that more faithfully represents the actual physical behavior of the device.

Figure 2 includes equivalent circuit descriptions of the same small-signal GFET model under cold-FET conditions. Figure 2(a) corresponds to the compact (or lumped) formulation, which can be regarded as the particular case of the distributed model for a unique trap section, i.e. $n = 1$, where a single trap branch, represented by R_{Tr} and C_{Tr}, summarizes the total trap activity along the channel. Figure 2(b) extends this representation to $n > 1$, where multiple trap branches are spatially distributed to emulate the gradual variation of trapping time constants $\tau(x)$. The latter is described by the combination of a total trap resistance R_{T} and a total trap capacitance C_{T}. Thus, both models are physically consistent and mathematically related, with the lumped case serving as a first-order approximation of the distributed configuration, and the distributed case serving as a physically grounded representation of the underlying trap population. Each approach is discussed in detail next.

3.1. Lumped single-pole trap model

The trap effect is first introduced with a lumped *RC* branch connected in parallel with the channel resistance, as shown in figure 2(a). In this configuration, the equivalent capacitance C_{Tr} accounts for the ability of traps to store charge, while the resistance R_{Tr} is the trap-induced impedance required for defining the

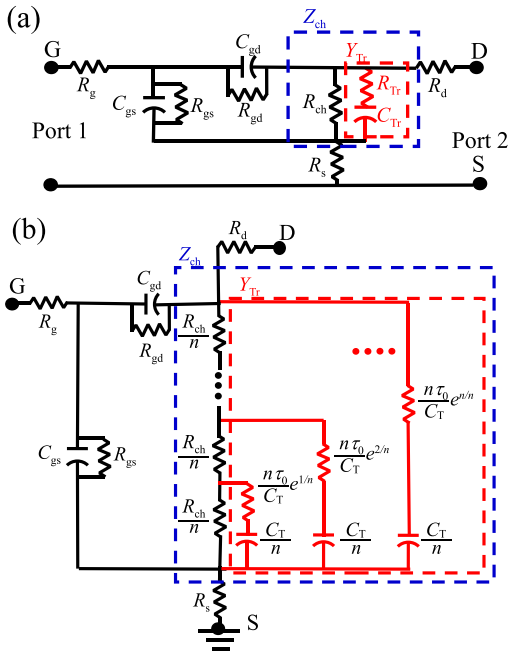


Figure 2. GFET small-signal equivalent circuits under cold-FET conditions: (a) two-port model with trap branch; (b) non-uniform transmission line model (NUTLM) for channel trap dynamics.

average time constant associated with carrier capture and emission. This representation condenses the collective influence of multiple trap states into a single effective branch, which makes the model analytically simple and suitable for circuit simulations. Although this single-pole approximation captures the essential physics of charge trapping and provides a useful first step in the modeling process, it cannot reproduce the multi-exponential response observed experimentally. Although only the channel under the gate is analyzed here, in practice traps are physically distributed in the gate dielectric (deep traps) and at the gate oxide–channel interface (interface traps), exhibiting different time constants depending on their location relative to the conduction path. Hence, the lumped model should be regarded as a first-order approximation, to be refined next by a distributed formulation that retains explicit spatial information.

3.2. Distributed trap network

A distributed trap network can be further interpreted as a non-uniform transmission line model (NUTLM), providing a more physically consistent description of how spatially distributed trap states affect the channel. The NUTLM, represented by the equivalent circuit in figure 2(b), highlights the multi-exponential behavior of trap dynamics and provides a direct analogy with transmission-line theory, where the small-signal current is progressively attenuated and phase-shifted by distributed *RC* elements. The latter approach represents the cumulative effect of charge capture and emission events distributed along the graphene channel.

In MOSFETs with border traps [37], the oxide capacitance is replaced by a distributed *RC* ladder. In GFETs, however, the trap states associated to both the dielectric and channel-dielectric interface induce a modulation of the channel resistance R_{ch}. In this representation, the channel is modeled as a cascade of infinitesimal segments, each consisting of $\Delta R_{ch} = R_{ch}/n$, where n is the number of trap sections into which the channel under the gate is divided, and each segment includes a position-dependent trap branch. This reflects the spatial nature of traps along the channel. Each trap segment is characterized by an incremental capacitance:

$$\Delta C_{bt}(x) = q^2 N_{bt}(x)\,\Delta x, \tag{1}$$

where q is the charge and $N_{bt}(x)$ the traps density per unit energy at position x along the channel.

A uniform trap density along the channel is assumed in this work, following the same physical construction used in established physics-based models of GFETs [39–42]: a spatially uniform trap density, combined with a position-dependent capture/emission time constant, reproduces the broad, decade-spanning distribution of relaxation times responsible for the experimentally observed $1/f$ noise spectrum in these devices. This construction is, however, an idealization of CVD transferred graphene, where wrinkles, folds, and residual transfer-polymer contamination are known to locally modify charge density and interfacial electrical response [43]. Since the present analysis extracts trap parameters from the impedance response of micrometer-scale channels, rather than from any spatially resolved measurement, local deviations of this kind are expected to be averaged out, and the extracted parameters should accordingly be interpreted as effective, channel-averaged quantities. Hence, considering a homogeneous trap distribution, equation (1) simplifies to:

$$\Delta C_{bt}(x) = \frac{C_T}{n}, \tag{2}$$

with C_T as the total trap capacitance, which contributes to the small-signal current only if the operating angular frequency $\omega \leqslant 1/\tau(x)$, where $\tau(x)$ is the characteristic trapping/detrapping time of the trap located at x given by:

$$\tau(x) = \tau_0 e^{x/\lambda}, \tag{3}$$

where τ_0 is the time constant of the fastest traps (closest to the conduction path), and λ is a fitting parameter with values between 0 and L, reflecting how the time constant increases along the channel. In this work, λ corresponds to L to embrace the entire device channel. In MOSFETs multi-exponential models describe deep traps along the perpendicular oxide–channel direction [37]. In GFETs, border/interface traps hosted within the gate dielectric could, in principle, exhibit an analogous depth-dependent response. In this work, the position-dependent time constant $\tau(x)$ is instead formulated along the source-to-drain direction, consistent with the two-port small-signal measurement configuration and the resulting transmission-line analogy adopted. This along-channel formulation is introduced as an effective, mathematically tractable parameterization capable of reproducing the broad distribution of relaxation times required to explain the observed multi-exponential impedance dispersion, rather than as a definitive statement on the microscopic spatial origin of the trap population. The present electrical characterization, based on macroscopic *S*-parameter measurements, cannot distinguish between a lateral and a vertical origin of the observed time-constant distribution.

The resistance associated with each trap, which is in series with $\Delta C_{bt}(x)$, is related to $\tau(x)$ and $\Delta C_{bt}(x)$ through the expression:

$$\Delta R_T(x) = \frac{\tau(x)}{\Delta C_{bt}(x)} = \frac{\tau_0 e^{x/L}}{\Delta C_{bt}(x)}, \tag{4}$$

where the location x is associated with the fraction of the channel modeled in the NUTLM approach, i.e. $x = (k/n)L$ with $k = 1, 2, \ldots, n$.

Although defined as the ratio of trap time constant τ_0 to total capacitance C_T, the effective value of R_T depends on n, and for each distributed configuration, there is a unique value of R_T that makes the distributed model reproduce the one-branch ($n = 1$, lumped) case. Under these conditions, the equivalent circuit becomes purely resistive, allowing the distributed response to be represented by adjusting only R_T. From a physical standpoint, the distributed model indicates that the dominant traps are located near the graphene–dielectric interface, where they effectively modulate the local channel resistance. Deeper traps, having much longer time constants [19, 44], contribute negligibly within the studied frequency range. This spatial selectivity is itself a useful diagnostic: it suggests that the RF impedance response reported here is preferentially sensitive to interface-proximal trap states, the population most directly linked to graphene/dielectric interface quality and fabrication conditions.

The distributed *RC* formulation captures the spatial signature of trap activity along the graphene channel, in contrast to the lumped model, which collapses this spatial information into a single effective time constant. To establish the equivalence between the one-branch and distributed representations, an intermediate analysis was performed in which the trap capacitors were short-circuited to isolate the

resistive behavior of the system. The methodology used to extract the equivalent resistance is detailed next.

4. Parameter extraction methodology

The analysis starts from the conventional small-signal equivalent circuit of the GFET under cold-FET conditions, shown in figure 2(a), where C_{gs} and C_{gd} represent the gate-to-source and gate-to-drain capacitances, respectively, and R_g, R_d, and R_s are the parasitic resistances of the gate, drain, and source. R_{ch} is the channel resistance, while C_{Tr} and R_{Tr} denote the equivalent trap capacitance and resistance, respectively. The equivalent circuits in figure 2 are represented as two-port networks in common-source configuration, where port 1 (input) corresponds to the gate–source terminals and port 2 (output) to the drain–source terminals. The output impedance of each network, $Z_{out} = Z_{22}$, is obtained under open-circuit conditions at the input. Figures 2(a) and (b) are equivalent representations of the same device: the former corresponds to a single trap branch model, whereas the latter generalizes it to the distributed case. The devices were designed with an approximately symmetric structure between the drain and source terminals; thus, at $V_{DS} = 0$ V, it is reasonable to assume that $C_{gs} \approx C_{gd}$ and that the capacitance associated to Z_{22} can be defined as $C_x \approx (C_{gs}C_{gd})/(C_{gs} + C_{gd}) \approx C_{gs}/2$ [32]. R_{gs} and R_{gd} losses associated with C_{gs} and C_{gd} [32] mainly affect the input and have a negligible impact on Z_{22}.

In accordance with the circuit in figure 2(a), and to simplify the analysis, the device's output impedance can be mathematically expressed at high frequencies, such that the angular frequency $\omega \gg 1/\tau(x)$, where the effect of traps is strongly reduced, as:

$$Z_{out} = R_s + R_d + \frac{R_{ch}}{1 + (\omega R_{ch} C_x)^2} - \frac{j\omega R_{ch}^2 C_x}{1 + (\omega R_{ch} C_x)^2}. \quad (5)$$

By this approach, R_{ch} and C_x can be determined at each bias point from the imaginary part of Z_{out} based on the following rearranged linear function:

$$\frac{-\omega}{\mathrm{Im}\,(Z_{out})} = \frac{1}{C_x R_{ch}^2} + C_x \omega^2, \quad (6)$$

as shown in figure 3 for a frequency range from 6 GHz to 20 GHz, where the impact of traps is minimum, i.e. a linear response of the experimental data is observed in contrast to its nonlinear dependence with ω^2 below $\sim$ 6 GHz. Equations (5) and (6) capture the primary response of the device at $\omega \gg 1/\tau$.

At low frequencies, i.e. $<$ 6 GHz in this study, the output device resistance can be expressed as the sum of contact and channel resistances, i.e.

$$R_{out}|_{\text{low frequency}} = R_s + R_d + R_{ch}. \quad (7)$$

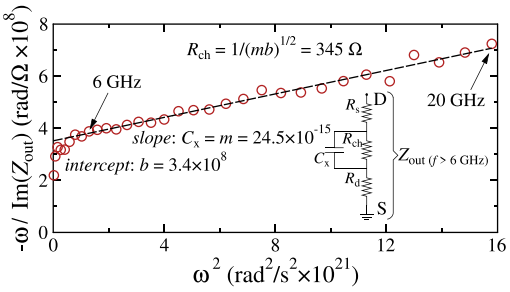


Figure 3. Measured data (markers) and linear regression (dashed line) for the calculation of C_x and R_{ch} at $V_{DS} = 0$ V and $V_{GS} = -0.25$ V, based on equation (6) for a GFET with $L = 2\,\mu$m and $W = 10\,\mu$m.

The source and drain resistances, R_s and R_d, were calculated as shown in equations (2) and (3) of [32], which help providing the reference for the intrinsic response of the device. Although $R_{out}|_{\text{low frequency}}$ would, in principle, include trap effects by considering a parallel combination of R_{ch} with a total trap-associated resistance, in our devices, and at the selected bias conditions, the parallel combination is considered to be dominated by R_{ch}[7]. As a result, the sensitivity of $\mathrm{Re}(Z_{out})$ to the trap-related resistance at low frequencies is weak, making a direct analytical extraction unreliable. In this study, both trap parameters R_{Tr} and C_{Tr} were obtained by fitting the one-branch model to the measured impedance, using the previously extracted R_s, R_d, R_{ch}, and C_x (see table I in [32]) as fixed parameters. The subsequent distributed analysis focuses on the channel-only representations (figures 2(a) and (b)), where a two-step procedure is applied: short-circuiting the trap capacitances to extract R_T, and then reintroducing them to determine C_T.

4.1. Extraction of R_{Tr} and C_{Tr} from the one-branch model

The values of R_{Tr} and C_{Tr} were obtained by fitting the complete model considering trap effects (figure 2(a)) to the measured output impedance in the low-frequency range ($\omega < 1/\tau$), where the trap effects are dominant. In practice, it is not feasible to extract these parameters through a closed-form analytical formulation because the contributions of R_{Tr} and C_{Tr} to both the real and imaginary parts of Z_{out} are strongly coupled and nonlinear. Therefore, the extraction was carried out by adjusting the model

[7] As an example, a value of $R_{ch} = 167\,\Omega$ for the $W/L = 10\,\mu\text{m}/2\,\mu$m device is extracted at zero-transconductance conditions (see table I in [32]) in contrast to the kΩ values for the trap-related resistances obtained here (cf figure 5).

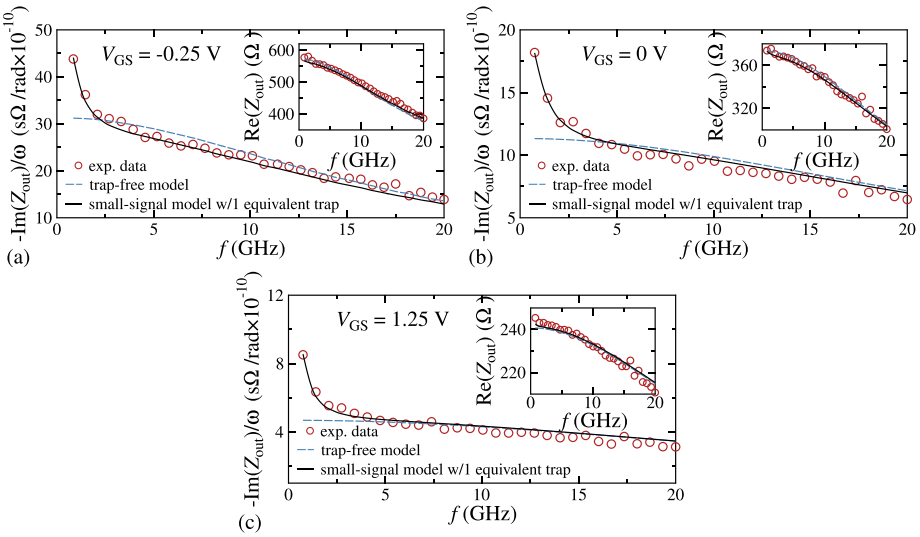


Figure 4. Experimental and modeled GFET output impedance with (solid line, figure 2(a) and without (dashed line, equation (6)) the equivalent *RC* trap branch at different bias points: (a) $V_{GS} = -0.25$ V, (b) $V_{GS} = 0$ V, and (c) $V_{GS} = 1.25$ V. Real (inset) and imaginary part (main). In all cases $V_{DS} = 0$ V ($L = 2\,\mu$m, $W = 10\,\mu$m).

response to the experimental data, while keeping the previously determined values [32] of R_s, R_d, R_{ch}, and C_x fixed. Once the best fit was achieved, the resulting circuit parameters provided a consistent reference for analyzing the intrinsic channel impedance in the following section.

As shown in figure 4, this fitting approach yields excellent agreement with experimental data, reproducing both real and imaginary components of Z_{out} for different bias points. The improvement is most evident at low frequencies, where traps strongly affect the device response. The trend shows a relative error, with respect to the experimental data, below 4% for all the frequency range when the model including traps is considered in contrast to an error of almost 30% at low-frequency if traps are neglected, a clear quantitative signature of the trapping activity at the graphene/oxide interface. At high frequencies ($\omega \gg 2\pi \times 6\,\text{GHz} \gg 1/\tau$), the complete model, including the $R_{Tr} - C_{Tr}$ branch, converges with the trap-free case, confirming that trap effects become negligible as the trap branch behaves as an open circuit dominated by R_{ch} and C_x. Physically, this indicates that even the fastest trap states in this technology relax on timescales that fall below the response window accessible above ∼6 GHz, consistent with the reported broad distribution of trap relaxation times at graphene/oxide interfaces [18, 19]. This validates the consistency of the extraction procedure across frequency decades.

While the one-branch model is useful as a first-order approximation, this approach fails to capture the full multi-exponential behavior observed in experiments. To better reflect the physical reality, a distributed network is introduced.

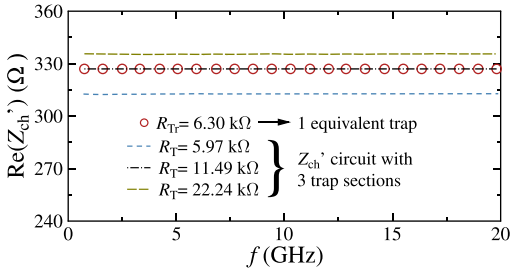


Figure 5. Comparison of the simulated intrinsic channel impedance of the equivalent model and the distributed network with $n = 3$ using different R_T values (below, above, and the equivalent one).

4.2. Extraction of NUTLM parameters

A two-step extraction procedure was employed to simplify the distributed *RC* network related to the trap-affected channel impedance below 6 GHz. In the first step, capacitive branches in figure 2(b) were short-circuited to isolate the resistive contribution and directly extract the parameter

$$R_T = \frac{n\tau_0 e}{C_T}. \tag{8}$$

This is related to the assumption of having a dominant effect of the traps near the graphene-oxide interface, consistent with the physical picture discussed in section 3. An intrinsic channel impedance Z'_{ch} is obtained after removing R_s and R_d, thereby isolating the distributed resistive response and enabling the determination of R_T as a function of the number of trap sections. As shown in figure 5, a unique value of $R_T = 11.49\,\text{k}\Omega$ reproduces the distributed case with

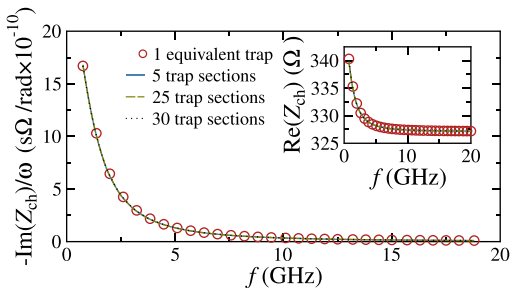


Figure 6. Output channel impedance of the one-branch and distributed trap models: real (inset) and imaginary parts. The one-branch model was parameterized from experimental data, while the distributed model was simulated using the extracted circuit parameters. $V_{DS} = 0$ V and $V_{Dirac} = -0.25$ V for a GFET with $L = 2\,\mu$m and $W = 10\,\mu$m.

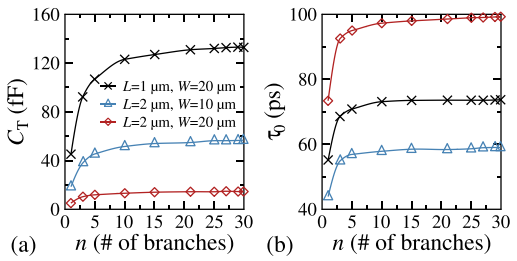


Figure 7. (a) Capacitance C_T, and (b) time constant parameter τ_0 versus the number of branches of the distributed model. At $V_{DS} = 0$ V and $V_{GS} = V_{Dirac}$ for three different transistor geometries.

three trap sections; higher or lower values shift the curves above or below the distributed response.

In the second step, C_T in figure 2(b) is iteratively adjusted until its impedance response (both real and imaginary parts) matches that of the equivalent circuit (figure 2(a)). This fitting is performed in the frequency domain and allows identifying a unique C_T value that faithfully reproduces the cumulative capacitive effects of the distributed trap population along the GFET channel. This analysis is conducted for several configurations of the distributed model, considering different numbers of trap branches: 1, 3, 5, 15, 25, and 30. Varying the number of trap sections enables the investigation of the system behavior as trap density increases and helps assess whether the equivalent model remains valid in different scenarios. Figure 6 presents the correlation between the frequency response of the output channel impedance obtained with the one-branch and distributed trap models for three configurations. In all cases, a strong agreement is observed between the two models, validating the accuracy of the procedure and supporting the applicability of the equivalent model in capturing the distributed trap effects.

This process yields a set of C_T values corresponding to each configuration, providing insights into how the total trap capacitance relates to the number and spatial distribution of the traps. The distributed NUTLM representation has been additionally validated directly against the imaginary part of the output impedance, reproducing the measured data with the same relative error (below 4%) as the lumped model (not shown here as both agreements are visually indistinguishable). Thus, the methodology demonstrates that the distributed *RC* network can be reduced to a one-branch model, with R_T and C_T acting as the effective parameters governing trap-related dynamics in GFETs. This is essential for understanding the device's frequency response and for validating the use of the proposed model in RF circuit simulation environments.

5. Discussion

The extracted values of R_{Tr} and C_{Tr} are 6.3 kΩ and 19 fF, respectively, for the GFET with $L = 2\,\mu$m and $W = 10\,\mu$m at $V_{DS} = 0$ V and $V_{GS} = -0.25$ V. From the values extracted of C_T shown in figure 7(a), for different number of trap sections, it can be observed that, approximately after 21 traps, the ratio $C_T/C_{Tr} \approx 3$, indicating that

$$C_{Tr} \approx C_T/3. \tag{9}$$

This behavior is consistent with analogous modeling strategies previously applied to gate resistance distribution in MOSFETs [38], i.e. just as the distributed gate resistance can be modeled as $R_g/3$, the distributed trap capacitance can similarly be described if the transistor channel is considered as a transmission line (i.e. many traps distributed along the channel due to its length).

In contrast, figure 7(b) shows that the parameter τ_0 continues to increase as the number of trap sections increases. Unlike the capacitance, τ_0 cannot be reduced to a single equivalent constant because the effective resistance depends explicitly on the position of each trap along the channel. Therefore, while the capacitance converges to a stable equivalent value, the resistive contribution (not shown here) retains its distributed nature. The plot was limited to $n =$ 30. However, upon close inspection of figure 7(b), τ_0 also continues to increase with the number of branches used to represent the trap effects in a distributed manner. Although the increment is small, τ_0 never stabilizes and remains dependent on trap number and position. This asymmetry between a converging capacitance and a non-converging, position-dependent time constant is itself physically meaningful: it indicates that while the total trapped charge can be represented by an effective, geometry-independent quantity, the dynamical signature of the trap population retains an intrinsic memory of the underlying spatial distribution of trap sites.

Additional validation of the model was performed by comparing the extracted C_T values for three GFETs

with different channel geometries. The results indicate that the channel aspect ratio L/W is the dominant geometric factor governing the extracted trap dynamics: for larger L, deeper (slower) traps become dynamically active but respond too slowly to contribute within the measurement bandwidth, reducing the effective capacitance; for larger W, current spreading across the channel partially decouples a larger fraction of trap sites from the conduction path, similarly reducing their electrical contribution. As shown in figure 7(b), the device with $L/W = 0.2$ exhibits the lowest τ_0, while the devices with $L/W = 0.05$ and $L/W = 0.1$ exhibit progressively higher values, with the $L/W = 0.1$ geometry showing the largest τ_0 overall. These results confirm that the extracted trap dynamics are geometry-dependent, and indicate that channel aspect ratio is a practical design parameter for tuning the frequency range over which trap-induced dispersion is electrically observable in graphene devices.

A further advantage of this modeling approach is the possibility to extract the trap density at graphene/dielectric interfaces. As an example the values extracted for the GFET with $L = 2\,\mu$m, $W = 10\,\mu$m are used next. Using the total trap capacitance of ~ 56.5 fF (see figure 7(a)) obtained for $n \gg 1$ where the distributed nature of the traps is captured by the multi-branch circuit and C_T approaches an asymptotic value, the corresponding interface trap density can be estimated from $D_{it} = C_T/(q^2LW)$ which follows from the definition of the incremental trap capacitance (see equation (1)) together with the channel area. This yields $D_{it} \approx 1.8 \times 10^{12}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$, a value consistent in order of magnitude with interface trap densities reported for graphene/Al-oxide systems [45, 46]. This value should be interpreted as the density of traps that are dynamically active within the frequency window accessible in this study, as set by the extracted relaxation time of ~ 58.9 ps (see figure 7(b)) and the sub-6 GHz analysis range, rather than the total interface trap density integrated over all trap energies. Nonetheless, this result demonstrates that the proposed distributed-to-lumped framework can extract physically meaningful, materials-relevant trap-density information directly from routine microwave measurements, without requiring dedicated stress or pulsed-bias characterization.

The 1–20 GHz range characterized in this work corresponds to trap time constants between approximately 8 ps (set by the 20 GHz upper limit) and 160 ps (set by the 1 GHz lower limit), consistent with the extracted characteristic time constants $\tau_0 \approx 60$–100 ps (see figure 7(b)). Effects due to traps with shorter time constants would be challenging to be observed in the frequency range, and hence, transient studies are preferred [18, 19]. On the other hand, traps with time constants longer than ~160 ps, extending into the MHz, and kHz range, fall below the lower edge of the characterized window and are therefore not captured by the present approach. Such slower traps are expected to be present, since the decade-spanning $1/f$ noise spectra reported for GFETs [39–41] imply a broad trap-relaxation-time distribution. Hence, the extracted trap capacitances (and interfacial trap density) reported above should be interpreted as a dynamically active quantification corresponding to the frequency range under study rather than due to the total trap population.

Additional mechanisms known to affect GFET HF behavior can be ruled out as the origin of the reported dispersion. Contact resistances (R_s, R_d) are extracted independently and treated as frequency-independent, consistent with prior measurements [32], and their inclusion alone leaves a ~30% low-frequency error (section 4), in contrast to the 4% error once the trap branch is added to the model, showing contact impedance is not responsible for the dispersion. Dielectric losses are already represented in the model through R_{gs} and R_{gd} (see figure 2), which affect the real part of the input impedance at low frequency [32] rather than the trap-related dispersion seen in the output impedance here. Quantum capacitance, set by the graphene density of states, equilibrates on sub-picosecond timescales via intraband carrier scattering, including in CVD-grown graphene [47, 48], such response is far faster than the dynamics considered here, i.e. outside of the GHz range studied. Since quantum-capacitance effects enter only through the total gate capacitance via C_{gs}, C_{gd}, already fixed from the trap-free HF adjustment (section 4), any such contribution is absorbed into C_x. Static carrier-density inhomogeneity reflects a fixed disorder landscape, not a dynamic process on the time scale probed here, and manifests instead as a bias-independent contribution to the DC/low-frequency channel resistance, already captured in the extracted R_{ch} [32, 49]. Furthermore, a time-varying version of this inhomogeneity would itself constitute the trapping mechanism already modeled.

The distributed model has been compared with the complete set of measured S-parameters at three gate–source voltages (figure 8) as an additional consistency check. Under the cold-FET condition used here ($V_{DS} = 0$ V), the device is reciprocal, i.e. $S_{21} = S_{12}$; this is an experimentally observed property of the bias condition and not a constraint imposed on the model. All S-parameters are reproduced simultaneously at each bias, indicating that the extracted circuit describes both the electrical behavior if input and output ports rather than providing a local fit to the output impedance. Since trap-induced dispersion is resolved only in the reactive part of Z_{out}, this test does not isolate the trap contribution. It verifies instead that the trap-inclusive model remains consistent with the full small-signal response,

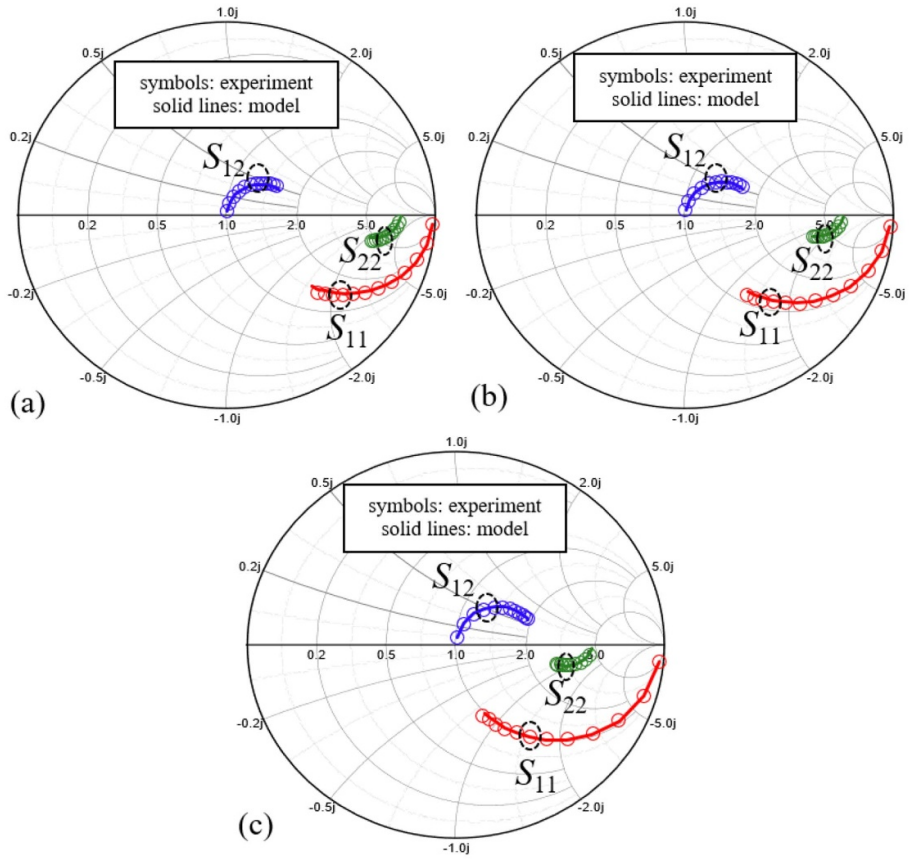


Figure 8. GFET *S*-parameters at different bias points: (a) $V_{GS} = -0.25$ V, (b) $V_{GS} = 0$ V, and (c) $V_{GS} = 1.25$ V. In all cases $V_{DS} = 0$ V ($L = 2\,\mu$m, $W = 10\,\mu$m). Experimental (markers) and modeling (lines) results using the NUTLM approach.

complementing the impedance-level validation of figure 4.

Beyond its diagnostic value for interface characterization, this trap-aware description of GFETs performance also improves circuit-level predictive accuracy: an accurate description of the HF output impedance, as obtained with the trap-inclusive model (see figure 4), leads to a correspondingly accurate description of the device input reflection coefficient Γ_S for frequencies below 3.5 GHz (not shown here). For example, a relative error of ∼3% with respect to experimental data is obtained for the real and imaginary parts of Γ_S when the trap-inclusive model is used, compared to ∼8% when traps are neglected. This confirms that a physically grounded description of interfacial trap dynamics is not only relevant for materials characterization, but is also a practical requirement for accurate circuit-level design of GFET-based RF building blocks.

6. Conclusion

This work establishes a physically grounded link between spatially distributed charge-trapping dynamics along the graphene channel and a measurable electrical signature: a frequency-dependent dispersion of the output impedance in GFETs, accessible directly from standard *S*-parameter measurements without dedicated stress or pulsed-bias protocols. By deriving an explicit correspondence between a non-uniform transmission-line description of channel trapping and an equivalent lumped *RC* circuit, we show that the distributed trap response can be captured by a single relaxation branch without loss of predictive accuracy, providing a practical route to extract local trap parameters from macroscopic microwave measurements. Two results carry particular physical significance: the extracted equivalent capacitance converges to approximately one third of the distributed capacitance as the channel discretization is refined, mirroring analogous distributed-resistance formulations previously reported for MOSFETs and suggesting a degree of universality in how distributed charge-storage phenomena project onto lumped descriptions across different channel materials and physical mechanisms; while the effective time constant retains an explicit dependence on the spatial distribution of trapping sites, showing that lumped-circuit reduction does not fully erase the microscopic, position-dependent character of the underlying trapping process. Using the converged distributed capacitance, we further extracted an interfacial trap density of $D_{it} \approx 1.8 \times 10^{12}$ eV^{-1} cm^{-2} for

the graphene/AlO_x interface studied here, consistent with reported values for comparable graphene/oxide systems and demonstrating that the proposed framework can deliver materials-relevant, quantitative trap information directly from routine microwave characterization. The model reproduces experimental impedance data from 1 GHz to 20 GHz with excellent accuracy, and its trap-aware description was further shown to improve the prediction of the device input reflection coefficient at sub-3.5 GHz frequencies, confirming its relevance for both materials characterization and circuit-level design. Overall, this work establishes HF electrical characterization, interpreted through a physically motivated distributed-to-lumped framework, as a practical, non-destructive spectroscopic tool for probing the spatial and dynamical characteristics of charge traps in graphene channels with direct relevance to interface engineering, defect characterization, and reliability-oriented RF modeling. This approach can be considered as the groundwork for future extensions to temperature-dependent trap activation, large-signal operation, and other two-dimensional semiconductor channel materials.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://zenodo.org/records/17975672 [50].

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